SGS-THOMSON MICROELECTRONICS

L6245

5V HARD DISK DRIVE POWER COMBO

PRODUCT PREVIEW

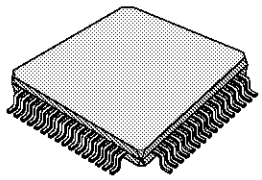
General
- +5V OPERATION
- REGISTER BASED ARCHITECTURE
- MINIMUM EXTERNAL COMPONENTS
- SLEEP AND IDLE MODES FOR LOW POWER CONSUMPTION
- SELECTABLE GAINS FOR BOTH VCM AND SPINDLE Gm LOOP
- LINEAR CURRENT CONTROL LOOPS FOR BOTH VCM AND SPINDLE
- 8 BIT D/A FOR ACTUATOR DRIVER AND SPINDLE DRIVER

VCM Driver
- CURRENT SENSE CONTROL (VOLTAGE PROPORTIONAL TO CURRENT)
- VOLTAGE SENSE CONTROL (VOLTAGE PROPORTIONAL TO THE VOLTAGE ACROSS THE VCM)
- TWO CURRENT RANGES FOR SEEKING AND TRACKING
- INTERNAL REGISTER FOR POWER AMP CONTROL LINES
- SPEED OUTPUT (VOLTAGE PROPORTIONAL TO BEMF)

Spindle Driver
- BEMF PROCESSING FOR SENSORLESS MOTOR COMMUTATION
- PROGRAMMABLE COMMUTATION PHASE DELAY
- PROGRAMMABLE SLEW-RATE FOR REDUCED EMI
- 0.7Ω TYP. FOR ANY HALF BRIDGE
- CROSS CONDUCTION PROTECTION
- SYNTHESIZED HALL OUTPUT

Other Functions
- POWER UP SEQUENCING
- POWER DOWN SEQUENCING
- LOW VOLTAGE SENSE
- ACTUATOR RETRACTION
- DYNAMIC BRAKE
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



PQFP64
ORDERING NUMBER: L6245

DESCRIPTION

The L6245 contains in a single chip all the functions to operate a sensorless brushless (DC) motor and a voice coil motor, suitable for hard disk drive applications.

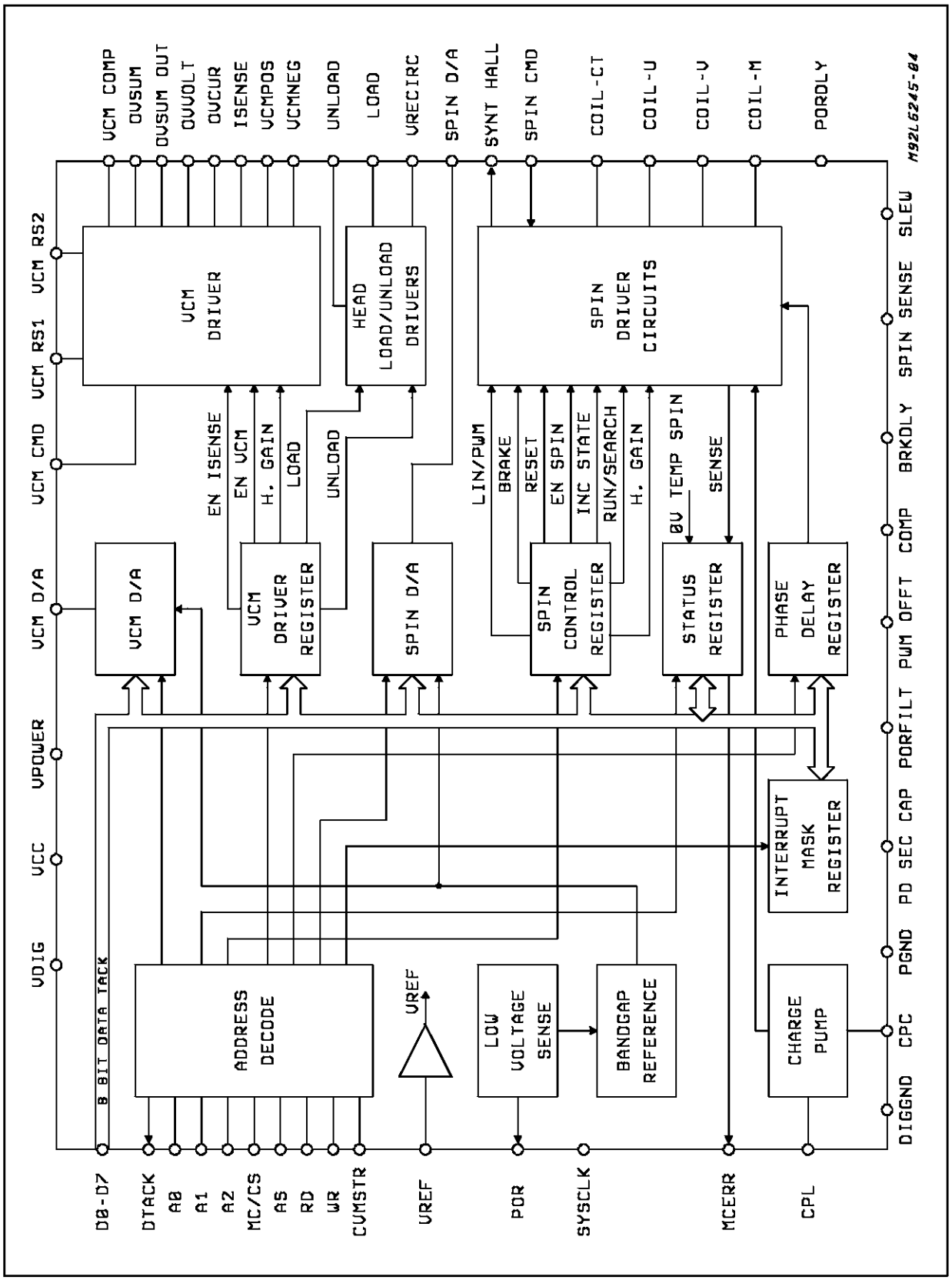
The device is configured to interface directly to an 8 bit parallel microprocessor bus, and has a register based architecture to reduce number of interconnection lines. All the positioning loop for sensorless spindle is integrated, including BEMF sensing, digital masking, digital delay and sequencing. All timing function are performed digitally, thus no external filtering components are required.

The VCM driver is a transconductance amplifier, able to provide 2 different current ranges, suitable for seeking or tracking of the head actuator. When a low voltage is detected, a monitor, in sequence, resets the internal registers, puts in tristate the spindle powers, retracts the actuator, and applies the dynamic brake of the spindle.

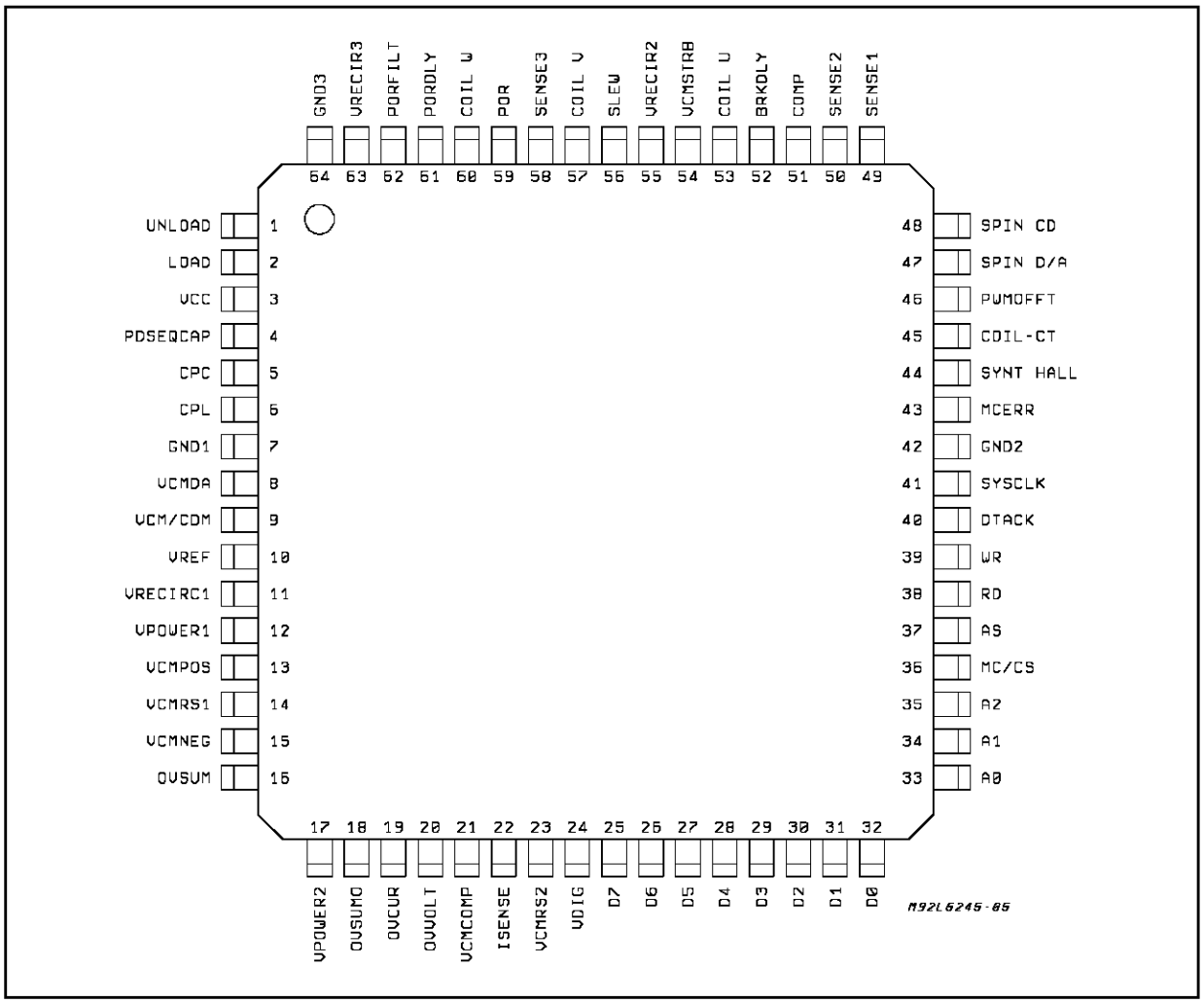
The L6245 is realized in Multipower-BCD 2 technology, which combine isolate DMOS power transistors with CMOS and Bipolar circuits in the same monolithic layer, and is assembled in a 64-pin PQFP.

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
$V_{ds\,sus}$	Peak Output Sustaining Voltage		14	V
V_P; Vcc	Supply Voltage	Power (V_P) Logic (V_{CC})	8 6	V V
V_i	Logic input Voltage		0 to 6	V
V_{cp}	Charge Pump Input Voltage		18	V
I_p	Sink-Source Peak Output Current		1.5	A
I_O	Sink-Source DC Output Current		1	A
P_{tot}	Total Power Dissipation (T_{amb} = 60°C)		1	W
T_{stg}, T_j	Storage and Junction Temperature		–40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (*)	max.	90	°C/W

(*) Mounted on a typical PCB layout (see Fig. 7)

PIN DESCRIPTION [Pin Types: I = Input, O = Output, P = Power, A = Analog (passive)]

Power

Pin Number	Pin Name	Pin Type	Description
12, 17 24, 3	VPOWER VDIG V_{CC}	P	Positive supply, nominally 5V.
7, 42, 64	GND	P	Ground.
10	V_{REF}	I	All analog signals are referenced to this voltage, nominally 2V.
59	$\overline{POR}$	0	POWER ON RESET - Goes low when the supply voltage is below the VOLTAGE GOOD threshold. $\overline{POR}$ is an open collector output with an internal 20kΩ pull-up.
61	POR_DLY	A	POR DELAY. An external parallel RC network from this pin to ground sets the time the $\overline{POR}$ signal stays active after voltage good.
62	POR_FILT	A	An external capacitor from this pin to ground provides filtering for the V_{CC} sense input of the POR circuit.
5	CPC	A	Charge pump capacitor
6	CPL	A	Charge pump inductor

Microprocessor Interface

Pin Number	Pin Name	Pin Type	Description
25 26 27 28 29 30 31 32	D7 D6 D5 D4 D3 D2 D1 D0	I/O I/O I/O I/O I/O I/O I/O I/O	An 8-bit bidirectional data bus which is connected to the internal registers.
38	$\overline{RD}$	I	$\overline{READ}$ A low level on this pin allows the bus to be driven by the IC.
39	$\overline{WR}$	I	A low level on $\overline{WRITE}$ allows the IC to read data from the system bus.
35	$\overline{MC_CS}$	I	$\overline{CHIP\ SELECT}$ A low level on this pin selects the IC for bus transactions.
41	SYSCLK	I	Microprocessor clock used for internal timing.
33 34 35	A0 A1 A2	I I I	The lowest three bits of the system address bus; used to address internal registers
37	AS	I	ADDRESS STROBE The address appearing on A [0:2] is latched on the falling edge of the AS pulse.
43	$\overline{MC_ERR}$	O	A maskable interrupt signal which is asserted low when an error flag in the Status Register is set. The output is open-drain with an internal 20KΩ pull-up.
40	$\overline{DTACK}$	O	An open drain, active low signal used for asynchronous bus transactions.

Brushless, Sensorless Motor Driver and 8 bit D/A

Pin Number	Pin Name	Pin Type	Description
47	SPIN_DAC	O	The output of an 8 bit D/A used for the command to the spindle driver.
48	SPIN_CMD	I	The input to the spindle driver transconductance amplifier.
45	COIL_CT	I	The center tap of the motor is connected to this pin.
53 57 60	COIL_U COIL_V COIL_W	O	The motor coils are driven by these outputs. Back EMF is also sensed at these pins.

PIN DESCRIPTION (continued)

Pin Number	Pin Name	Pin Type	Description
44	SYNTH_HALL	O	A TTL compatible signal that emulates one of the Hall signals. SYNTH_HALL is an open drain output with an internal 20KΩ pull-up.
49, 50, 58	SPIN SENSE 1,2,3	A	The current sensing resistors is connected from these pins to ground.
46	PWM_OFFT	A	A parallel R-C from this pin to ground sets the PWM mode OFF time.
56	SLEW	A	A resistor from this pin to ground sets the slew rate of the driver.
51	S_COMP	A	An R-C network from this pin to GND sets the spin driver compensation.

VCM Driver and 8 bit D/A

Pin Number	Pin Name	Pin Type	Description
8	VCM_DAC	O	The output of an 8 bit D/A used to command the VCM driver.
9	VCM_CMD	I	VCM driver input command which is relative to V_{REF}.
21	VCM_COMP	A	An R-C network from this pin to ground compensates the VCM driver.
14	VCM_RS1	A	The high gain current sense resistor is attached from this pin to ground.
23	VCM_RS2	A	The low gain current sense resistor is connected from this pin to VCM_RS1
13	VCM+	O	One end of the load is attached to this pin (Positive).
15	VCM-	O	The other end of the load is attached to this pin (Negative).
20	OV_VOLT	O	A voltage which is proportional to the voltage across the load, referenced to V_{REF}.
19	OV_CUR	O	A voltage which is proportional to the current through the load, referenced to V_{REF}.
16	OV_SUM–	I	Over-velocity summing op-amp inverting input.
18	OV_SUM_OUT	O	Over-velocity summing op-amp output.
22	ISENSE	O	A voltage which is proportional to the current through the VCM load as sensed by the sense resistor. This signal is enabled by setting bit 2 in the VCM Control Register.
54	VCM_STRB	I	The 8 bit input to the VCM D/A is updated on the rising edge of VCM_STRB.

Solenoid Pre-drivers and Power Down Sequencing

Pin Number	Pin Name	Pin Type	Description
11,55, 63	V_RECIR	P	Under normal conditions, power is supplied to various blocks via the V_RECIR pin. When external power is removed, energy stored in the rotating spindle is converted to a voltage which supplies the park circuit.
2	LOAD_SOL	O	When a logic one is written to bit 3 of the VCM Control Register, current is sourced from the LOAD_SOL pin. Otherwise, the pin is high impedance.
1	UNLOAD_SOL	O	When a logic one is written to bit 4 of the VCM Control Register, current is sourced from the UNLOAD_SOL pin. Otherwise, the pin is high impedance.
4	PD_SEQ_CAP	A	When power is removed, the charge stored on this capacitor keeps selected blocks alive long enough to effect an orderly power down.
52	BRK_DLY	A	An external parallel RC network from this point to ground delays activation of the dynamic brake after power is removed.

ELECTRICAL CHARACTERISTICS (V_S = 5V, T_j = 25°C; unless otherwise specified)

Power Supply Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_S	Supply Voltage	$V_S = V_P = V_{CC}$	4.5		5.5	V
ID-READY	Quiescent Current Dissipation	No load attached VCM and Spin drivers enab.			25	mA
ID_IDLE		VCM driver disabled Spin driver enabled			20	mA
ID_SLEEP		VCM and Spin drivers disabled			4	mA

VCM Driver (Notes 1, 2)

I_{OS}	Maximum Load Current (Seeking)	Output Devices A, B, E, F (Fig. 1)			0.3	A
I_{OT}	Maximum Load Current (Traking)	Output Devices C, D (Fig. 1)			0.1	A
$R_{DS(on)}$	Source & Sink Out ON Resistance	Output Devices A, B, E, F T_j = 125°C (Fig. 1)			1	Ω
$R_{DS(on)}$	Sink Out On Resistance	Output Devices C, D Tj = 125°C (Fig. 1)			2.4	Ω
$R_{DS(on)}$	Sink Out On Resistance	Parking Device Tj = 125°C			12	Ω
V_F	Body Diode Forward Drop	I = 0.3A			1.5	V
V_{jump}	Jump Discontinuity (**)	R_{sense} = 2.01Ω			30	mV
V_{DB}	Deadband Discontinuity (*)	R_{sense} = 2.01Ω			6	mV
V_{CMOS}	Offset (***)	R_{sense} = 2.01Ω			40	mV

(*) The range of input voltages applied to the VCM_CMD pin (with respect to V_{REF}) for which only negligible current is present in the load. This deadband voltage (VDB) can be expressed either in mV or in LSBs, where one LSB is equal to 11.7mV.

(**) A condition in which the transfer characteristic (i.e., load current vs. VCM_CMD-V_{REF}) exhibits a slope which is significantly grater than the desired value. The range of currents for which this condition exists is termed IJUMP. This current is referred o the VCM_CMD input according to the following equation: VJUMP = IJUMP x 3 x RSENSE
In this document, RSENSE is assumed to be 2.01Ω. VJUMP can be expressed either in mV or in LSBs, where one LSB is equal to 11.7mV.

(***) The value of VCM_CMD (with respect to V_{REF}) for which the load current is zero. In parts which exihibit a DEADBAND dicontinuity, the offset is defined to be at the midpoint of the deadband region. RSENSE is assumed to br 2.01Ω.

VCM Current sense amplifier (I_{SENSE})

V_{off}	Output Offset Voltage	VCM_RS2 Shorted to GND O/S is $V_{(Isense)}$ - V_{ref}	–50		50	mV
G	Closed Loop Voltage Gain	3V/V nominal	2.85		3.15	V/V
PSRR	Power Supply Rejection Ratio	at DC	50			dB
BW	Banwwidth		200			KHz
V_{OR}	Output Range	V_{CC} = 4.5V (note 4)	–0.2		3.5	V

VCM Full wave rectifying amplifier

I_B	Input Bias Current	VCM_CMD = V_{ref}			2	µA
I_{imp}	Input Impedance	Impedance seen at VCM_CMD wrt V_{ref}	5			KΩ
G	Closed Loop Gain		0.320		0.347	V/V
PSRR	Power Supply Rejection Ratio	at DC	50			dB
GBW	Unity Gain Bandwidth		200			KHz
CMR	Input Common Mode Range	VCM_CMD pin	0.3		3.7	V
V_{OR}	Output Range		0		1	V

ELECTRICAL CHARACTERISTICS (Continued)

VCM DAC (Notes 5, 6)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Res	Resolution		8			bit
N.L.	Differential Nonlinearity				±0.5	LSB
I.N.L.	Integral Nonlinearity				±0.5	LSB
CT	Conversion Time	From 50% point of $\overline{WR}$ falling to 1% settling			2	µs
Z_O	Output Z				100	Ω
FSTC	Full Scale Temp. Coeff.				200	ppm/°C
V_{OH}	High Output Voltage	Relative to V_{ref} Input Code = 7Fh	1.46		1.52	V
V_{OL}	Low Output Voltage	Relative to Vref Input Code = 80h	–1.53		–1.47	V
V_{ZSO}	Zero Scale Offset	Relative to V_{ref} Input Code = 00			±10	mV

Over velocity detector, coil voltage sense amplifier

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_O	Output Offset Voltage	VCM+ = VCM–, within input common mode range. Measure wrt to V_{ref}	–50		+50	mV
I_{BC}	Input Bias Current	(Note 3)			10	µA
G	Closed Loop Voltage Gain	Av = 0.25V/V nominal	0.242		0.258	V/V
PSRR	Power Supply Rejection Ratio	at DC	50			dB
BW	Bandwidth		200			KHz
CMR	Input Common Mode Range	Above and below these values the op amp will be in saturation and will not invert sign.	0		V_{POWER}	V
V_{DR}	Input Differential Range		0		V_{POWER}	V
V_{OR}	Output Range		0.3		3.5	V
I_O	Output Current		æ400			µA

Over velocity detector, coil current sense amplifier

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_O	Output Offset Voltage	VCM_RS1 shorted to GND for: (a) VCM_CMD < V_{ref} and b) VCM_CMD > V_{ref}. Measure wrt V_{ref}	–50		+50	mV
G	Closed Loop Voltage Gain	Av = 2.5V/V nominal	2.425		2.575	V/V
PSRR	Power Supply Rejection Ratio	at DC	50			dB
Bw	Bandwidth		200			KHz
CMR	Input Common Mode Range		–0.1		2	V
V_R	Output Range		0.5		3.5	V
I_O	Output Current		±400			mA

ELECTRICAL CHARACTERISTICS (Continued)

Over velocity detector, summing amplifier

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_O	Input Offset Voltage				10	mV
I_{BC}	Input Bias Current				1	µA
G	Open Loop Gain		60			dB
PSRR	Power Supply Rejection Ratio	at DC	50			dB
GBW	Unity Gain Bandwidth		200			KHz
V_R	Output Range		0.5		3.5	V
I_O	Output Current		±400			µA

Over velocity detector, window comparator

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_S	Switching Time				50	µs
V_{TL}	Low Threshold	Relative to V_{ref}	–1.32		–1.18	V
V_{TH}	High Threshold	Relative to Vref	1.18		1.32	V

Solenoid pre-driver (Note 7)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{OH}	Output Current	V_{OH} = 1.5V, V_{CC} = 4.4V	10			mA

Three phase sensorless motor driver

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_O	Max. Load Current				0.5	A
$R_{DS(on)}$	Out On Resistance	T_j = 125°C			0.75	Ω
dV/dt	Slew Rate		0.05			V/µs
V_F	Body Diode Forward Drop	I = 0.5A			1.2	V

Motor Current Sense Amplifier

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{BC}	Input Bias Current				1	µA
G	Closed Loop Voltage Gain	Low Gain mode High Gain mode	19.4 4.85		20.6 5.15	V/V V/V
PSRR	Power Supply Rejection Rate	at DC	50			dB
BW	Bandwidth		200			KHz
I_O	Output Range		0		3.2	V

Spin DAC (Notes 8, 9)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Res	Resolution		8			bit
NL	Differential Nonlinearity				±0.5	LSB
INL	Integral Nonlinearity				±0.5	LSB
CT	Conversion Time	From 50% point of –WR falling to 1% settling			5	µs
Zo	Output Z				14	KΩ
FSTC	Full Scale Temp. Coeff.				200	ppm/°C
V_{OH}	High Output Voltage		2.85		3.15	V
V_{OL}	Low Output Voltage	Unloaded	0		20	mV

ELECTRICAL CHARACTERISTICS (Continued)

Step-up converter

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{SU}	Step-up Voltage	Relative to V_{CC}	7		11	V

Microprocessor interface (Note 10)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		3			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage	VCC = 5V, I_{OH} = 400µA	4.4			V
V_{OL1}	Low Level Output Voltage	–MCERR, –POR, –DTACK IOL = 4mA			0.4	V
V_{OL2}	Low Level Output Voltage	SYNT_ALL IOL = 0.5mA			0.4	V
I_{IN1}	Input Leakage Current	–RD, –WR, AS, –MC_CS, SYSCLK, A [0:2]			1	µA
I_{IN2}	Input Leakage Current	D [0:7]			10	µA

Microprocessor interface timing

Trddh	Read Data Hold		5	40		ns
Trddt	–RD High to –DTACK high			40		ns
Twrdt	–WR High to –DTACK High			40		ns

Power on reset

V_{CCHL}	V_{CC} Good, HL	V_{CC} falling	4.2		4.4	V
V_{CCHL}	V_{CC} Good, LH	V_{CC} rising	4.26		4.5	V
T_{PLH}	Rise Time	C_{Load} = 100pF			200	ns
R_T	Response Time				50	µs

Notes:
1) The minimum voltage available from the brushless DC motor after power has been removed is 2.7V
2) The voltage available for actuator etraction shall be greater than 0.7V.
3) Sum of I_{bias+}(V_{ref}/internal resistor + power leakage).
4) Minimum output voltage is set to V_{ref} by a resistor network.
5) The VCM DAC shall be monotonic over its full range.
6) The coding of the digital input shall be 2's complement.
7) The voltage available for solenoid operation shall be greater than 1.9V.
8) The Spin DAC shall be monotonic over its full range.
9) The coding of the digital input shall be uniplar (unsigned binary).
10) SYNTH_HALL, MC_ERR, DTACK and POR shall have open drain (collector) outputs and internal pull-up resistors. The minimum value of these pull-up resistors shall be 20KΩ..

FUNCTIONAL DESCRIPTION

Inside the system is the sensorless Spindle driver (Spin), the Voice Coil Motor driver (VCM), the Head load/unload predrivers, power sequencing, actuator over-velocity detection, actuator retraction and dynamic braking. The architecture of the system is configured to interface directly to an 8 bit, parallel, microprocessor bus.

During the application of power to the system (power-on), the output drivers are held in a disabled state until the applied voltage reaches the Voltage Good Threshold (VGT). During this period of time the output drivers are disabled, the internal register are set to predetermined states, and the Power On Reset (POR) signal is held low. The POR signal is held low from the time the applied voltage reaches 0.7V and the VGT. The POR delay is programmable changing the value of a capacitor.

The VCM driver is driven via a D/A and it can be enabled through the VCM driver register. The VCM driver has a gain capability too. This function is to be accomplished by switching the sense resistor used such that the current sensing feedback in the VCM driver has more information and therefore results in lower deadband, offset current, and gain error. An actuator over velocity sensing circuit is incorporated in the system, which is accomplished by measuring BEMF voltage and comparing to a threshold.

The head load /unload mechanisms are just buffers for driving external power transistors. Controlled internally by Bit 3 and Bit 4 of the VCM Driver Register, each output has a current surcing capability of 10mA.

The Sensorless Spindle Driver function can be accessed from the microprocessor over the data bus to the Spin Register and Spin D/A. The Spin D/A is in Binary format. The operation of the Spindle system is controlled entirely by the microprocessor from start-up to speed regulaton. The spin system is accessible by selecting the Spin Control Register with the address 011 on the 3 bit address bus and has the following functions:

1)Enable (Bit 0): high to enable the spin system, while a low asserts braking of the spindle motor (if VCR enable is low.)
2)Sense amplifier gain (Bit 1): high implies high current mode which is equivalent to low sense amp gain, while a low selects low current mode or high sense amp gain.
3)Unipolar/Bipolar (Bit 2): High selects the Unipolar driving mode.
4)Run/Search Mode (Bit 3): high selects the run mode whereby the Hall synthesizer output gives speed information while a low asserts the search mode whereby the sequencer is under µP control (stepper function).
5)Reset State (Bit 4): a low level resets the commutation state sequencer.
6)Incremental state (Bit 5): toggling of the bit increments the sequencer to drive the output stage when search mode is selected.
7)Linear/PWM (Bit 6): high selects linear mode of driving for current (speed) regulation while a low sets to PWM mode used during start-up.

Start-up current limiting is accomplished by the output of the microprocessor commanded D/A value. Jammed or stuck rotor detection is also done as part of the microprocessor algorithm. Integrated diode are present in the power bridge for BEMF rectification. This rectified voltage is used to retract the actuator and unload or latch the head assembly.

A conventional Bandgap is used to generate internal biasing for the device as well as the reference voltage for the D/A converters.

A Step-up Converter is used to generate a 15V internal supply to drive the upper DMOSs and a regulated 11.6V internal supply to power internal circuits which have voltage head room problem, as well as to drive the lower DMOSs.

A Low Voltage Detector (LVD) is incorporated to sense a severely low value of applied voltage so as to shunt-down the VCM and Spindle drivers. The LVD is activated when the applied voltage drops below 4.3V (+/-0.1V). When a voltage drop is sensed, the LVD:

1. asserts POR, which resets the internal register ;

2. retracts the actuator ;

3. applies the dynamic brake.

When a severe low value of applied voltage is sensed, the motor control system goes into reset mode and also asserts the POR line to reset other circuits. The sub-circuit which get affected by the reset mode in the motor control system are the Spin Control Register, the VCM Driver Register, the Spindle D/A and the VCM D/A. This effectively disables the spin driver, VCM driver, head load/unload driver and initializes the D/A's at zero output command value.

An Over Velocity Detector circuit is integrated to sense when head arms are moving at a speed which could cause a damaging condition. When an over velocity condition is detected sensing the actuator BEMF, the actuator driver is shut off and held off until the microprocessor has detected this condition and then resets the error and retries the access.

The microprocessor has the possibility to put the device in sleep mode, which is asserted when both the VCM and Spindle drivers are disabled through the internal registers (Enable VCM and Enable Spindle). Under this condition, only the POR circuit is kept "alive", thus power consumption is kept at minimal. Before sleep mode is activated, the microprocessor must move the actuator to the unload zone, unload the recording heads, and apply dynamic braking.

All bits of all the registers are readable by the microprocessor interface. Also there are certain bits of the internal registers which are writable as defined in the Register Definition Tables (Tables 1 - 7).

An internal register monitors the internal work of the system and latches certain error condition that are detected.

REGISTER DEFINITION and 3bit Address Code

Table 1: Status Register (A.C. 001)

Bit	Name	POR Initial Value
7	NC	
6	NC	
5	NC	
4	NC	
3	REVERSE SPIN	1
2	OVER TEMP.	1
1	SPIN SENSE	0
0	OVER VEL SET	1

Table 2: VCM Driver Register (A.C. 010)

Bit	Name	POR Initial Value
7	NC	
6	NC	
5	NC	
4	UNLOAD HD	0
3	LOAD HD	0
2	ENABLE ISENSE	0
1	HIGH GAIN VCM	0
0	ENABLE VCM	0

Table 3: Spin Control Register (A.C. 011)

Bit	Name	POR Initial Value
7	NC	0
6	LINEAR/PWM	0
5	INCREMENT STATE	0
4	RESET STATE	0
3	RUN/SEARCH	0
2	UNI/BI	0
1	HIGH GAIN SPIN	0
0	ENABLE Spin	0

Table 4: VCM D/A Register (A.C. 100)

Bit	Name	POR Initial Value
7	Most Significant Bit	0
6		0
5		0
4		0
3		0
2		0
1		0
0	Least Significant Bit	0

Table 5: Spin D/A Register (A.C. 101)

Bit	Name	POR Initial Value
7	Most Significant Bit	0
6		0
5		0
4		0
3		0
2		0
1		0
0	Least Significant Bit	0

Table 6: Interrupt Mask Register (A.C. 110)

Bit	Name	POR Initial Value
7	NC	
6	NC	
5	NC	
4	NC	
3	NC	
2	MASK REV Spin	0
1	MASK OVER TEMP ERROR	0
0	MASK OVER VEL ERROR	0

Table 7: Phase Delay Register (A.C. 111)

Bit	Name	POR Initial Value
7	NC	
6	NC	
5	NC	
4	NC	
3	Most Significant Bit	0
2		0
1		0
0	Least Significant Bit	0

SYSTEM BUS DESCRIPTION

The system bus is designed as a data acknowledge handshanking bus. At the beginning of the bus cycle the address and chip select are decoded transparently and qualified with read or write going low. On a read operation, data must not be driven for 5nsec after read goes low to allow the bus to clear. Once data is driven, data acknowledge is driven low to notify the processor that data is on the bus and ready to be read. The processor reads the data and responds by raising read. This is an indication that the processor has compleated the read and cycle is complete. Data acknowledge and data must go to high impedence within 20ns to clear the bus for the next

cycle. On a write operation, following write going low and whatever setup time required to latch data, data acknwledge is driven low. This notifies the processor that the cycle can end. This processor responds by raising write, indicating the end of the cycle. Data acknowledge must go to high impedance within 20nsec to clear the bus for the next cycle.

This handshaking design allows a peripheral to control the length of the bus cycle. The peripheral can take as much time as it needs to drive data onto the bus, then drive DTACK low. Likewise, the peripheral can wait as long as it needs to set up data and latch it (or set up data if WR is used to latch), then drive DTACK low. However, performance is an issue, so even though this control has been given to the peripheral, it must not be abused. All delays are minimized to assure optimum system speed, infact the bus can be driven synchronously (E.G. has regarding DTACK) when procesor clocks below 12MHz are used.

Figure 1: System Bus Timing (see Table 8)

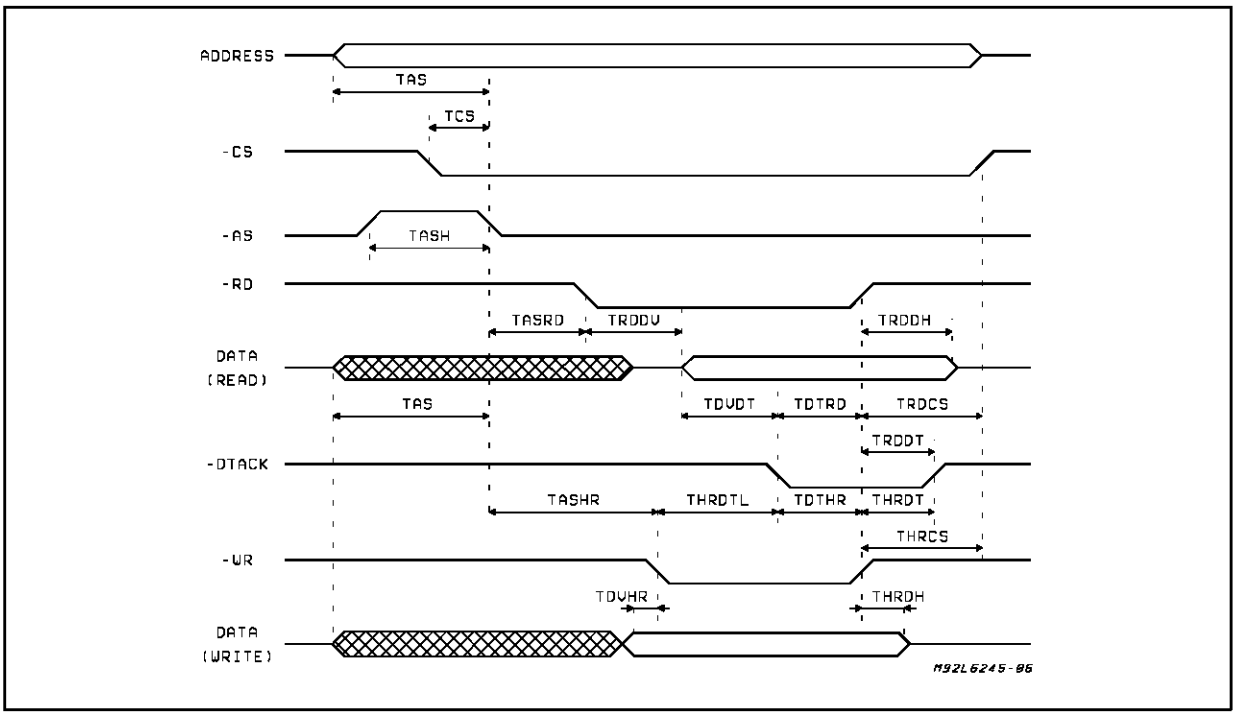


Table 8: System Bus Timing

Symbol	Description
TAS	Address Setup Time (non MUX bus; (MUX bus)
TCS	System Select to Address Strobe
TASW	Address Strobe Width
TASRD	Address Strobe to $\overline{RD}$
TRDDV	$\overline{RD}$ to Data Driven
TRDDH	Read Data Hold
TRDCS	RD High to CS High
TDVDT	Data Valid to $\overline{DTACK}$
TDTRD	$\overline{DTACK}$ to RD High
TRDDT	RD High to DTACH High
TASWR	Address Strobe to $\overline{WR}$
TDVWR	Write Data Valid to $\overline{WR}$
TWRDTL	$\overline{WR}$ to $\overline{DTACK}$
TDTWR	$\overline{DTACK}$ to WR High
TWRCS	WR High to CS High
TWRDT	WR High to DTACK High
TWRDH	Write Data Hold

THERMAL CHARACTERISTICS

On the application, the L6245 must be soldered on a PCB system. The Traks Area, depending on the lenght and the width of each track, must be between 2 to 10 square mm. An area of 10 mm^2 can give a typ. Thermal Resistance Junction-to-Ambient value of 85°C/W (See Fig. 2): this value refer3 to a Total Power Dissipated Power of 1W.

Figure 2: Typical $R_{th\ j\text{-}amb}$ vs. Tracks Area on PCB

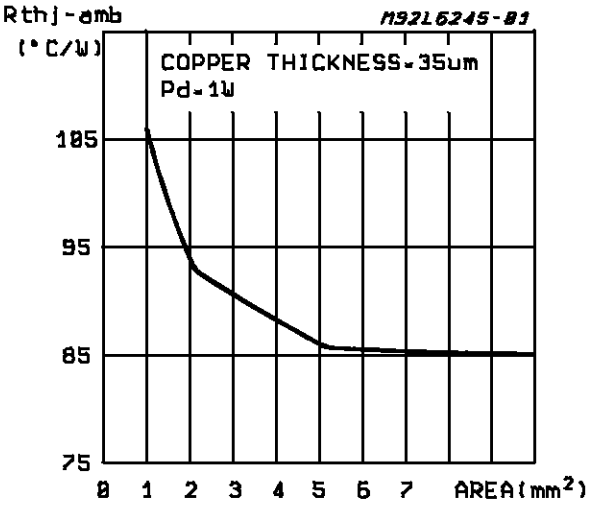


Fig. 9 shows the increase of the Rth j-amb when the Dissipated Power decreases.

Practically, very useful information is the change of the thermal resistance (Thermal Impedance) versus a single pulse of power width or versus the time the dissipation begins.

Fig. 4 shows this Thermal Impedance trend.

Figure 3: Typical Junction-to-Ambient Thermal Resistance vs. Total Dissipated Power. (L6245 mounted on a typical PCB)

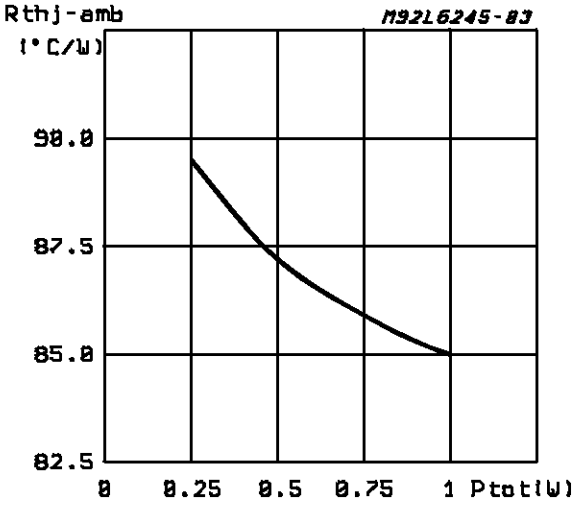
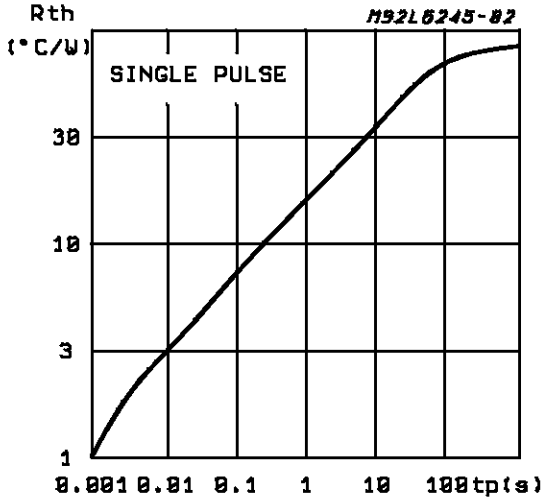
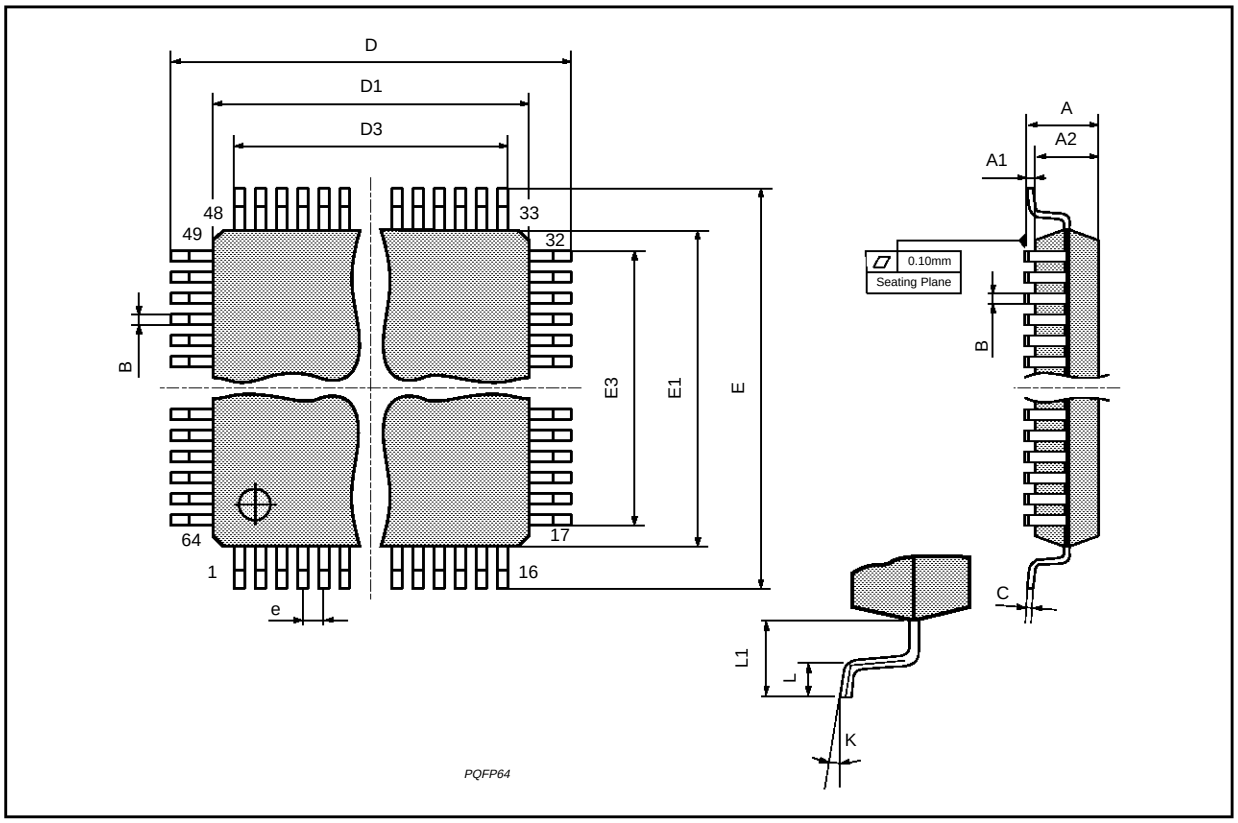


Figure 4: Typical Transient Thermal Impedance vs. Time or Pulse Width. (L6245 mounted on a typical PCB)



PQFP64 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.30		0.45	0.0118		0.0177
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		12.00			0.472	
e		0.80			0.0315	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
K	0°(min.), 7°(max.)					
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063	



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