



# LK115D00 SERIES

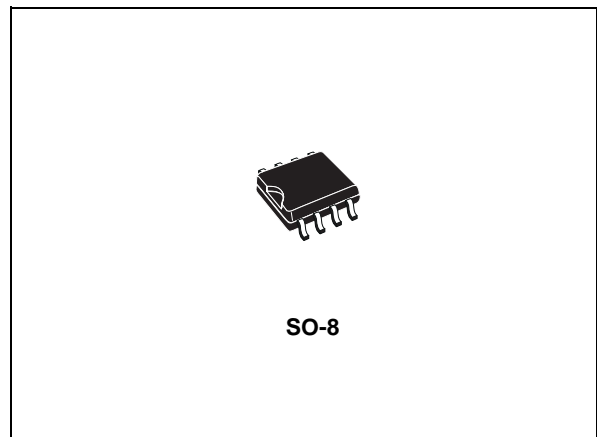
## VERY LOW DROP WITH INHIBIT VOLTAGE REGULATORS

- VERY LOW DROPOUT VOLTAGE (0.2 V TYP.)
- VERY LOW QUIESCENT CURRENT (TYP. 0.01 $\mu$ A IN OFF MODE, 280 $\mu$ A IN ON MODE)
- OUTPUT CURRENT UP TO 100mA
- TWO LOGIC-CONTROLLED ELECTRONIC SHUTDOWNS
- OUTPUT VOLTAGES OF 2; 2.5; 3.0; 3.3; 4; 4.75; 4.85; 5; 5.5 V
- INTERNAL CURRENT AND THERMAL LIMIT
- ONLY 2.2 $\mu$ F FOR STABILITY
- $V_{OUT}$  TOLLERANCE  $\pm 3\%$  AT 25°C
- SUPPLY VOLTAGE REJECTION: 80dB (TYP)
- TEMPERATURE RANGE: -40°C TO 125°C

### DESCRIPTION

The LK115D00 series are very Low Drop regulators available in SO-8 package and in a wide range of output voltages.

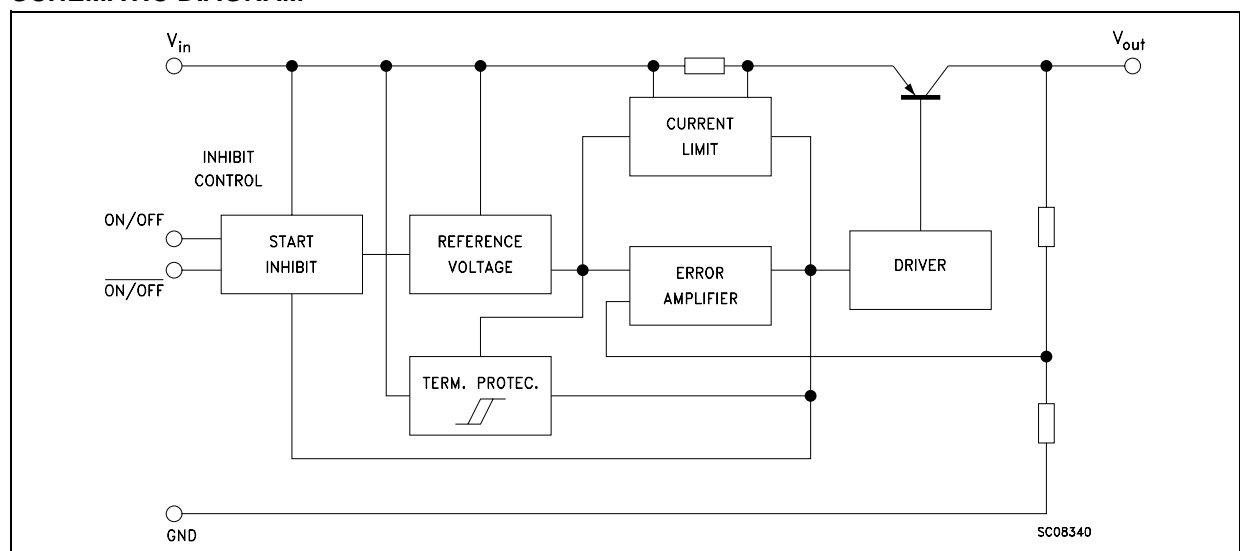
The very Low Drop voltage (0.2V) and the very low quiescent current (0.01 $\mu$ A in OFF MODE, 280 $\mu$ A in ON MODE) make them particularly



suitable for Low Noise, Low Power applications and specially in battery powered systems.

Both active HIGH and active LOW shutdown Logic Control are available (pin2 and 3). This means that when the device is used as a local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. It requires only a 2.2  $\mu$ F capacitor for stability allowing space and cost saving.

### SCHEMATIC DIAGRAM



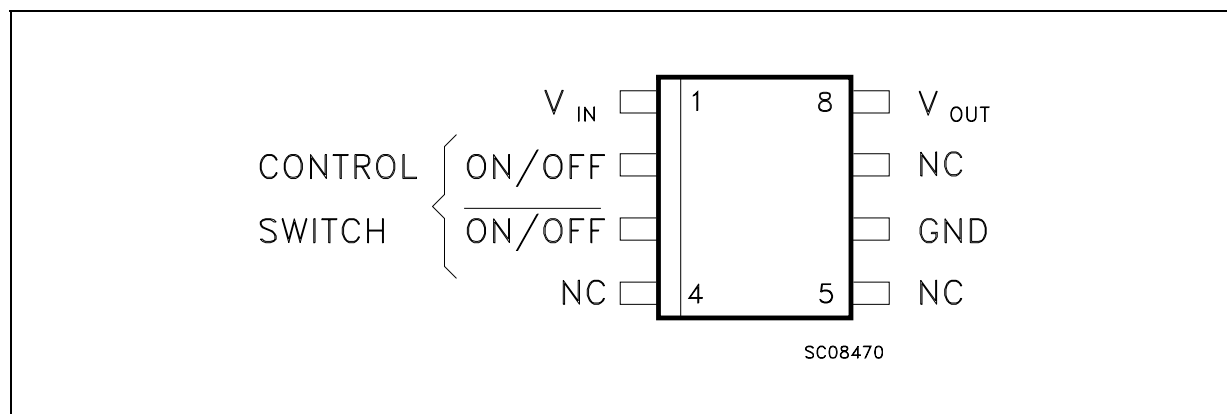
## LK115D00 SERIES

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_I$	DC Input Voltage	20	V
$I_O$	Output Current	Internally limited	
$P_{tot}$	Power Dissipation	Internally limited	
$T_{stg}$	Storage Temperature Range	-40 to 150	°C
$T_{op}$	Operating Junction Temperature Range	-40 to 125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

### CONNECTION DIAGRAM (top view)



### ORDERING CODES

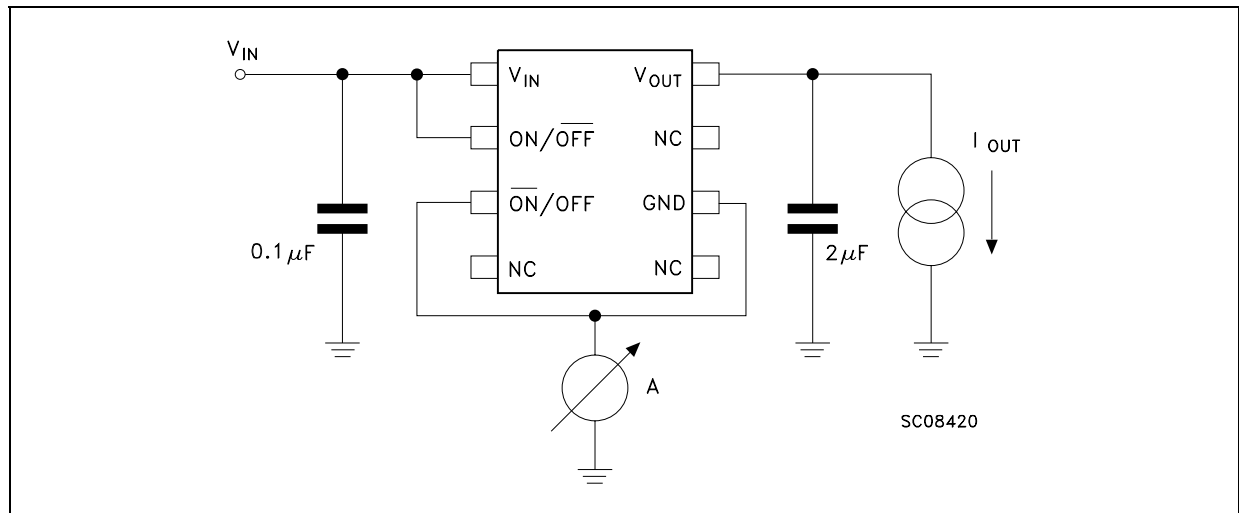
TYPE	OUTPUT VOLTAGE
LK115D20	2 V
LK115D25	2.5 V
LK115D30	3 V
LK115D33	3.3 V
LK115D40	4 V
LK115D47	4.75 V
LK115D48	4.85 V
LK115D50	5 V
LK115D55	5.5 V

### TRUTH TABLE

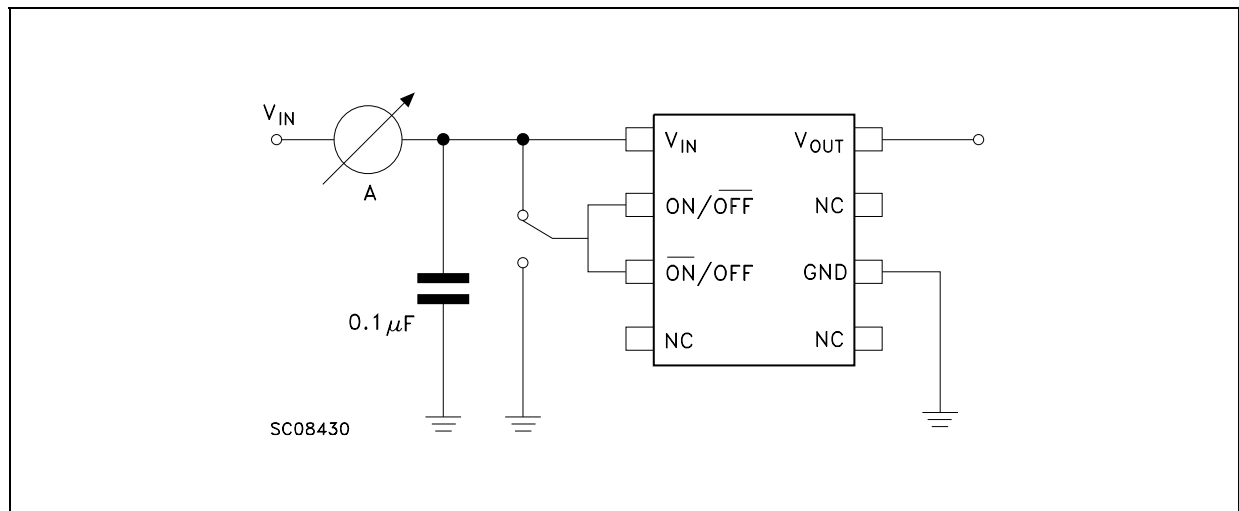
$\overline{\text{ON/OFF}}$ (PIN 2)	$\overline{\text{ON/OFF}}$ (PIN 3)	STATUS
H	L	ON
H	H	OFF
L	L	OFF
L	H	NOT ALLOWED

NOTES: Logic Levels are those defined in the electrical characteristics.

**TEST CIRCUITS: Supply Current (ON MODE)**



**TEST CIRCUITS: Supply Current (OFF MODE)**



NOTE: The switch emulates the two possibilities to set the regulator in OFF mode.

## LK115D00 SERIES

**ELECTRICAL CHARACTERISTICS FOR LK115D20** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 4\text{ V}$	1.940	2	2.060	V
		$I_O = 10\text{ mA}$ , $V_I = 4\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	1.9		2.1	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 3\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		2	10	mV
$\Delta V_O$	Load Regulation	$V_I = 3\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 3\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 3\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 3\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $f = 120\text{Hz}$		83		dB
		$V_I = 4\text{ V} \pm 1\text{ V}$ $f = 1\text{ KHz}$		78		
		$f = 10\text{ KHz}$		59		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		44		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

**ELECTRICAL CHARACTERISTICS FOR LK115D25** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 4.5\text{ V}$	2.425	2.5	2.575	V
		$I_O = 10\text{ mA}$ , $V_I = 4.5\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	2.375		2.625	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 3.5\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		2	10	mV
$\Delta V_O$	Load Regulation	$V_I = 3.5\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 3.5\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 3.5\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 3.5\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $f = 120\text{Hz}$		81		dB
		$V_I = 4.5\text{ V} \pm 1\text{ V}$ $f = 1\text{ KHz}$		76		
		$f = 10\text{ KHz}$		58		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		55		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

**ELECTRICAL CHARACTERISTICS FOR LK115D30** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 5\text{ V}$	2.910	3	3.090	V
		$I_O = 10\text{ mA}$ , $V_I = 5\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	2.850		3.150	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 4\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		2	10	mV
$\Delta V_O$	Load Regulation	$V_I = 4\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 4\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 4\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 4\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $V_I = 5\text{ V} \pm 1\text{ V}$	$f = 120\text{ Hz}$	79		dB
			$f = 1\text{ KHz}$	74		
			$f = 10\text{ KHz}$	57		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		66		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

**ELECTRICAL CHARACTERISTICS FOR LK115D33** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 5.3\text{ V}$	3.2	3.3	3.4	V
		$I_O = 10\text{ mA}$ , $V_I = 5.3\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	3.135		3.465	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 4.3\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		2	10	mV
$\Delta V_O$	Load Regulation	$V_I = 4.3\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 4.3\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 4.3\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 4.3\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $V_I = 5.3\text{ V} \pm 1\text{ V}$	$f = 120\text{ Hz}$	79		dB
			$f = 1\text{ KHz}$	74		
			$f = 10\text{ KHz}$	57		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		72.6		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

## LK115D00 SERIES

**ELECTRICAL CHARACTERISTICS FOR LK115D40** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 6\text{ V}$	3.880	4	4.120	V
		$I_O = 10\text{ mA}$ , $V_I = 6\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	3.8		4.2	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 5\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		3	15	mV
$\Delta V_O$	Load Regulation	$V_I = 5\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 5\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 5\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 5\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $V_I = 5\text{ V} \pm 1\text{ V}$	$f = 120\text{ Hz}$	77		dB
			$f = 1\text{ KHz}$	72		
			$f = 10\text{ KHz}$	56		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		88		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

**ELECTRICAL CHARACTERISTICS FOR LK115D47** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 6.8\text{ V}$	4.607	4.75	4.892	V
		$I_O = 10\text{ mA}$ , $V_I = 6.8\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	4.513		4.987	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 5.8\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		3	15	mV
$\Delta V_O$	Load Regulation	$V_I = 5.8\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 5.8\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 5.8\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 5.8\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $V_I = 6.8\text{ V} \pm 1\text{ V}$	$f = 120\text{ Hz}$	75		dB
			$f = 1\text{ KHz}$	70		
			$f = 10\text{ KHz}$	55		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		104.5		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

**ELECTRICAL CHARACTERISTICS FOR LK115D48** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 6.9\text{ V}$	4.705	4.85	4.966	V
		$I_O = 10\text{ mA}$ , $V_I = 6.9\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	4.607		5.093	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 5.9\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		3	15	mV
$\Delta V_O$	Load Regulation	$V_I = 5.9\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 5.9\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 5.9\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 5.9\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $f = 120\text{Hz}$		75		dB
		$V_I = 6.9\text{ V} \pm 1\text{ V}$ $f = 1\text{ KHz}$		70		
		$f = 10\text{ KHz}$		55		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		106.7		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

**ELECTRICAL CHARACTERISTICS FOR LK115D50** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 7\text{ V}$	4.85	5	5.15	V
		$I_O = 10\text{ mA}$ , $V_I = 7\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	4.75		5.25	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 6\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		3	15	mV
$\Delta V_O$	Load Regulation	$V_I = 6\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 6\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 6\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 6\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $f = 120\text{Hz}$		75		dB
		$V_I = 7\text{ V} \pm 1\text{ V}$ $f = 1\text{ KHz}$		70		
		$f = 10\text{ KHz}$		55		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		110		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Llc}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

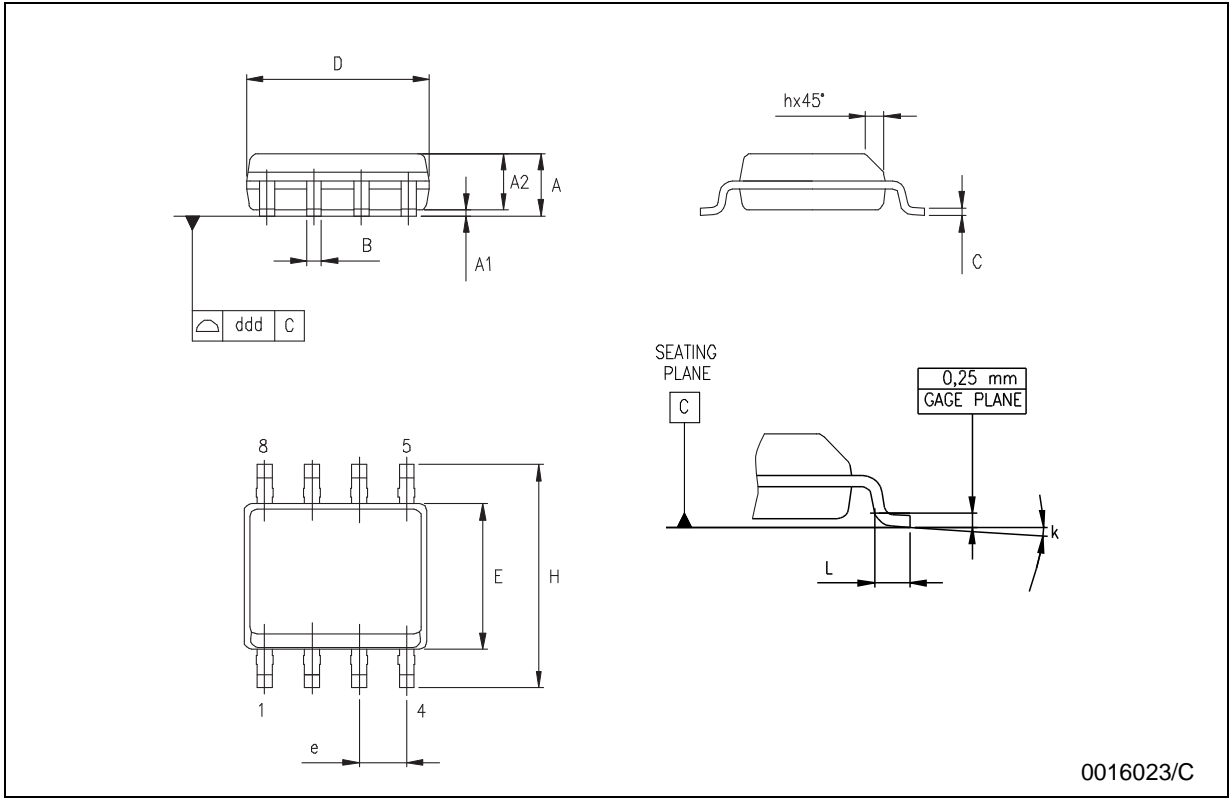
## LK115D00 SERIES

**ELECTRICAL CHARACTERISTICS FOR LK115D55** (refer to the test circuits,  $T_J = 25^\circ\text{C}$ ,  $C_I = 0.1\mu\text{F}$ ,  $C_O = 2.2\mu\text{F}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$I_O = 10\text{ mA}$ , $V_I = 7.5\text{ V}$	5.335	5.5	5.665	V
		$I_O = 10\text{ mA}$ , $V_I = 7.5\text{ V}$ , $T_a = -40\text{ to }125^\circ\text{C}$	5.225		5.775	
$V_I$	Operating Input Voltage	$I_O = 100\text{ mA}$			20	V
$I_{out}$	Output Current Limit		120	200		mA
$\Delta V_O$	Line Regulation	$V_I = 6.5\text{ to }20\text{ V}$ $I_O = 0.5\text{ mA}$		3	15	mV
$\Delta V_O$	Load Regulation	$V_I = 6.5\text{ V}$ $I_O = 0.5\text{ to }100\text{ mA}$		4	20	mV
$I_d$	Quiescent Current (On Mode)	$V_I = 6.5\text{ to }20\text{ V}$ $I_O = 0$		0.28	0.5	mA
		$V_I = 6.5\text{ to }20\text{ V}$ $I_O = 100\text{ mA}$		1.5	3	
	(Off Mode)	$V_I = 6.5\text{ to }20\text{ V}$		0.01	2	$\mu\text{A}$
SVR	Supply Voltage Rejection	$I_O = 5\text{ mA}$ $f = 120\text{ Hz}$		74		dB
		$V_I = 7.5\text{ V} \pm 1\text{ V}$ $f = 1\text{ KHz}$		69		
		$f = 10\text{ KHz}$		55		
eN	Output Noise Voltage (RMS)	$B = 10\text{ Hz to }100\text{ KHz}$		121		$\mu\text{V}$
$V_d$	Dropout Voltage	$I_O = 60\text{ mA}$		0.17		V
$V_{Hic}$	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		$V_{in}$	
$V_{Lic}$	ON/OFF Control (pin 3)	Pin 2 to $V_{in}$ OFF	$V_{in}-0.2$		$V_{in}$	V
		Pin 2 to $V_{in}$ ON	0		$V_{in}-2.4$	
$C_O$	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\ \Omega$ , $I_O = 0\text{ to }100\text{ mA}$	2	10		$\mu\text{F}$

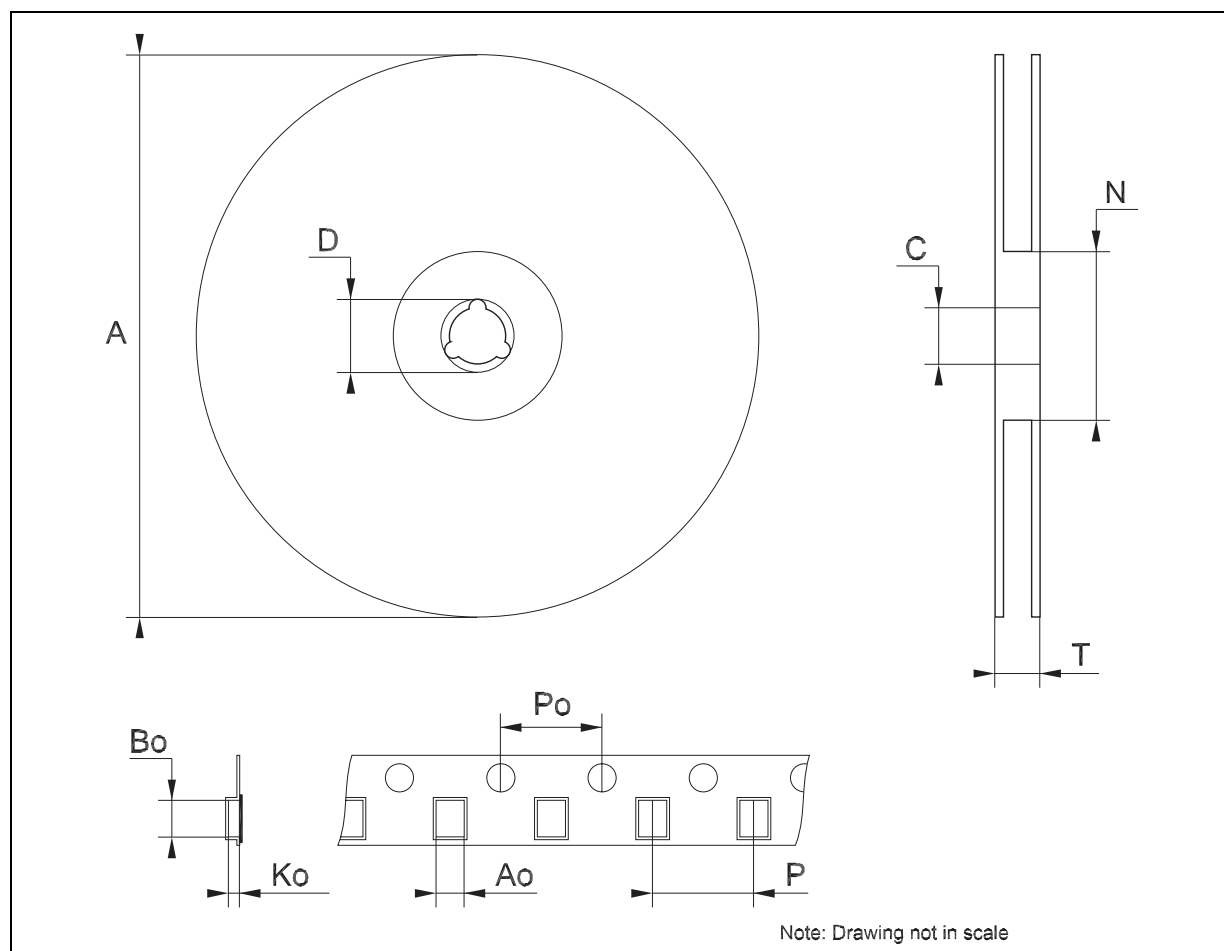
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



**Tape & Reel SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



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