



M25P10

1 Mbit Low Voltage Paged Flash Memory With 20 MHz Serial SPI Bus Interface

PRELIMINARY DATA

- 1 Mbit PAGED Flash Memory
- 128 BYTE PAGE PROGRAM IN 3 ms TYPICAL
- 256 Kbit SECTOR ERASE IN 1 s TYPICAL
- BULK ERASE IN 2 s TYPICAL
- SINGLE 2.7 V to 3.6 V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 20 MHz CLOCK RATE AVAILABLE
- SUPPORTS POSITIVE CLOCK SPI MODES
- DEEP POWER DOWN MODE (1 μ A TYPICAL)
- ELECTRONIC SIGNATURE
- 10,000 ERASE/PROG CYCLES PER SECTOR
- 20 YEARS DATA RETENTION
- -40 TO 85°C TEMPERATURE RANGE

DESCRIPTION

The M25P10 is an 1 Mbit Paged Flash Memory fabricated with STMicroelectronics High Endurance CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

The device connected to the bus is selected when the chip select input (\bar{S}) goes low. Data is clocked in during the low to high transition of clock C, data

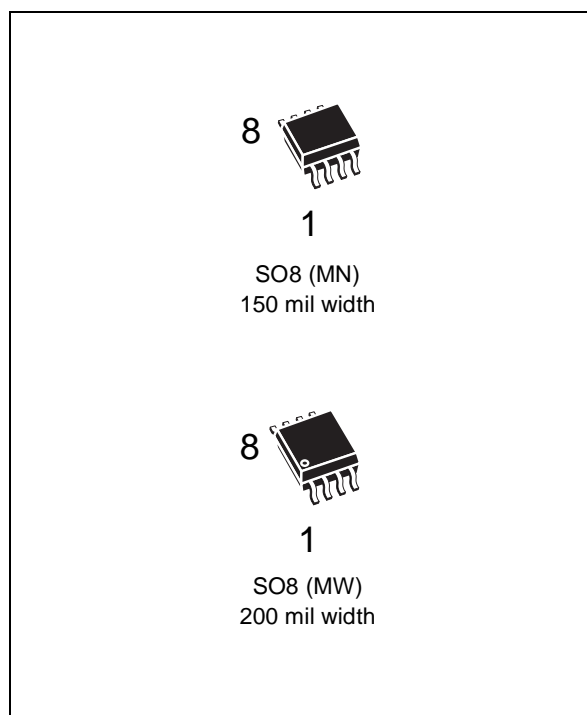


Figure 1. Logic Diagram

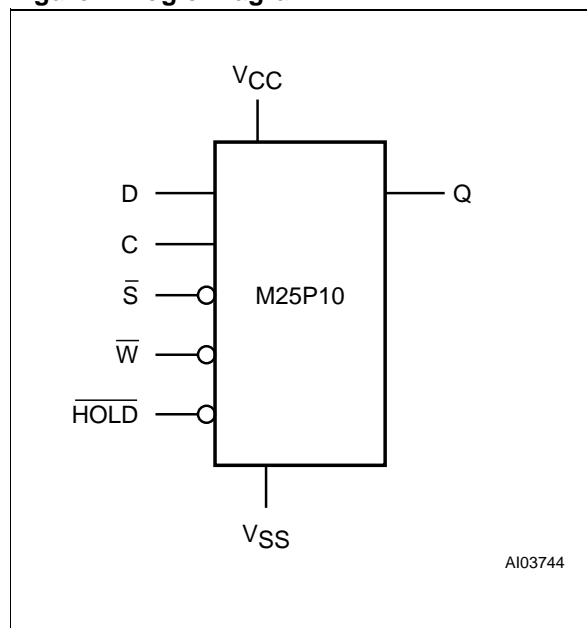
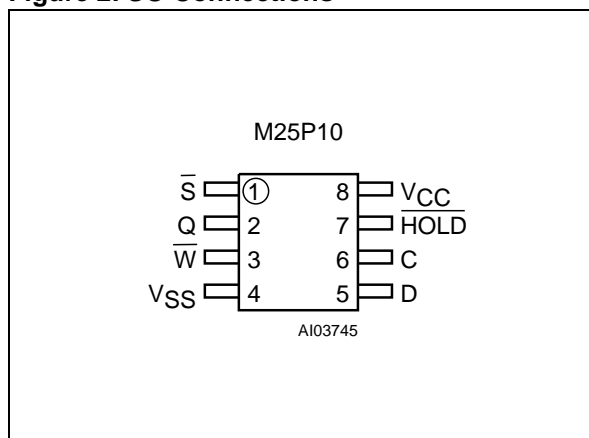


Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
\bar{S}	Chip Select
\bar{W}	Write Protect
$\overline{\text{HOLD}}$	Hold
V _{CC}	Supply Voltage
V _{SS}	Ground

Figure 2. SO Connections



is clocked out during the high to low transition of clock C

SIGNALS DESCRIPTION

Serial Output (Q)

The output pin is used to transfer data serially out of the memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D)

The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Input is latched on the rising edge of the serial clock.

Serial Clock (C)

The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select (\bar{S})

When \bar{S} is high, the memory is deselected and the Q output pin is at high impedance and, unless an internal Read, Program, Erase or Write Status Register operation is underway, the device will be in the Standby Power mode (this is not the Deep Power Down mode). \bar{S} low enables the memory, placing it in the active power mode. It should be noted that after power-on, a high to low transition on \bar{S} is required prior to the start of any operation.

Hold ($\overline{\text{HOLD}}$)

The HOLD pin is used to pause serial communications with a SPI memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected. The HOLD condition is validated by a 0 state on the Hold pin synchronized with the 0 state on the Clock, as shown in Figure 4. The DeHOLD condition is validated by a 1 state on the Hold pin synchronized with the 0 state on the Clock. During the Hold condition D, Q, and C are at a high impedance state.

When the memory is under HOLD condition, it is possible to deselect the device. Then, the protocol is reset. The memory remains on HOLD as long as the Hold pin is Low. To restart communication with the device, it is necessary to both DeHOLD (H = 1) and to SELECT the memory.

Write Protect (\bar{W})

This pin is for hardware write protection of the Status Register (SR); except WIP and WEL bits. When bit 7 (SRWD) of the status register is 0 (the initial delivery state); it is possible to write the SR once the WEL (Write Enable Latch) has been set with the WREN instruction and whatever is the status of pin \bar{W} (high or low).

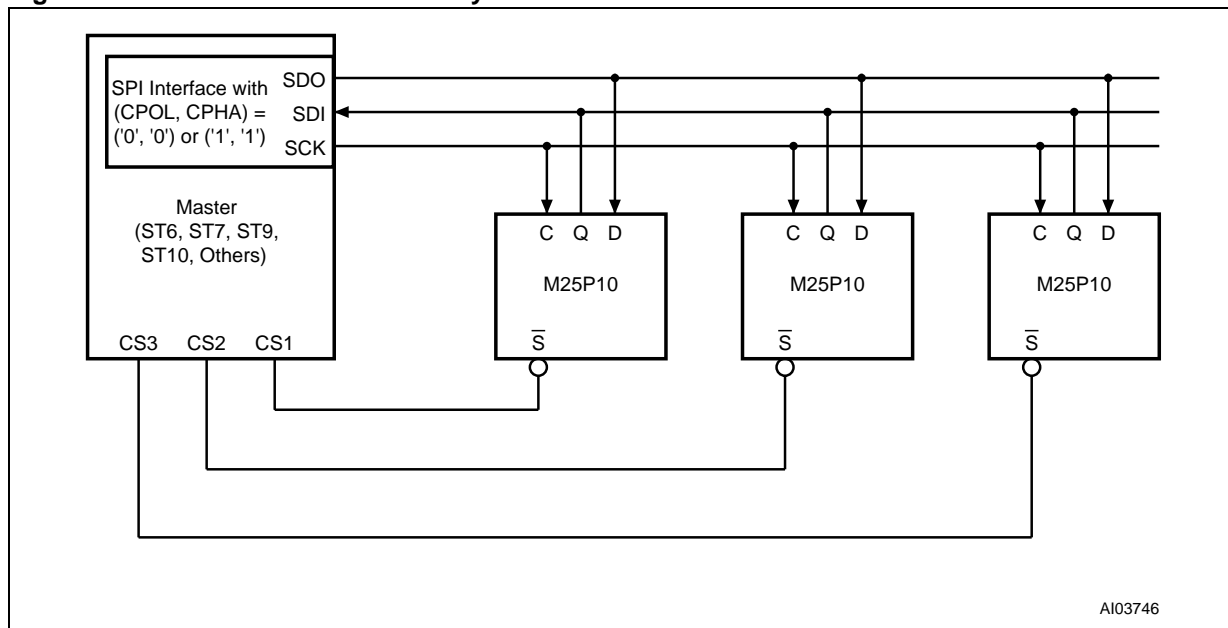
Table 2. Absolute Maximum Ratings ¹

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	-40 to 85	°C
T _{STG}	Storage Temperature	-65 to 150	°C
T _{LEAD}	Lead Temperature during Soldering SO8: 40 seconds	215	°C
V _{IO}	Input and Output Voltage Range (with respect to Ground)	-0.3 to 5.0	V
V _{CC}	Supply Voltage Range	-0.6 to 5.0	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ²	2000	V

Note: 1. Except for the rating "Ambient Operating Temperature Range", stresses above those listed in this table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.

2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

Figure 3. Microcontroller and Memory Devices on the SPI Bus



Once bit 7 (SRWD) of the status register has been set to 1, the possibility to rewrite the SR depends on the logical level present at pin \overline{W} :

- If \overline{W} pin is high, it will be possible to rewrite the status register after having set the WEL (Write Enable Latch).
- If \overline{W} pin is low, any attempt to modify the status register will be ignored by the device even if the WEL was set. As a consequence: all the data bytes in the memory area software protected (SPM) by the BPi bits of the status register are also hardware protected against data modification and can be seen as a Read Only memory area. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) by setting SRWD bit after pulling down the \overline{W} pin or by pulling down the \overline{W} pin after setting SRWD bit.

The only way to abort the Hardware Protected Mode once entered is to pull high the \overline{W} pin.

If \overline{W} pin is permanently tied to high level, the Hardware Protected Mode will never be activated and the memory will only allow the user to software protect a part of the memory with the BPi bits of the status register.

All protection features of the device are summarized in Table 3.

Figure 4. Hold Condition Activation

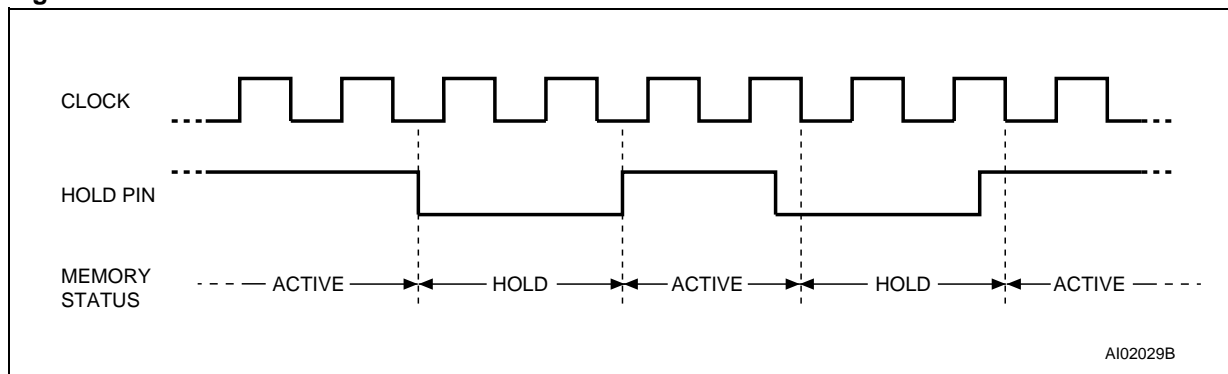
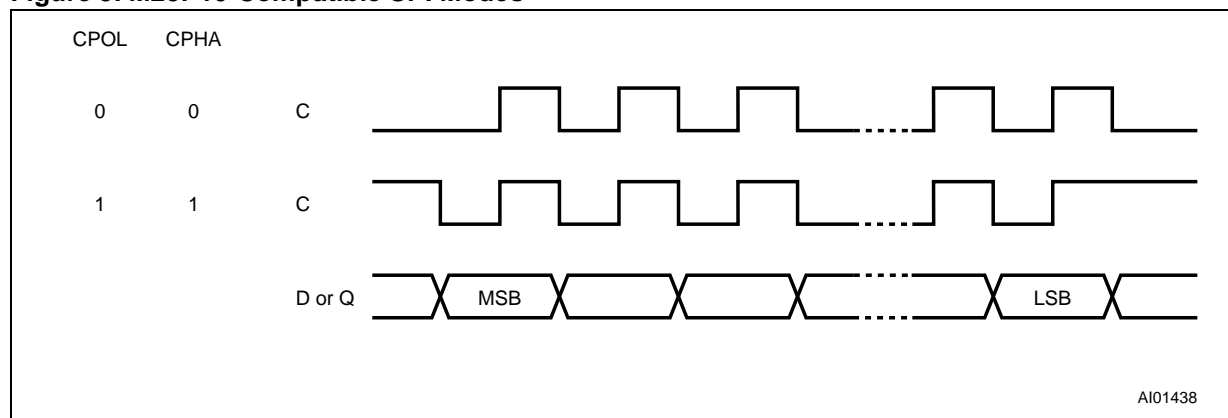


Figure 5. M25P10-Compatible SPI Modes



Clock Polarity (CPOL) and Clock Phase (CPHA) with SPI Bus

As shown in Figure 5, the M25P10 can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1'). For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C). The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the clock polarity when in stand-by: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

MEMORY ORGANIZATION

The memory is organized in 131,072 words of 8 bits each. The device features 1,024 pages of 128 bytes each. Each page can be individually programmed (bits are programmed from '1' to '0' state).

The device is also organized in 4 sectors of 262,144 bits (32,768 x 8 bits) each. The device is Sector or Bulk Erasable but not Page Erasable (bits are erased from '0' to '1' state).

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select (\bar{S}) goes low. Prior to any

Table 4. Memory Organization

Sector	Address Range	
3	18000h	1FFFFh
2	10000h	17FFFh
1	08000h	0FFFFh
0	00000h	07FFFh

Table 3. Protection Features

\bar{W}	SRWD	Status Register (SR)	Data Bytes (Software Protected Area by BPi bits)	Mode	Data Bytes (Unprotected Area)
X	0	Writeable after setting WEL	Software protected by the BPi bits of the Status Register	SPM	Paged Programmable and Sector Erasable
1	1	Writeable after setting WEL	Software protected by the BPi bits of the Status Register	SPM	Paged Programmable and Sector Erasable
0	1	Hardware protected	Hardware protected by the BPi bits of the Status Register and the \bar{W} pin	HPM	Paged Programmable and Sector Erasable

Note: 1. SPM: Software Protected Mode.

2. HPM: Hardware Protected Mode.

3. BPi: Bits BP0 and BP1 of the Status Register.

4. WEL: Write Enable Latch of the Status Register.

5. \bar{W} : Write Protect Input Pin.

6. SRWD: Status Register Write Disable Bits of the Status Register.

7. The device is Bulk Erasable if, and only if, (BP0, BP1) = (0, 0), (see Bulk Erase paragraph).

Figure 6. Block Diagram

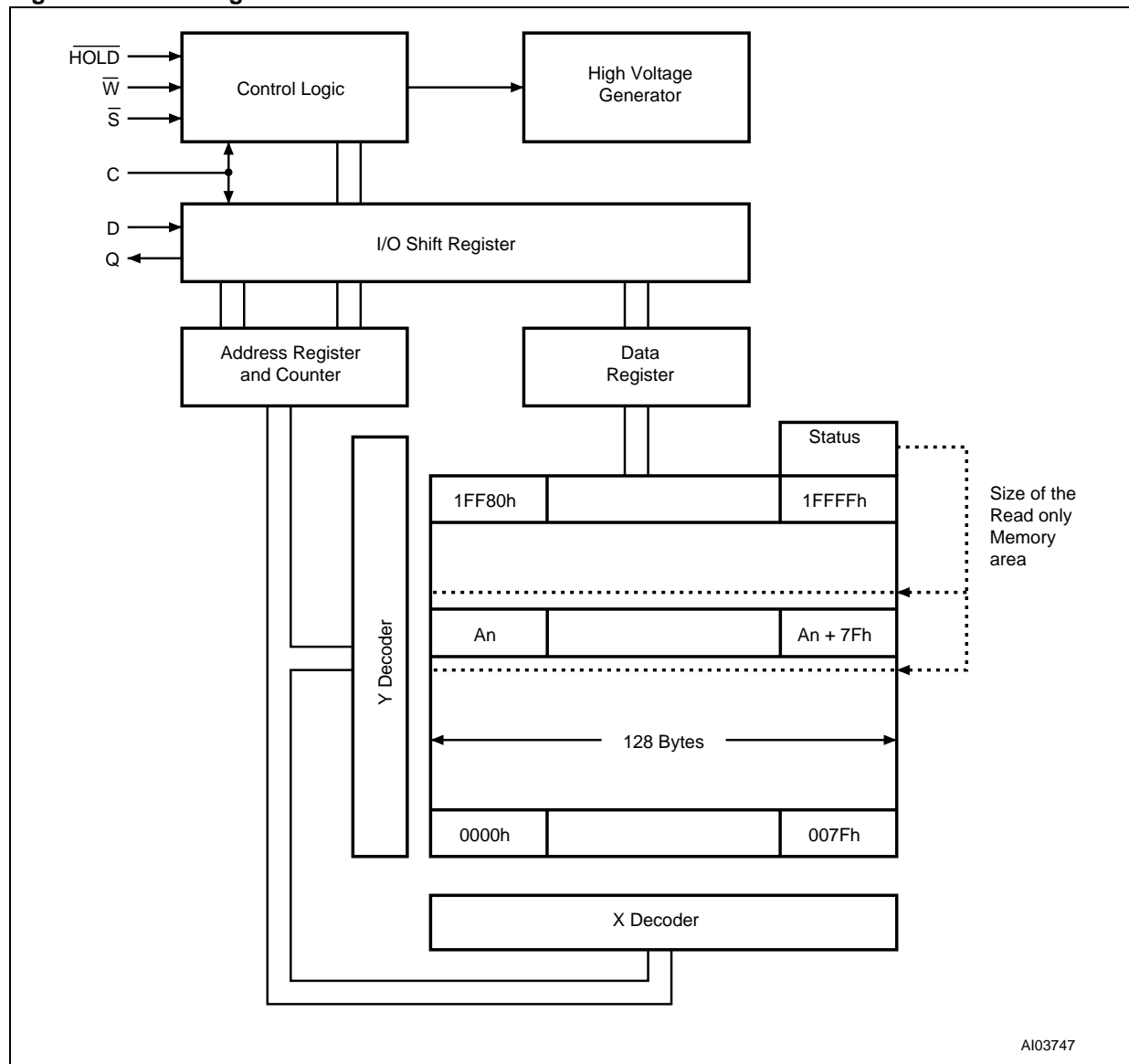


Table 5. Protected Area Sizes

BP1	BP0	Software Protected Area
0	0	none
0	1	Upper quarter = Sector 3
1	0	Upper half = Sectors 2 & 3
1	1	Whole memory= Sectors 0, 1, 2 & 3

Table 6. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
PP	Program up to 128 Data bytes to Memory Array	0000 0010
SE	Sector Erase (set to FFh) one sector of Memory Array	1101 1000
BE	Bulk Erase (set to FFh) whole of Memory Array	1100 0111
DP	Enter Deep Power-down mode	1011 1001
RES	Release from Deep Power-down mode, and Read Electronic Signature	1010 1011

operation, a one-byte instruction code must be sent to the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the device must have been previously selected (\overline{S} = low). Table 6 shows the available instruction set.

At Power-up and Power-down, the device must not be selected (that is the \overline{S} input must follow the voltage applied on the V_{CC} pin) until the supply voltage reaches the correct V_{CC} values which are $V_{CC}(\text{min})$ at Power-up and V_{SS} at Power-down (a simple pull-up resistor on \overline{S} insures safe and proper power up and down phases).

Read Data Byte(s) (READ)

The device is first selected by putting \overline{S} low. The Read instruction byte is followed by a three bytes address (A23-A0), each bit being latched-in during the rising edge of the clock (C). Then the data stored in the memory at the selected byte address is shifted out on the Q output pin, each bit being shifted out during the falling edge of the clock (C).

The first byte addressed can be any byte within a page. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can therefore be read with a single Read instruction. When the highest address is reached, the address counter rolls over to 000000h allowing the read cycle to be continued indefinitely.

The Read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during an Erase, Program or Write Status Register cycle will be rejected and will deselect the chip without having any effects on the ongoing operation.

The timing sequence is shown in Figure 11.

Page Program (PP)

Prior to any Page Program attempt, a write enable instruction (WREN) must have been previously sent (the \overline{S} input driven low, WREN instruction properly transmitted and the \overline{S} input driven high). After the WREN instruction decoding, the memory sets the Write Enable Latch (WEL) which allows the execution of any further Page Program instruction. The Page Program instruction is entered by driving the Chip select input (\overline{S}) low, followed by the instruction byte, 3 address bytes and at least 1 data byte on Data In input (D). If the least significant address bits differ from [A6-A0]=000.0000, all transmitted data exceeding the addressed page boundary will roll over and will be programmed from address [A6-A0]=000.0000 of this same page. The Chip Select input (\overline{S}) must be driven low for the entire duration of the sequence.

Figure 7. WREN: Set Write Enable Latch Sequence

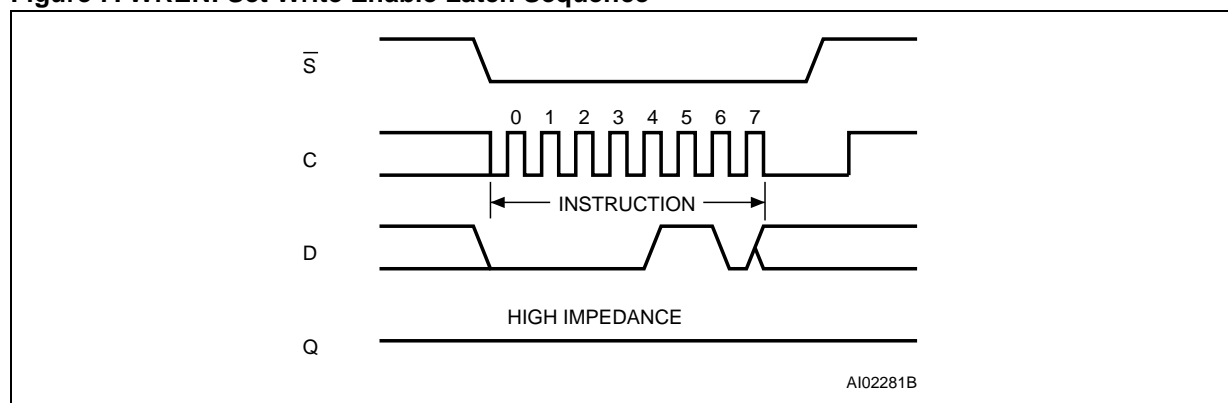
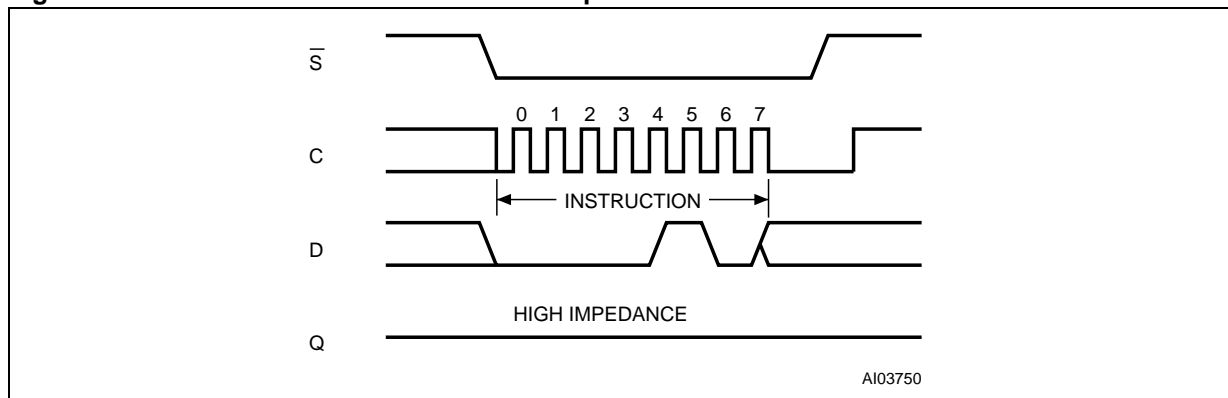


Figure 8. WRDI: Reset Write Enable Latch Sequence

If more than 128 bytes are sent to the device, previously latched data are discarded and the last 128 data bytes are guaranteed to be programmed correctly within the same page. If less than 128 Data bytes are sent to device; they are correctly programmed at the requested addresses without having any effects on the other bytes of the same Page.

The device must be deselected just after the eighth bit of the last data byte has been latched in. If not, the Page Program instruction is not executed. As soon as the device is deselected, the self-timed Page Program cycle (t_{pp}) is initiated. While the Page Program cycle is in progress, the status register may be read to check the WIP bit value. WIP is high during the self-timed Page Program cycle and is low when it is completed. When the cycle is completed, the write enable latch (WEL) is reset.

A Page Program instruction applied to a Page which is software protected by the BPI bits (see Table 4 and Table 5) is not initiated.

The timing sequence is shown in Figure 12.

Write Enable (WREN) and Write Disable (WRDI)

The Write Enable Latch must be set prior to every Page Program (PP), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) operation. The WREN instruction, whose timing sequence is shown in Figure 7, will set the latch and the WRDI instruction, whose timing sequence is shown in Figure 8, will reset the latch.

The Write Enable Latch is reset under the following conditions:

- Power on
- WRDI instruction completion
- WRSR instruction completion
- Page Program instruction completion
- Sector Erase instruction completion
- Bulk Erase instruction completion.

After completion of either WREN or WRDI instruction, the chip enters a wait state and waits for a deselect.

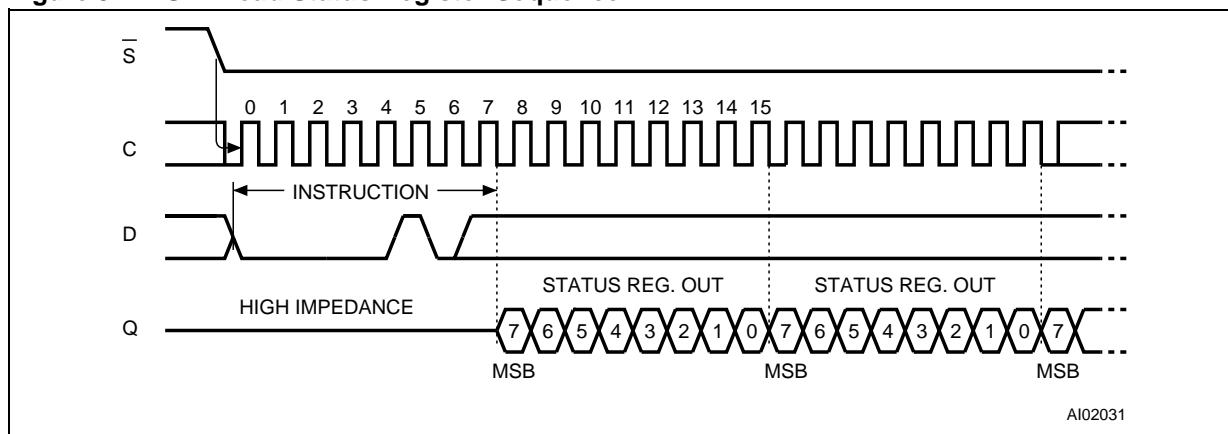
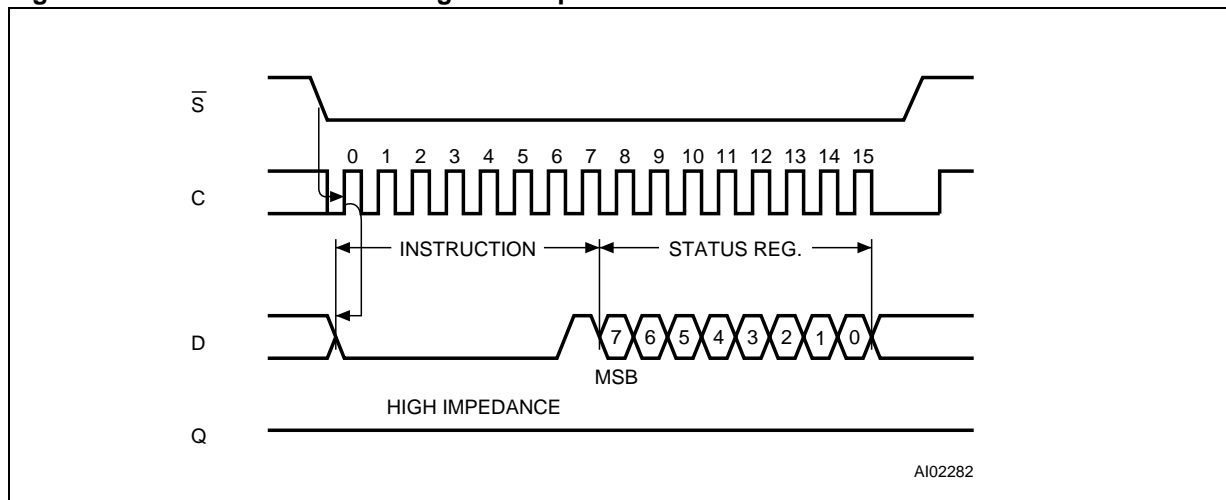
Figure 9. RDSR: Read Status Register Sequence

Figure 10. WRSR: Write Status Register Sequence

**Read Status Register (RDSR)**

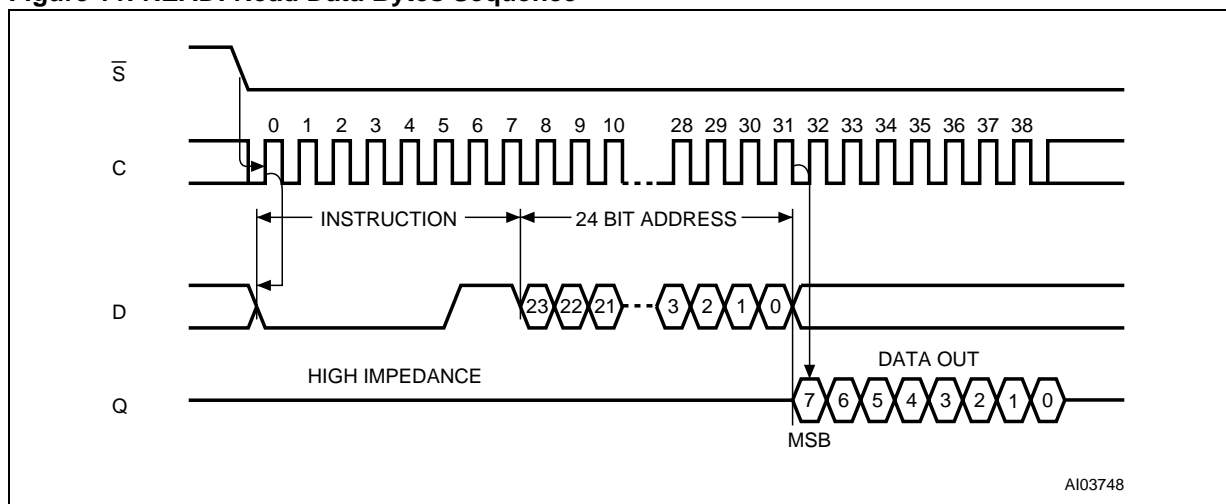
The RDSR instruction provides access to the Status Register content. The Status Register may be read at any time, even during a Page Program, Sector Erase, Bulk Erase or Write Status Register. When one of these instructions is in progress, it is recommended to check the WIP bit before sending a new instruction to the device. For this, it is possible to continuously read the Status Register value.

WIP bit: The Write-In-Process (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase operation. When set to a '1', such an operation is in progress, when set to a '0' no such operation is in progress.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to a '1' the latch is set, when set to a '0' the latch is reset and no Write Status Register, Program or Erase sequence will be allowed.

BP1, BP0 bits: The Block Protect bits BPi are non-volatile bits. They define the size of the area to be software protected against Program and Erase operations. These bits are written with the WRSR instruction (see Table 5). Once (BP0, BP1) are set to a value different from (0,0), the relevant area becomes protected against Page Program and Sector Erase operations. BPi bits can be written provided that the Hardware Protected Mode has not been set. The Bulk Erase instruction is

Figure 11. READ: Read Data Bytes Sequence



Note: 1. Address bits A23 to A17 are Don't Care on the M25P10 series.

Table 7. Status Register Format

b7				b0			
SRWD	0	0	0	BP1	BP0	WEL	WIP

Note: 1. SRWD, BP0 and BP1 are non-volatile read and write bits.
 2. WEL and WIP are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).

internally taken into account if, and only if, (BP0, BP1) = (0,0).

SRWD bit: The SRWD bit operates together with the \overline{W} pin. SRWD bit and \overline{W} pin allow the part to be put in the Hardware protected mode. In this mode (\overline{W} pin = 0 and SRWD = 1), the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read only bits and the Write Status Register (WRSR) instruction has no more effect on the device (please see the section entitled "Write Protect (W)" on page 2, and Table 3).

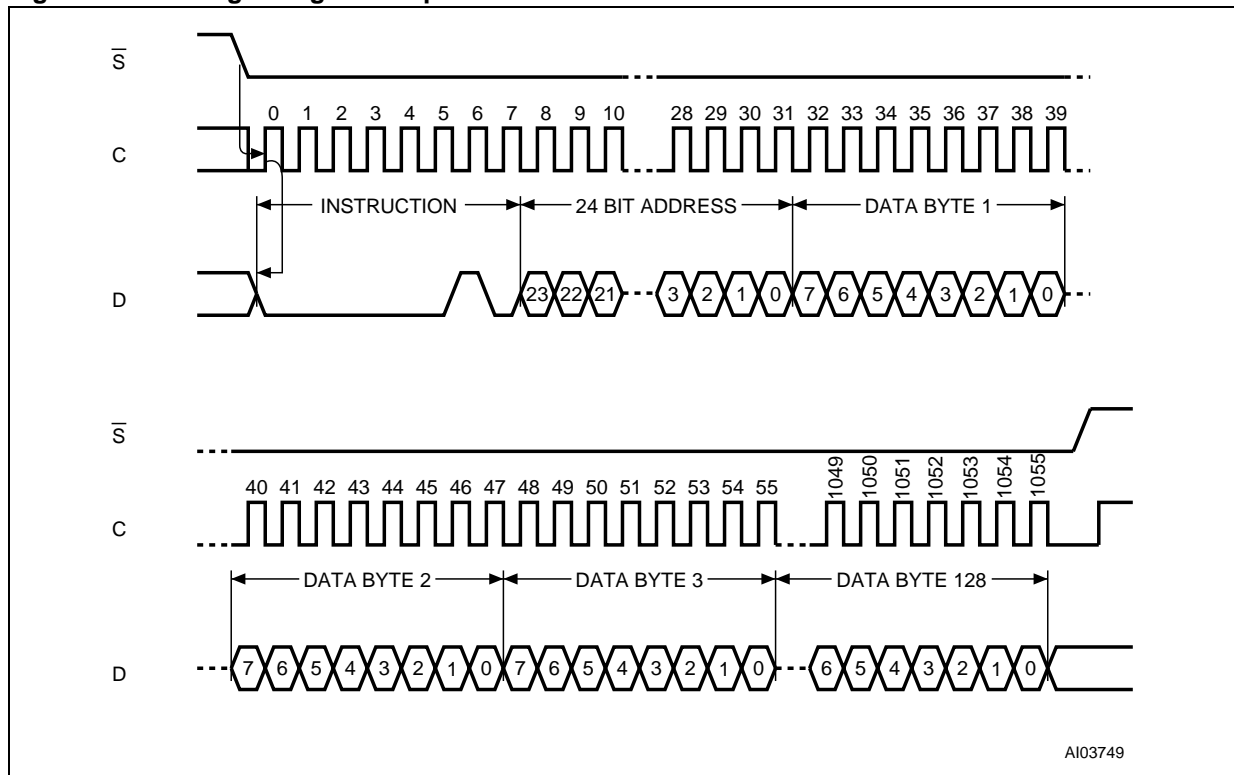
Write in the Status Register (WRSR)

Prior to any WRSR instruction, a write enable instruction (WREN) must have been previously sent (the \overline{S} input driven low, WREN instruction properly transmitted and the \overline{S} input driven high). After the WREN instruction decoding, the memory sets the Write Enable Latch (WEL) which allows

the execution of any further WRSR instruction. The WRSR instruction is entered by driving the Chip select input (\overline{S}) low, followed by the instruction byte and the data byte on Data In input (D). WRSR instruction has no effect on b6, b5, b4, b1 and b0 of the Status Register. b6, b5 and b4 are always read at '0'.

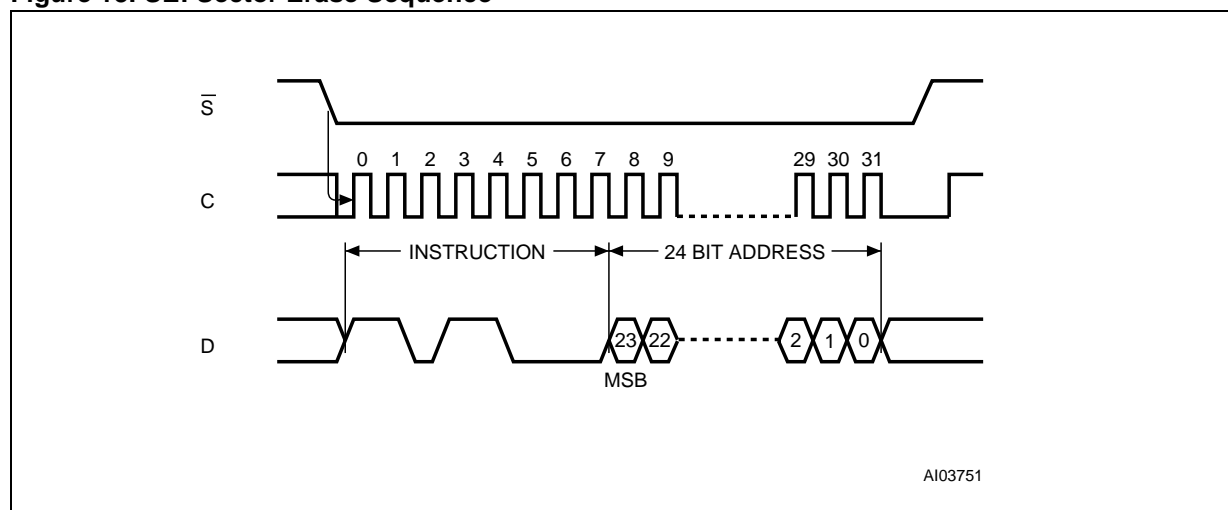
The device must be deselected just after the eighth bit of the data byte has been latched in. If not, the WRSR instruction is not executed. As soon as the device is deselected, the self-timed Write Status Register cycle (t_{WS}) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the WIP bit value. WIP is high during the self-timed Write Status Register cycle and is low when it is completed. When the cycle is completed, the write enable latch (WEL) is reset.

The WRSR instruction allows the user to define the size of the software Protected area (Read Only) when setting the BP1, BP0 values, according to Table 4. The WRSR instruction also allows the user to set or reset the SRWD bit in accordance with the \overline{W} pin. SRWD bit and \overline{W} pin allow the part to be put in the Hardware protected mode (please see the sections entitled "Read Status Register (RDSR)" on page 8, "Write Protect (W)" on page 2, and Table 3). WRSR instruction has no effect on

Figure 12. PP: Page Program Sequence

Note: 1. Address bits A23 to A17 are Don't Care on the M25P10 series.

Figure 13. SE: Sector Erase Sequence



Note: 1. Address bits A23 to A17 are Don't Care on the M25P10 series.

the device once the Hardware Protected Mode is entered.

The timing sequence is shown in Figure 10.

Sector Erase (SE)

Prior to any Sector Erase attempt, a write enable instruction (WREN) must have been previously sent (the \overline{S} input driven low, WREN instruction properly transmitted and the \overline{S} input driven high). After the WREN instruction decoding, the memory sets the Write Enable Latch (WEL) which allows the execution of any further Sector Erase. The Sector Erase instruction is entered by driving the Chip select input (\overline{S}) low, followed by the instruction byte and 3 address bytes on Data In input (D). Any address of the Sector (see Table 4) is a valid address for the Sector Erase instruction.

The Chip Select input (\overline{S}) must be driven low for the entire duration of the sequence. The device must be deselected just after the eighth bit of the

last address byte has been latched in. If not, the Sector Erase instruction is not executed. As soon as the device is deselected, the self-timed Sector Erase cycle (t_{SE}) is initiated. While the Sector Erase cycle is in progress, the status register may be read to check the WIP bit value. WIP is high during the self-timed Sector Erase cycle and is low when it is completed. When the cycle is completed, the write enable latch (WEL) is reset.

A Sector Erase instruction applied to a Sector which is software protected by the BPI bits (see Table 4 and Table 5) is not initiated.

The timing sequence is shown in Figure 13.

Bulk Erase (BE)

Prior to any Bulk Erase attempt, a write enable instruction (WREN) must have been previously sent (the \overline{S} input driven low, WREN instruction properly transmitted and the \overline{S} input driven high). After the WREN instruction decoding, the memory

Figure 14. BE: Bulk Erase Sequence

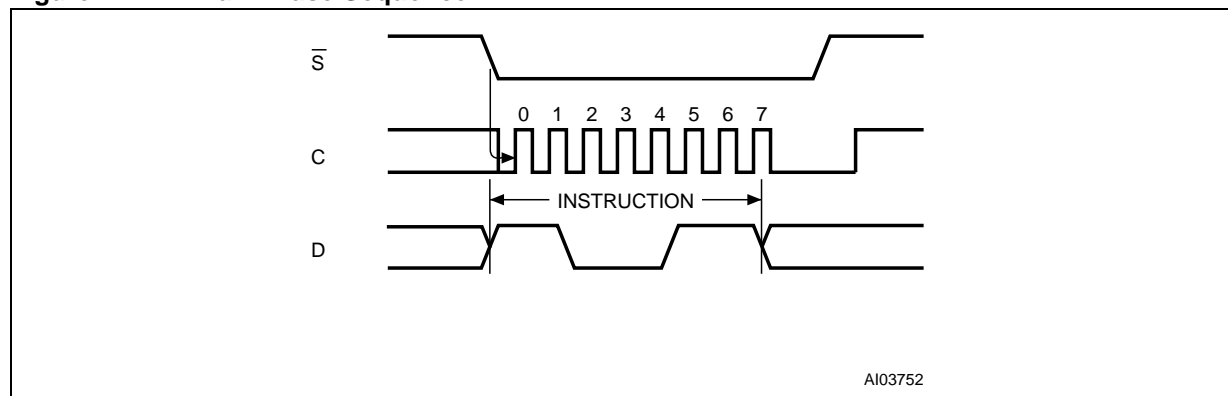
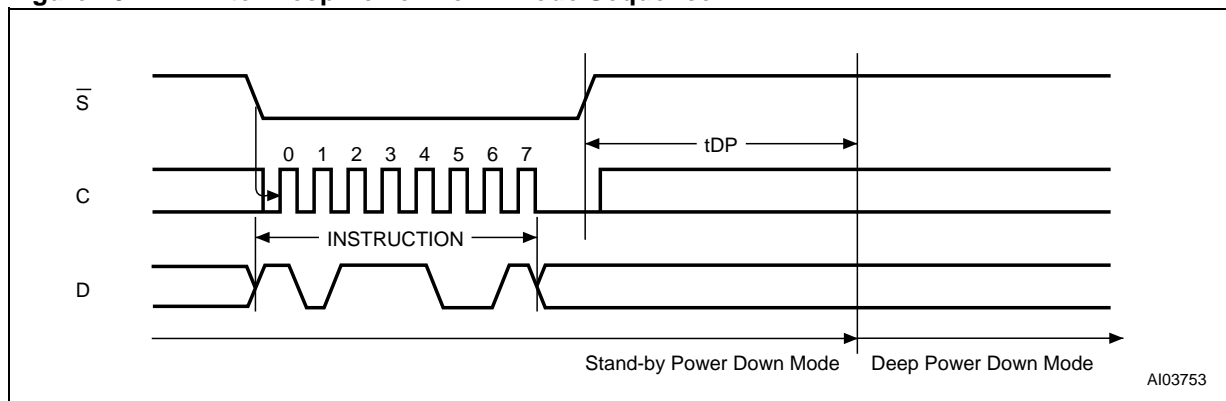


Figure 15. DP: Enter Deep Power Down Mode Sequence



sets the Write Enable Latch (WEL) which allows the execution of any further Bulk Erase. The Bulk Erase instruction is entered by driving the Chip select input (\bar{S}) low, followed by the instruction byte on Data In input (D).

The Chip Select input (\bar{S}) must be driven low for the entire duration of the sequence. The device must be deselected just after the eighth bit of the instruction byte has been latched in. If not, the Bulk Erase instruction is not executed. As soon as the device is deselected, the self-timed Bulk Erase cycle (t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the status register may be read to check the WIP bit value. WIP is high during the self-timed Bulk Erase cycle and is low when it is completed. When the cycle is completed, the write enable latch (WEL) is reset.

The Bulk Erase instruction is internally taken into account if, and only if, (BP0, BP1) = (0,0). In other

words, the Bulk Erase instruction is ignored if at least one Sector is software protected. In this case the Bulk Erase instruction is discarded and none of the Sectors are erased.

The timing sequence is shown in Figure 14.

Enter Deep Power Down Mode (DP)

After Power-on, when \bar{S} is high, the memory is deselected, the Q output pin is at high impedance and the device is in the Standby Power Mode state (I_{CC1}). Under this state, the Memory waits for a select condition and is able to receive, decode and execute all instructions. This mode is not the Deep Power Down Mode which is entered by the way of a specific instruction. The purpose of the Deep Power down mode is to drastically reduce the standby current from I_{CC1} to I_{CC2} (see Table 10). Once the device has entered the Deep Power Down Mode, all instructions are ignored except the RES instruction which releases the part from this

Figure 16. RES: Release from Deep Power Down Mode and Read Electronic Signature Sequence

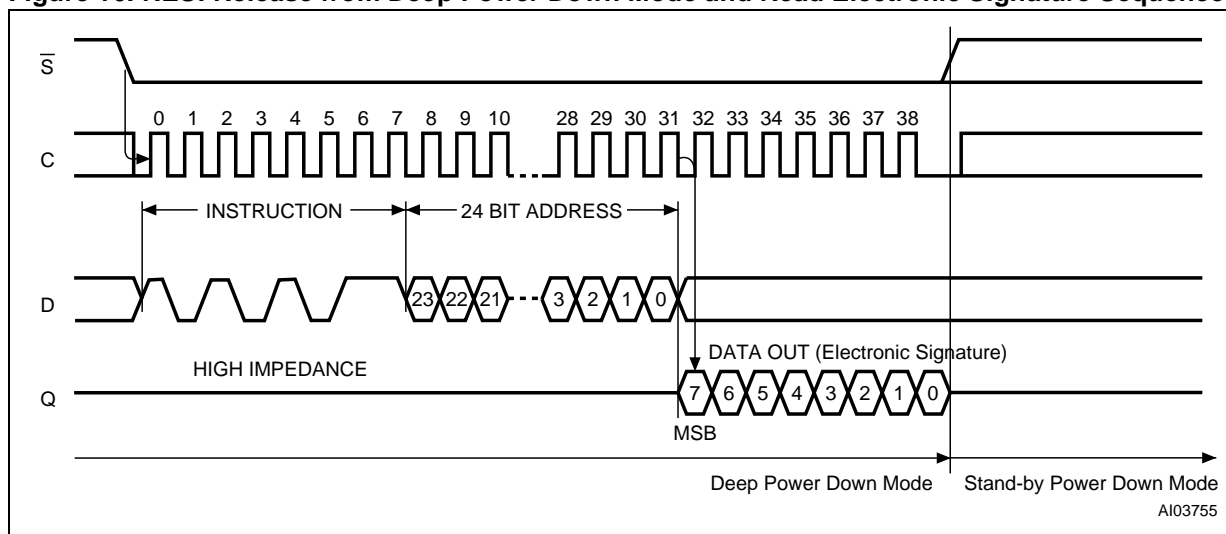
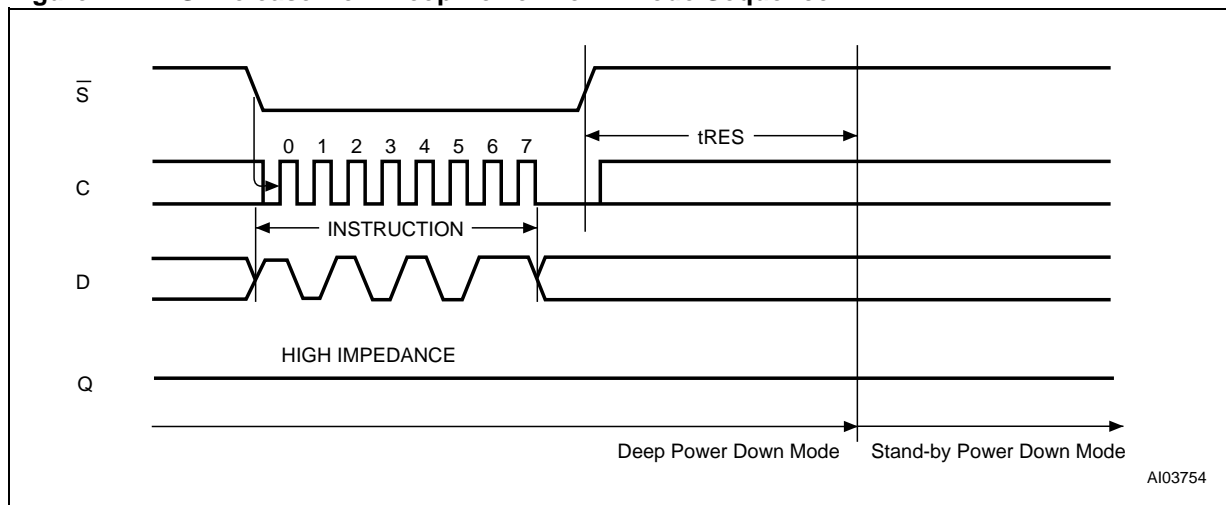


Figure 17. RES: Release from Deep Power Down Mode Sequence



mode. At the same time, the RES instruction provides the Electronic Signature of the device on the Q output pin. At power down, the Deep Down Mode is automatically discarded. This causes the device to always wake up in the Standby Power Mode state after power-on.

The DP instruction is entered by driving the Chip select input (\overline{S}) low, followed by the instruction byte on Data In input (D). The Chip Select input (\overline{S}) must be driven low for the entire duration of the sequence. The device must be deselected just after the eighth bit of the instruction byte has been latched in. If not, the DP instruction is not executed. As soon as the device is deselected, it requires t_{DP} to enter the Deep Power Down Mode where standby current is reduced to I_{CC2} .

The timing sequence is shown in Figure 15.

Release from Deep Power Down Mode and Read Electronic Signature (RES)

Once the device has entered the Deep Power Down Mode, all instructions are ignored except the RES instruction which releases the part from this mode. At the same time, the RES instruction provides the Electronic Signature of the device on the Q output pin. Except during an Erase, Program cycle or Write Status register, the RES instruction always provides access to the Electronic Signature of the device and can be applied even if the Deep Power Down Mode has not been entered. Any RES attempt during an Erase, Program cycle or Write Status register, will be rejected and will deselect the chip without having any effects on the ongoing Erase, Program cycle or Write Status Register.

The device is first selected by putting \overline{S} low. The RES instruction byte is followed by a dummy three bytes address (A23-A0), each bit being latched-in on Data In input (D) during the rising edge of the clock (C). Then, the Electronic Signature stored in the memory is shifted out on the Q output pin, each bit being shifted out during the falling edge of the clock (C). It is possible to continuously read the Electronic Signature value. The RES operation is terminated by deselecting the chip after the Electronic Signature has been read at least one time (see Figure 16). At this step, the device is immediately put again in the Standby Power Mode state. It waits for a select condition and is able to receive, decode and execute all instructions. Deselecting the device after the 8 bits RES instruction has been sent but before the LSB of the Electronic Signature has been read, will insure the Deep Power Down Mode to be released but will generate a delay (t_{RES}) before the device is put in Standby Power Mode state (see Figure 17) and \overline{S} must remain high for at least t_{RES} max value (see Table 13).

POWER ON STATE

At Power-up, the device must not be selected (that is the \overline{S} input must follow the voltage supplied on the V_{CC} pin) until the supply voltage reaches the minimum V_{CC} value (2.7 V). Once V_{CC} has reached the minimum operating voltage (2.7 V), the Chip Select input pin (\overline{S}) must remain high for a time higher than t_{VSL} min (See Table 8).

After a Power up, the memory is in the following state:

Table 8. Power-Up Timing and V_{WI} Threshold
($T_A = -40$ to $85\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{VSL}^1	$V_{CC}(\text{min})$ to \overline{S} low		10		μs
t_{PUW}^1	Time delay to Write operation			15	ms
V_{WI}^1	Write Inhibit Voltage		1.5	2.5	V

Note: 1. These parameters are characterized only.

- The device is in the low power standby state (not the Deep Power Down Mode).
- The chip is deselected.
- The Write Enable Latch is reset.

POWER UP OPERATION

In order to prevent data corruption and inadvertent Page Program, Erase or Write Status Register operations, an internal V_{CC} comparator inhibits all these features if the V_{CC} voltage is lower than V_{WI} (see Table 8).

Once the voltage applied on the V_{CC} pin goes over the V_{WI} threshold ($V_{CC} > V_{WI}$):

- Page Program, Erase and Write Status Register operations are allowed after a time-out of t_{PUW} , as specified in Table 8.
- This time-out delay allows the voltage applied on V_{CC} pin to reach $V_{CC}(\text{min})$ of the device. It should be noted that none of the device's operation are guaranteed till V_{CC} is not $\geq V_{CC}(\text{min})$.

DATA PROTECTION AND PROTOCOL CONTROL

Once all bits of a Page Program, Sector Erase, Bulk Erase or Status Register Write instruction are received; the \overline{S} input must be driven high (Deselect) right after the proper clock count in order to execute the instruction, that is the Chip Select \overline{S} must driven high after a clock pulses count multiple of 8 bit.

Attempting to access the memory array during a Write, Program or Erase cycle is ignored, however the internal cycle continues.

ELECTRONIC SIGNATURE

The device features an 8 bits Electronic Signature (10h) which can be read with the help of the RES instruction (please see the section entitled "Release from Deep Power Down Mode and Read Electronic Signature (RES)" on page 12).

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set at '1' (each byte = FFh). The

Table 9. Initial Status Register Format

b7							b0
0	0	0	0	0	0	0	0

Status Register content is 00h (all Status Register bits are '0').

Table 10. DC Characteristics(T_A = -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I _{LI}	Input Leakage Current			± 2	μA
I _{LO}	Output Leakage Current			± 2	μA
I _{CC1}	Stand-by mode Current	$\overline{S} = V_{CC}$, V _{IN} = V _{SS} or V _{CC}		50	μA
I _{CC2}	Deep Power Down Current	$\overline{S} = V_{CC}$, V _{IN} = V _{SS} or V _{CC}		5	μA
I _{CC3}	Operating Current (READ)	C = 0.1V _{CC} / 0.9.V _{CC} at 20 MHz, Q = open		3	mA
I _{CC4}	Operating Current (PP)	$\overline{S} = V_{CC}$		15	mA
I _{CC5}	Operating Current (WRSR)	$\overline{S} = V_{CC}$		15	mA
I _{CC6}	Operating Current (SE)	$\overline{S} = V_{CC}$		15	mA
I _{CC7}	Operating Current (BE)	$\overline{S} = V_{CC}$		15	mA
V _{IL}	Input Low Voltage		- 0.6	0.3V _{CC}	V
V _{IH}	Input High Voltage		0.7V _{CC}	V _{CC} +1	V
V _{OL}	Output Low Voltage	I _{OL} = 1.6 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -100 μA	V _{CC} -0.2		V

Table 11. Input Parameters¹ (T_A = 25 °C, f = 20 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C _{OUT}	Output Capacitance (Q)			8	pF
C _{IN}	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested.

Table 12. AC Measurement Conditions

Input Rise and Fall Times	≤ 5 ns
Input Pulse Voltages	0.2V _{CC} to 0.8V _{CC}
Input and Output Timing Reference Voltages	0.3V _{CC} to 0.7V _{CC}
Output Load	C _L = 30 pF

Note: 1. Output Hi-Z is defined as the point where data out is no longer driven.

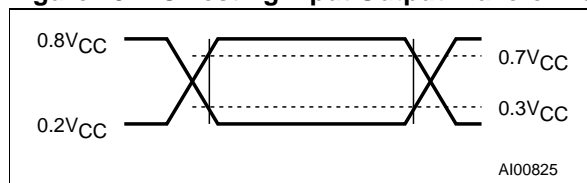
Figure 18. AC Testing Input Output Waveforms

Table 13. AC Characteristics

Symbol	Alt.	Parameter	M25P10		Unit
			V _{CC} =2.7 to 3.6 V T _A =−40 to 85°C		
			Min	Max	
f _C	f _C	Clock Frequency	D.C.	20	MHz
t _{SLCH}	t _{CSS}	\overline{S} Active Setup Time (relative to C)	10		ns
t _{CHSL}		\overline{S} Not Active Hold Time (relative to C)	10		ns
t _{CH} ¹	t _{CLH}	Clock High Time	22		ns
t _{CL} ¹	t _{CLL}	Clock Low Time	22		ns
t _{DVCH}	t _{DSU}	Data In Setup Time	5		ns
t _{CHDX}	t _{DH}	Data In Hold Time	5		ns
t _{CHSH}		\overline{S} Active Hold Time (relative to C)	10		ns
t _{SHCH}		\overline{S} Not Active Setup Time (relative to C)	10		ns
t _{SHSL}	t _{CSH}	\overline{S} Deselect Time	50		ns
t _{SHQZ} ²	t _{DIS}	Output Disable Time		20	ns
t _{CLQV}	t _v	Clock Low to Output Valid		20	ns
t _{CLQX}	t _{HO}	Output Hold Time	0		ns
t _{HLCH}		\overline{HOLD} Setup Time (relative to C)	10		ns
t _{CHHH}		\overline{HOLD} Hold Time (relative to C)	10		ns
t _{HHCH}		HOLD Setup Time (relative to C)	10		ns
t _{CHHL}		HOLD Hold Time (relative to C)	10		ns
t _{HHQX} ²	t _{LZ}	HOLD to Output Low-Z		20	ns
t _{HLQZ} ²	t _{HZ}	\overline{HOLD} to Output High-Z		20	ns
t _{DP} ²		\overline{S} High to Deep Power Down Mode		1.6	μs
t _{RES} ²		\overline{S} High to Stand-by Power Mode		1.6	μs
t _W		Write Status Register Cycle Time		5	ms
t _{PP}		Page Program Cycle Time		5	ms
t _{SE}		Sector Erase Cycle Time		2	s
t _{BE}		Bulk Erase Cycle Time		4	s

Note: 1. t_{CH} + t_{CL} ≥ 1 / f_C.

2. Value guaranteed by characterization, not 100% tested in production. These parameters are specified with an output load capacitance of 30 pF.

Figure 19. Serial Input Timing

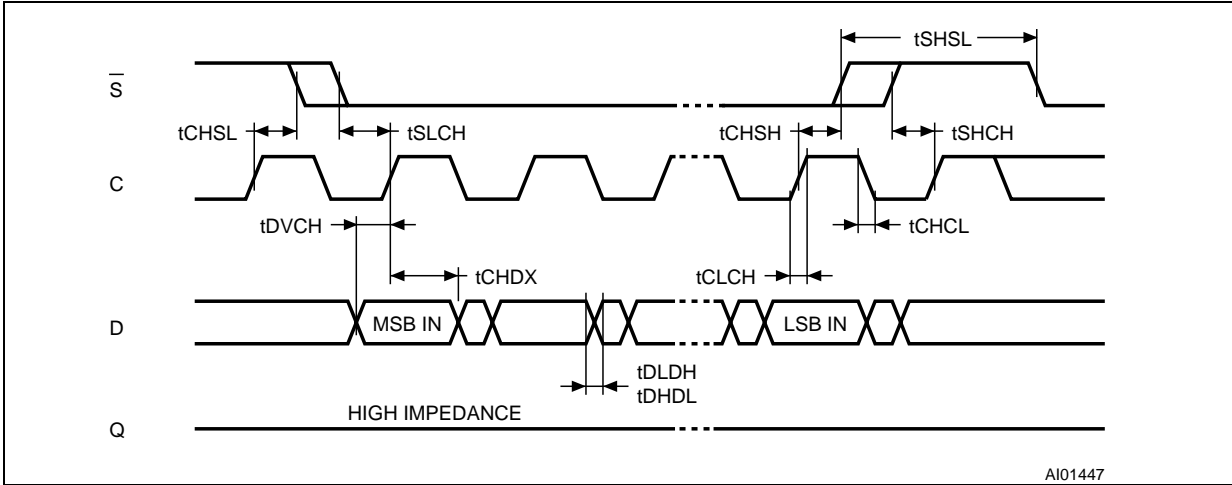


Figure 20. Hold Timing

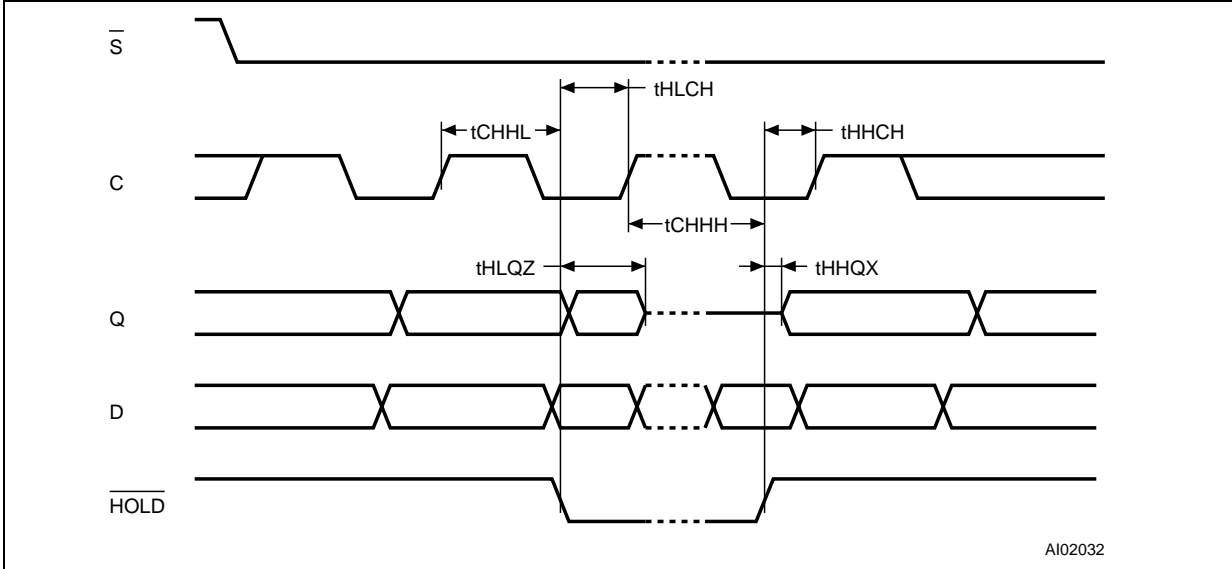


Figure 21. Output Timing

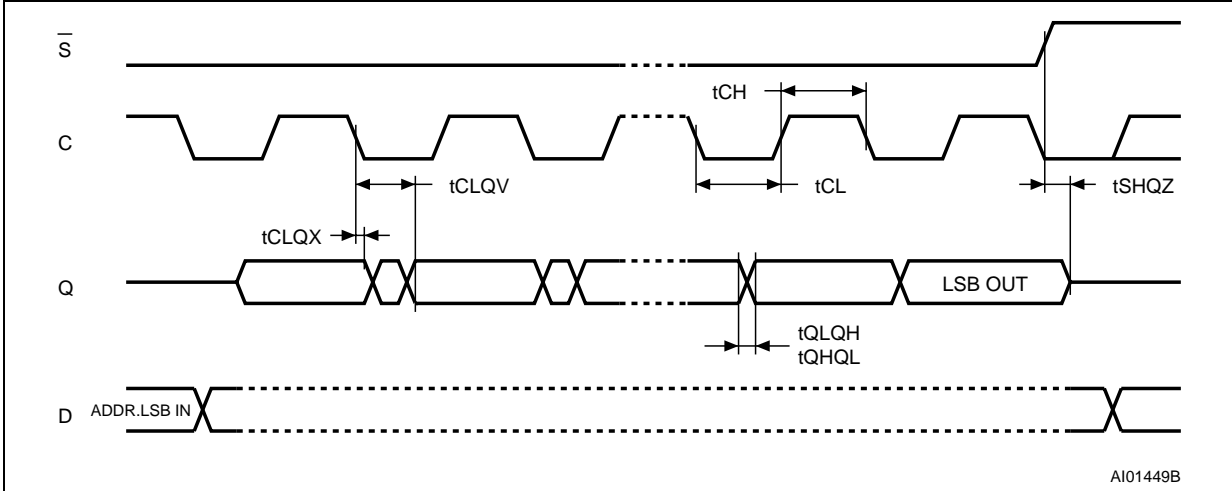


Table 14. Ordering Information Scheme

Example:

M25P10		–	V	MW	6	T	
Memory Capacity						Option	
10	1 Mbit (128K x 8)					T	Tape and Reel Packing
						Temperature Range	
						6	–40 °C to 85 °C
Operating Voltage						Package	
V	2.7 V to 3.6 V					MN	SO8 (150 mil width)
						MW	SO8 (200 mil width)

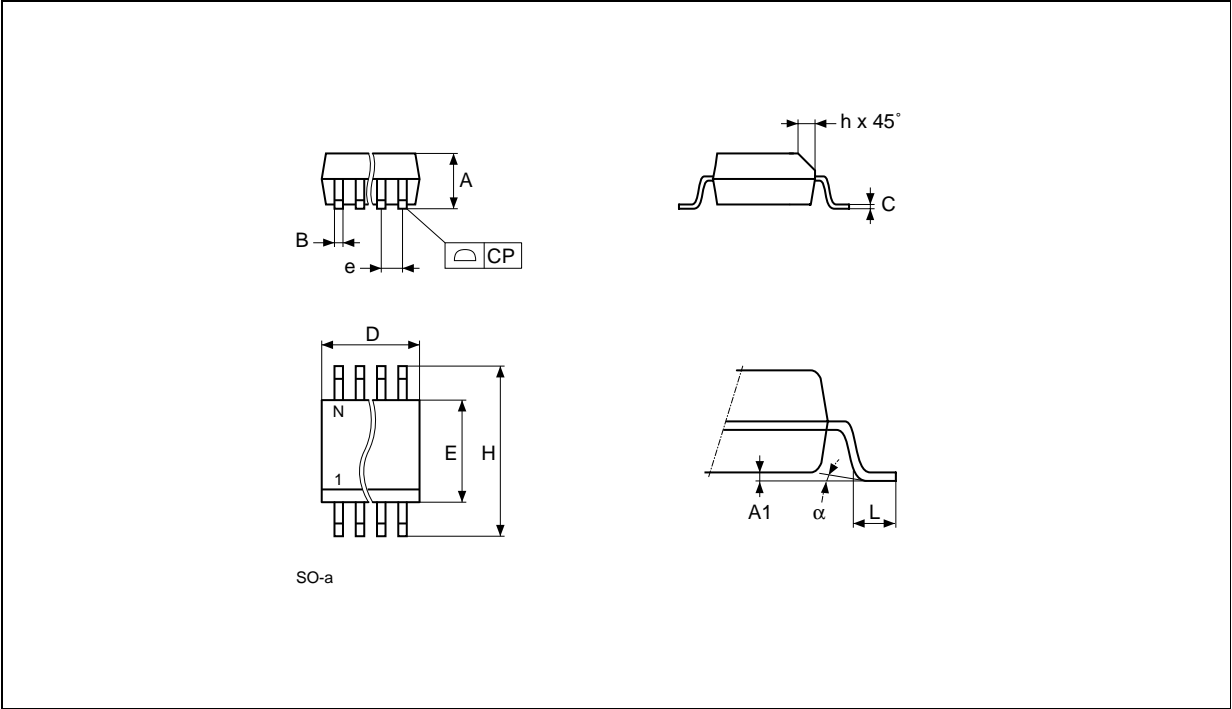
ORDERING INFORMATION

The notation used for the device number is as shown in Table 14. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office

Table 15. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	—	—	0.050	—	—
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 22. SO8 narrow (MN)

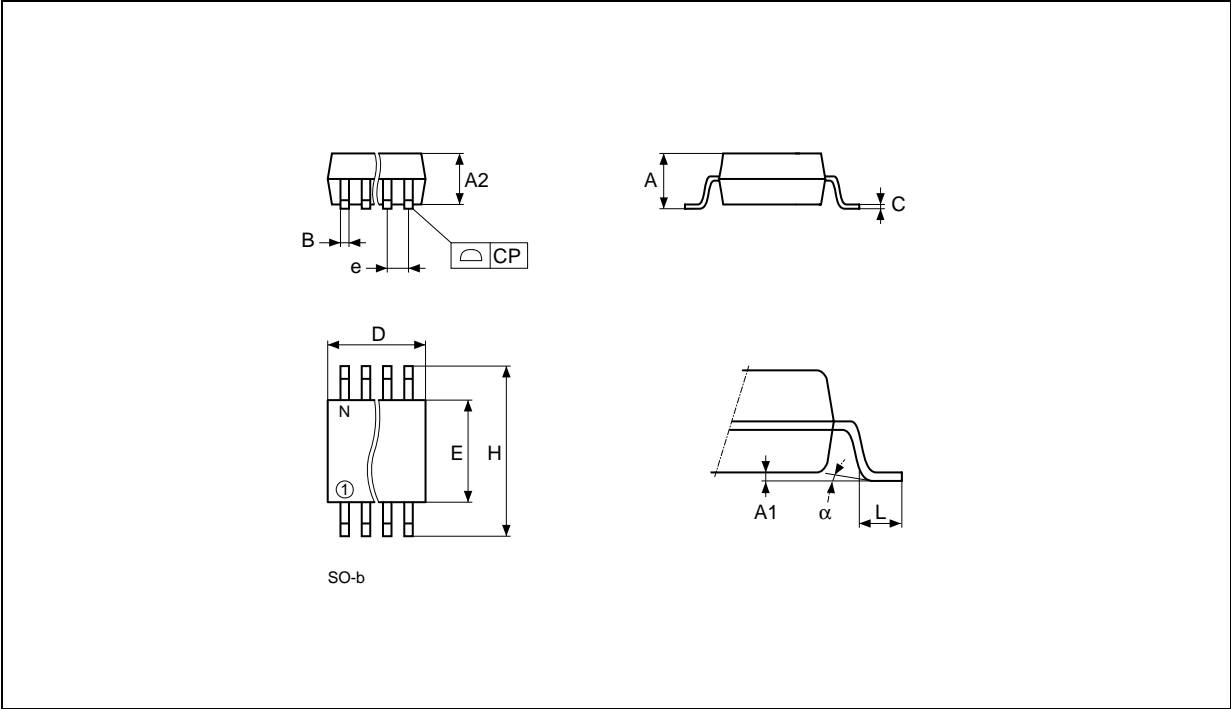


Note: 1. Drawing is not to scale.

Table 16. SO8 - 8 lead Plastic Small Outline, 200 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

Figure 23. SO8 wide (MW)



Note: 1. Drawing is not to scale.

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