



# STS8C5H30L

N-CHANNEL 30V - 0.018Ω - 8A SO-8

P-CHANNEL 30V - 0.045Ω - 5A SO-8

LOW GATE CHARGE StripFET™ III MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS8C5H30L (N-Channel)	30 V	< 0.022 Ω	8 A
STS8C5H30L (P-Channel)	30 V	< 0.055 Ω	5 A

- TYPICAL R<sub>DS(on)</sub> (N-Channel) = 0.018 Ω
- TYPICAL R<sub>DS(on)</sub> (P-Channel) = 0.045 Ω
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DRIVE
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

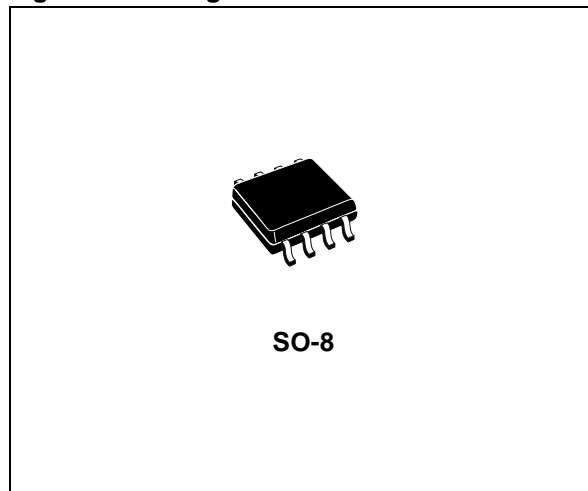
## DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

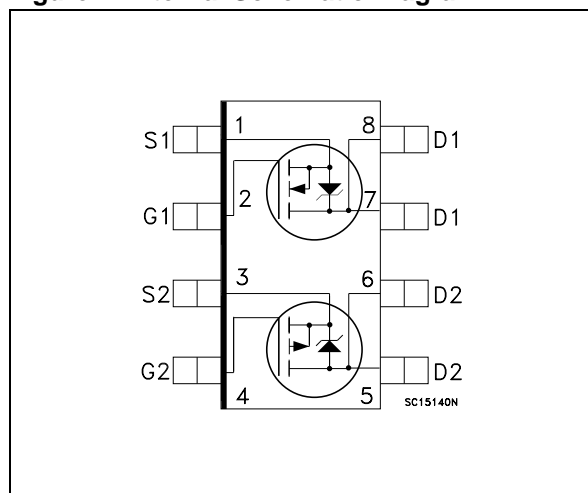
## APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES
- DC MOTOR DRIVE

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

PART NUMBER	MARKING	PACKAGE	PACKAGING
STS8C5H30L	S8C5H30L	SO-8	TAPE & REEL

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value		Unit
		N-CHANNEL	P-CHANNEL	
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	30		V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	30		V
$V_{GS}$	Gate- source Voltage	$\pm 16$	$\pm 16$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$ Single Operating	8	4.2	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$ Single Operating	6.4	3.1	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	32	16.8	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$ Dual Operating	1.6		W
	Total Dissipation at $T_C = 25^\circ\text{C}$ Single Operating	2		W
$T_j$	Operating Junction Temperature	150		$^\circ\text{C}$
$T_{stg}$	Storage Temperature	-55 to 150		$^\circ\text{C}$

( $\bullet$ ) Pulse width limited by safe operating area

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

**Table 4: Thermal Data**

$R_{thj-case}$	Thermal Resistance Junction-case Single Operating Dual Operating	62.5 78	$^\circ\text{C/W}$ $^\circ\text{C/W}$
$T_I$	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^\circ\text{C}$  UNLESS OTHERWISE SPECIFIED)

**Table 5: On/Off**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	n-ch p-ch	30 30			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$	n-ch p-ch			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16\text{V}$ $V_{GS} = \pm 16\text{V}$	n-ch p-ch			$\pm 100$ $\pm 100$	nA nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	n-ch p-ch	1 1	1.6	2.5	V V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 2.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 4\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 2.5\text{ A}$	n-ch p-ch n-ch p-ch		0.018 0.045 0.020 0.070	0.022 0.055 0.025 0.075	$\Omega$ $\Omega$ $\Omega$ $\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$g_{fs}(1)$	Forward Transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 4\text{ A}$ $V_{DS} = 15\text{ V}$ , $I_D = 2.5\text{ A}$	n-ch p-ch		8.5 10		S S
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	n-ch p-ch		857 1350		pF pF
$C_{oss}$	Output Capacitance		n-ch p-ch		147 490		pF pF
$C_{rss}$	Reverse Transfer Capacitance		n-ch p-ch		20 130		pF pF

(1) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**ELECTRICAL CHARACTERISTICS(CONTINUED)****Table 7: Switching On**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$	n-ch		12		ns
			p-ch		25		ns
		<b>P-CHANNEL</b> $V_{DD} = 15\text{ V}$ , $I_D = 2\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$ (Resistive Load see, Figure 28)	n-ch		14.5		ns
			p-ch		35		ns
$Q_g$	Total Gate Charge	$V_{DD} = 24\text{ V}$ , $I_D = 8\text{ A}$ , $V_{GS} = 5\text{ V}$	n-ch p-ch		7 12.5	10 16	nC nC
$Q_{gs}$	Gate-Source Charge	<b>P-CHANNEL</b> $V_{DD} = 24\text{ V}$ , $I_D = 4\text{ A}$ , $V_{GS} = 5\text{ V}$ (see, Figure 31)	n-ch		2.5		nC
			p-ch		5		nC
$Q_{gd}$	Gate-Drain Charge		n-ch p-ch		2.3 3		nC nC

**Table 8: Switching Off**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$	n-ch		23		ns
			p-ch		125		ns
		<b>P-CHANNEL</b> $V_{DD} = 15\text{ V}$ , $I_D = 2.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$ (Resistive Load see, Figure 28)	n-ch		8		ns
			p-ch		35		ns

**Table 9: Source-Drain Diodef**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current		n-ch p-ch			8 5	A A
$I_{SDM(2)}$	Source-drain Current (pulsed)		n-ch p-ch			32 20	A A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 8\text{ A}$ , $V_{GS} = 0$ $I_{SD} = 5\text{ A}$ , $V_{GS} = 0$	n-ch p-ch			1.5 1.2	V V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ , $T_j = 150^\circ\text{C}$	n-ch p-ch		15 45		ns ns
$Q_{rr}$	Reverse Recovery Charge	<b>P-CHANNEL</b> $I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ , $T_j = 150^\circ\text{C}$ (see test circuit, Figure 29)	n-ch		5.7		nC
			p-ch		36		nC
$I_{RRM}$	Reverse Recovery Current		n-ch p-ch		0.76 1.6		A A

(1) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3)  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Figure 3: .Safe Operating n-channel

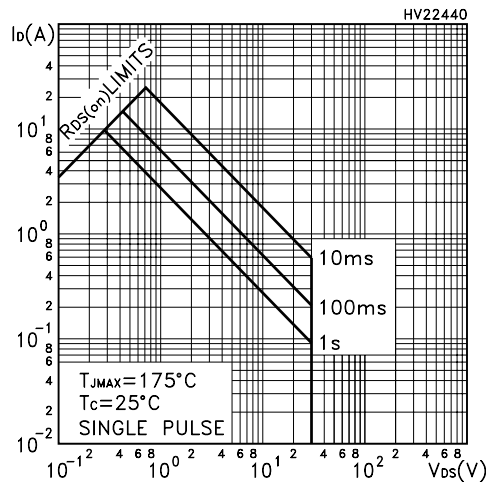


Figure 4: Output Characteristics n-channel

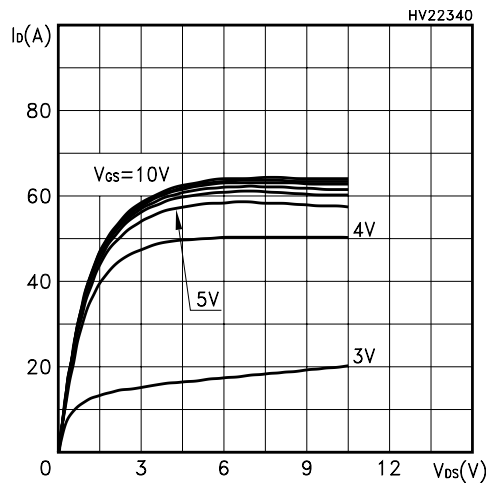


Figure 5: Transconductance n-channel

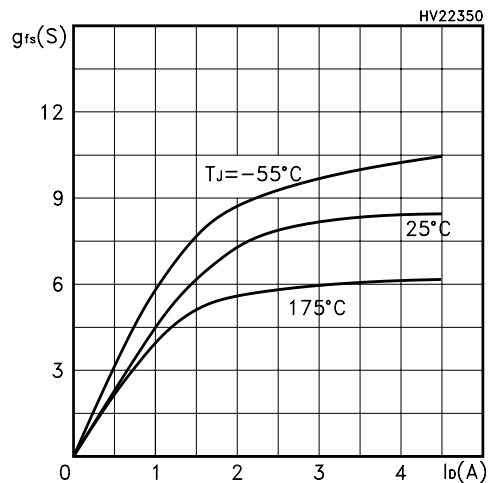


Figure 6: Thermal Impedance For Complementary Pair

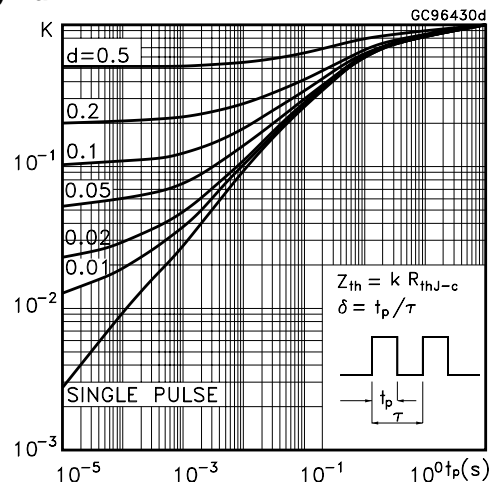


Figure 7: Transfer Characteristics n-channel

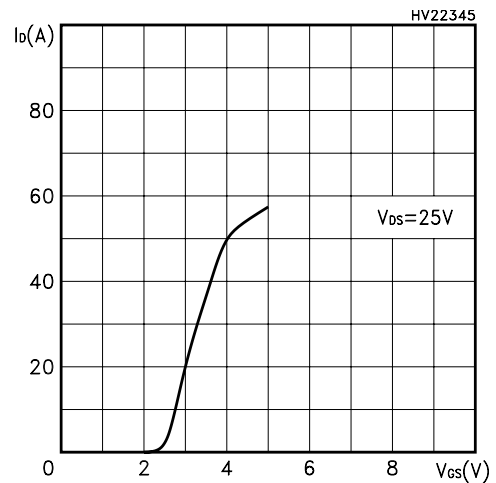
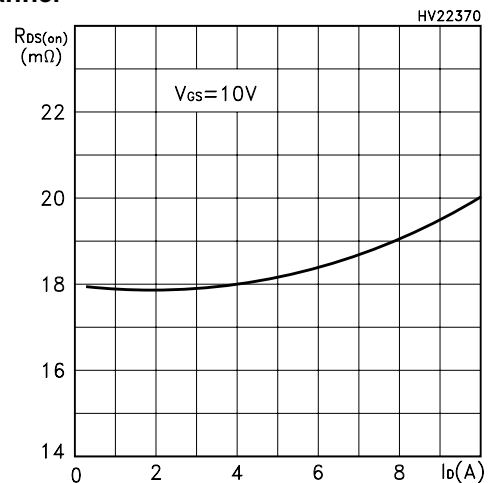
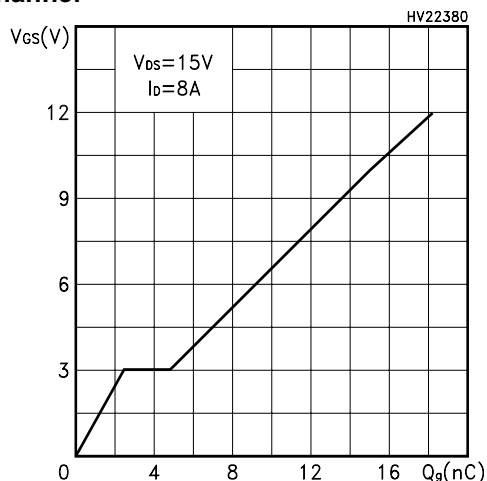


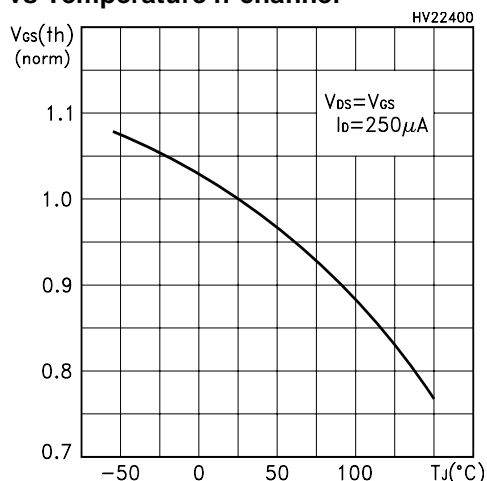
Figure 8: Static Drain-Source On Resistance n-channel



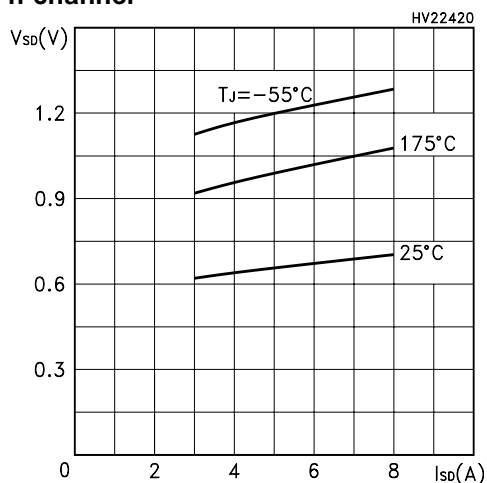
**Figure 9: Gate Charge vs Gate-Source Voltage n-channel**



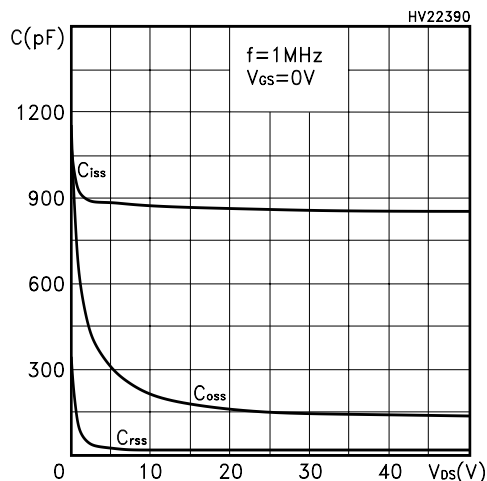
**Figure 10: Normalized Gate Threshold Voltage vs Temperature n-channel**



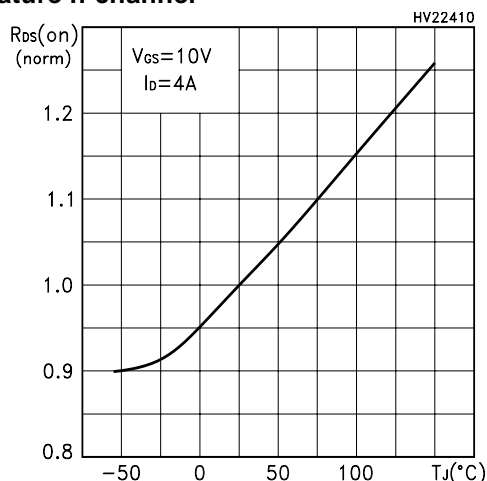
**Figure 11: Source-Drain Forward Characteristics n-channel**



**Figure 12: Capacitance Variations n-channel**



**Figure 13: Normalized On Resistance vs Temperature n-channel**



**Figure 14: Normalized BVdss vs Temperature n-channel**

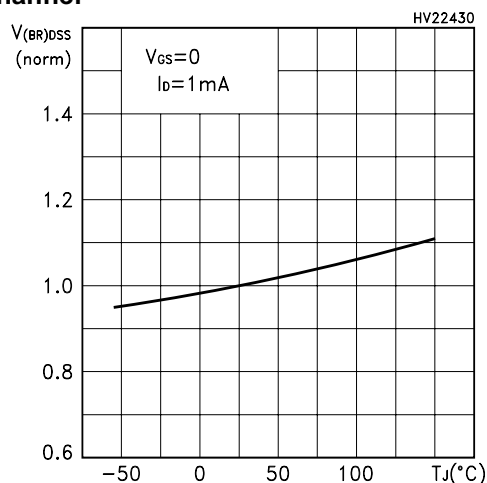


Figure 15: Safe Operating p-channel

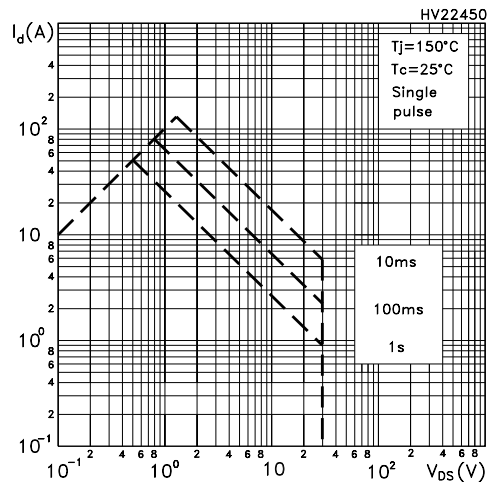


Figure 16: Output Characteristics p-channel

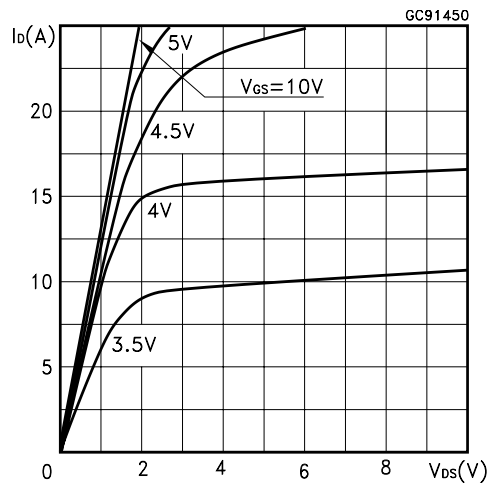


Figure 17: Transconductance p-channel

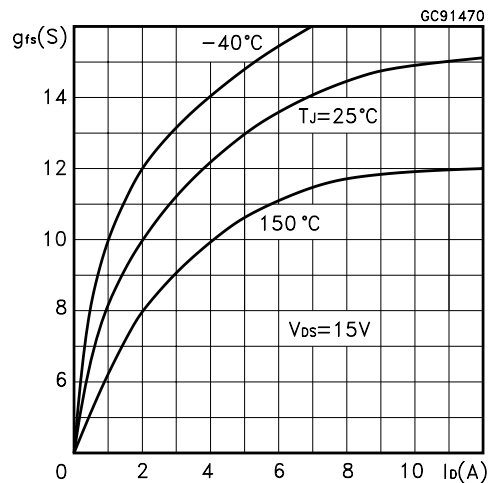


Figure 18: Thermal Impedance for Complementary Pair

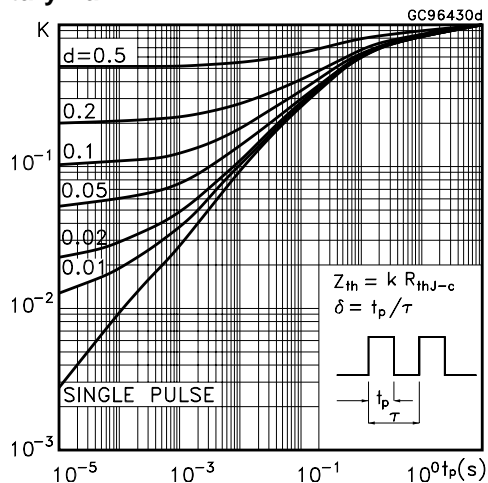


Figure 19: Transfer Characteristics p-channel

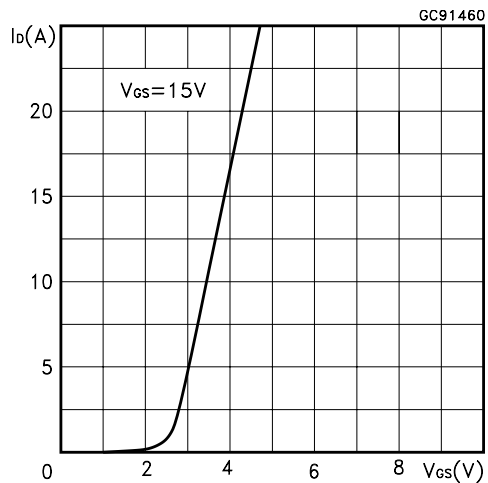
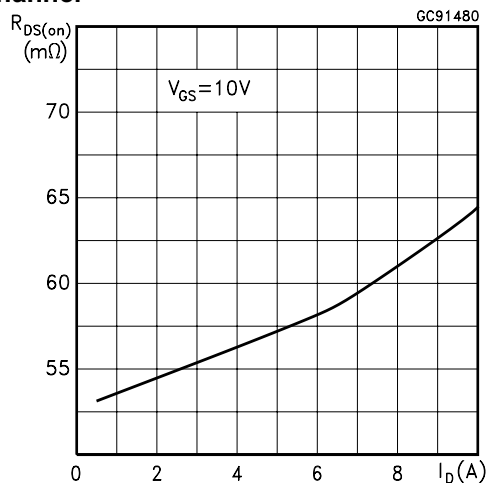
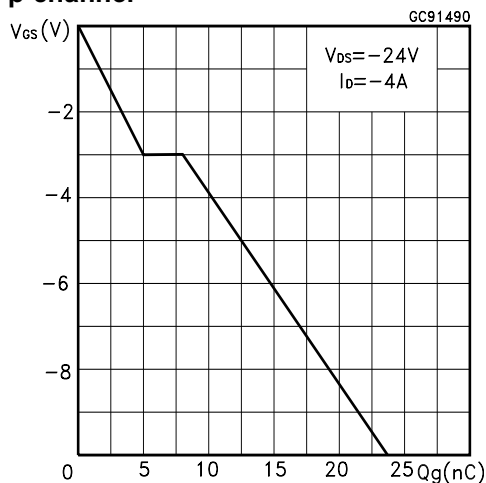


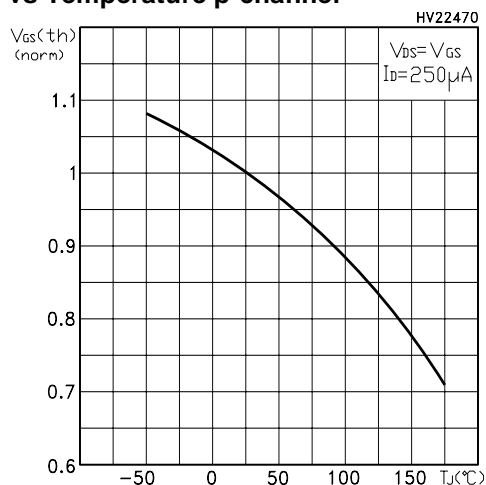
Figure 20: Static Drain-Source On Resistance p-channel



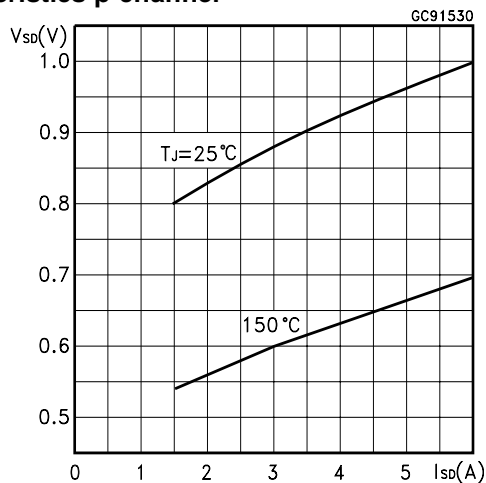
**Figure 21: Gate Charge vs Gate-Source Voltage p-channel**



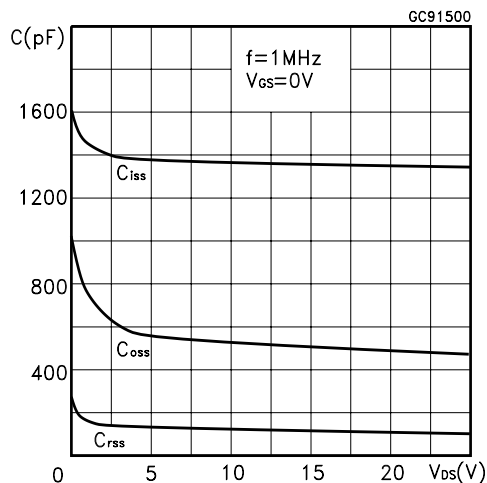
**Figure 22: Normalized Gate Threshold Voltage vs Temperature p-channel**



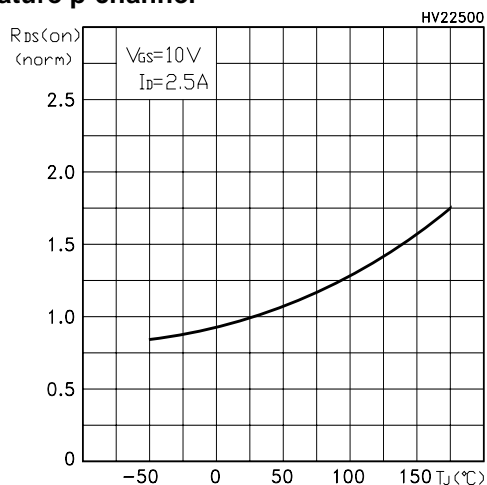
**Figure 23: Source-Drain Diode Forward Characteristics p-channel**



**Figure 24: Capacitances Variations p-channel**



**Figure 25: Normalized On Resistance vs Temperature p-channel**



**Figure 26: Normalized BVdss vs Temperature p-channel**

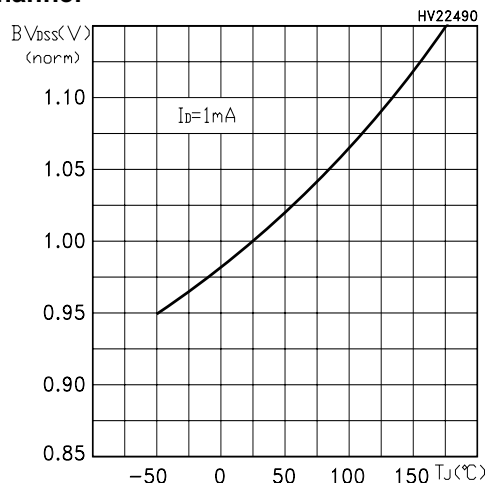


Figure 27: Unclamped Inductive Load Test Circuit

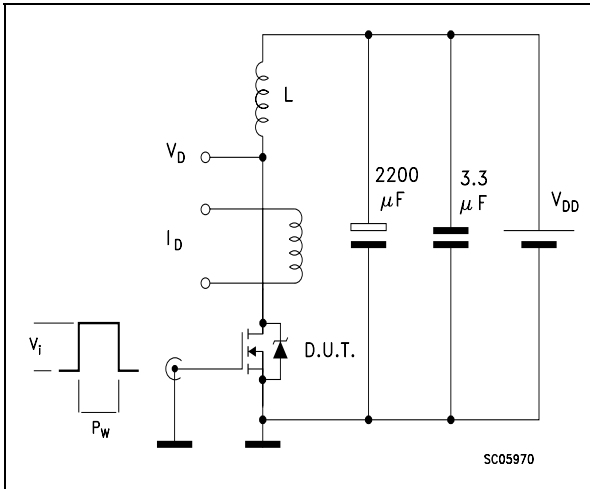


Figure 28: Switching Times Test Circuit For Resistive Load

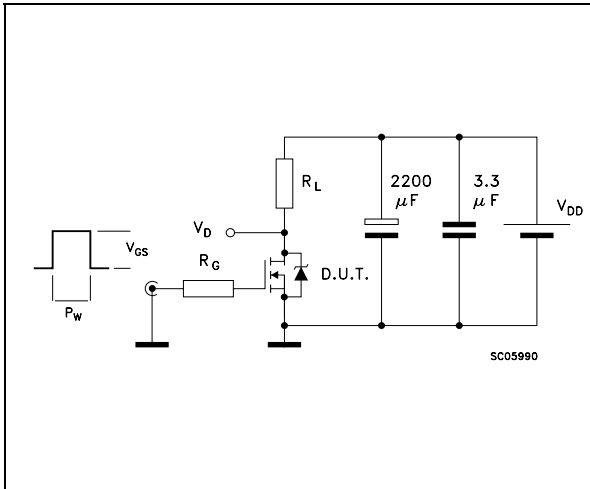


Figure 29: Test Circuit For Inductive Load Switching and Diode Recovery Times

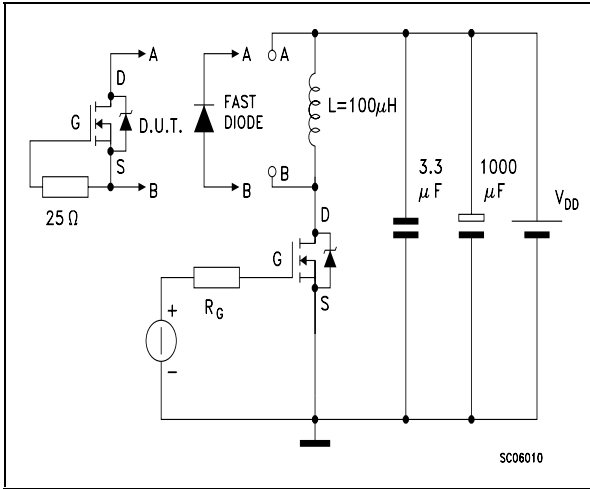


Figure 30: Unclamped Inductive Waform

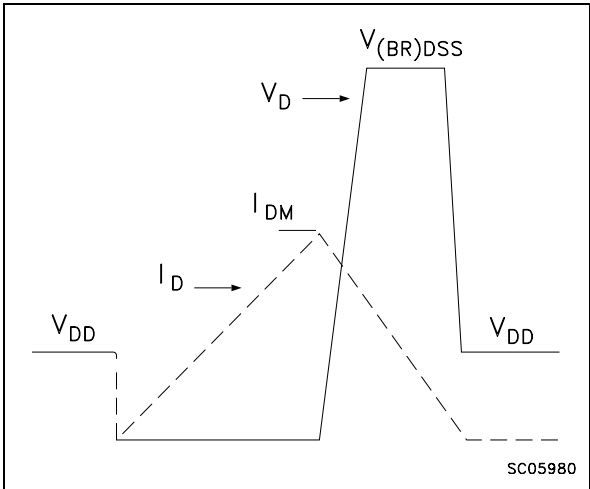
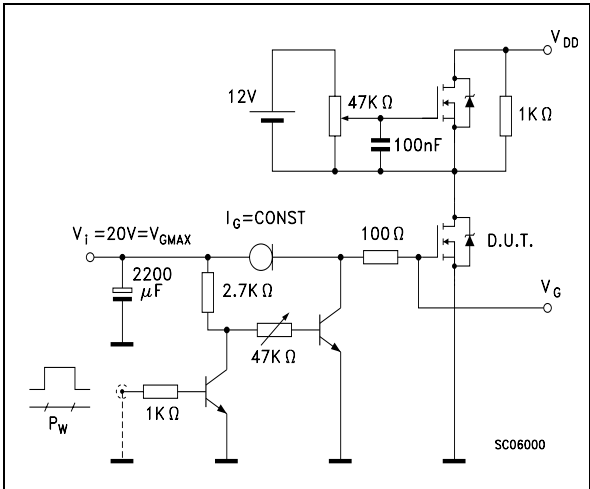


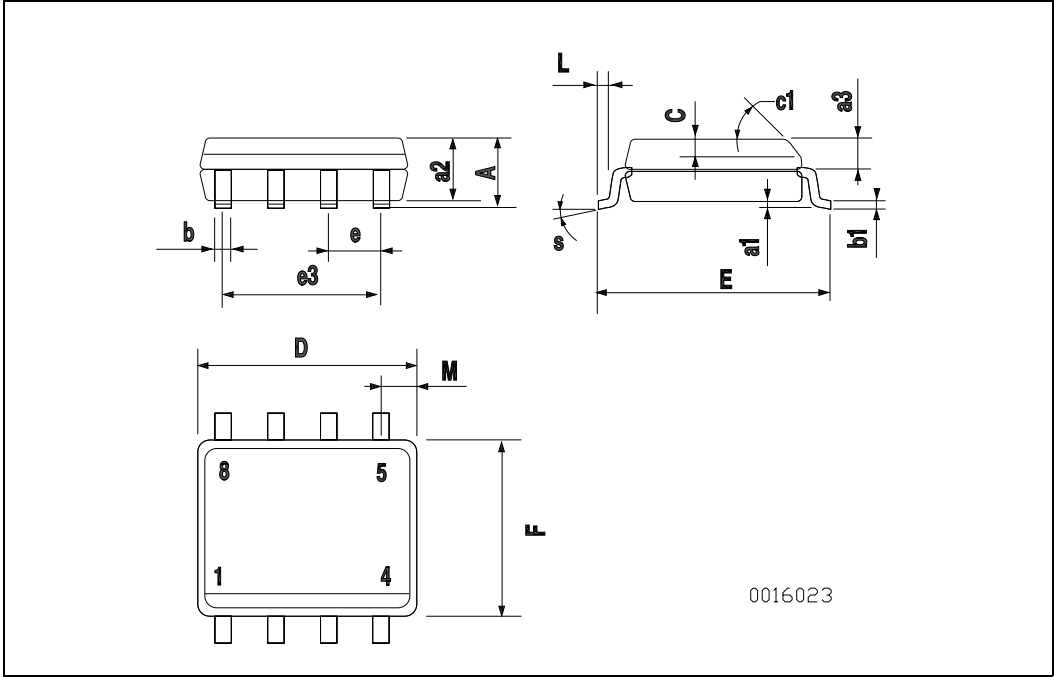
Figure 31: Gate Charge Test Circuit





SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



**Table 10: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
10-Aug-2004	1	First Revision
10-Sep-2004	2	Complete Version

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