



# STB120NH03L

## N-CHANNEL 30V - 0.005 $\Omega$ - 60A D<sup>2</sup>PAK STripFET™ III POWER MOSFET FOR DC-DC CONVERSION

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB120NH03L	30 V	<0.0055 $\Omega$	60 A(#)

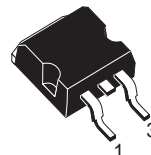
- TYPICAL R<sub>DS(on)</sub> = 0.005  $\Omega$  @ 10 V
- R<sub>DS(ON)</sub> \* Q<sub>g</sub> INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D<sup>2</sup>PAK (TO-263)  
POWER PACKAGE IN TUBE (NO SUFFIX) OR  
IN TAPE & REEL (SUFFIX "T4")

### DESCRIPTION

The STB120NH03L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

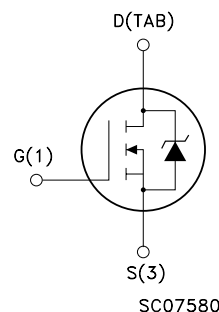
### APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED  
FOR HIGH EFFICIENCY DC-DC  
CONVERTERS



**D<sup>2</sup>PAK  
TO-263**  
(Suffix "T4")

### INTERNAL SCHEMATIC DIAGRAM



### Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB120NH03LT4	B120NH03L	TO-252	TAPE & REEL

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	30	V
V <sub>GS</sub>	Gate- source Voltage	$\pm 20$	V
I <sub>D</sub> (#)	Drain Current (continuous) at T <sub>C</sub> = 25°C	60	A
I <sub>D</sub> (#)	Drain Current (continuous) at T <sub>C</sub> = 100°C	60	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	240	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	115	W
	Derating Factor	0.77	W/°C
E <sub>AS</sub> (1)	Single Pulse Avalanche Energy	700	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

(#) Value limited by wire bonding

(1) Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 30A, V<sub>DD</sub> = 15V

**THERMAL DATA**

Rthj-case	Thermal Resistance Junction-case	Max	1.30	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

**ELECTRICAL CHARACTERISTICS** (T<sub>case</sub> = 25 °C unless otherwise specified)**OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 µA V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	µA µA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA

**ON (\*)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 µA	1	1.8	2.5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 30 A V <sub>GS</sub> = 5 V I <sub>D</sub> = 30 A		0.005 0.006	0.0055 0.0105	Ω Ω

**DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 10 V I <sub>D</sub> = 30 A		40		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 15V f = 1 MHz V <sub>GS</sub> = 0		4100 680 70		pF pF pF
R <sub>G</sub>	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.3		Ω

**ELECTRICAL CHARACTERISTICS** (continued)**SWITCHING ON (\*)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		16 95		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=15\text{ V}$ $I_D=60\text{ A}$ $V_{GS}=10\text{ V}$		57 11.8 7.3	77	nC nC nC
$Q_{oss}^{(1)}$	Output Charge	$V_{DS} = 16\text{ V}$ $V_{GS} = 0\text{ V}$		27		nC
$Q_{glS}^{(2)}$	Third-quadrant Gate Charge	$V_{DS} < 0\text{ V}$ $V_{GS} = 10\text{ V}$		55		nC

**SWITCHING OFF(\*)**

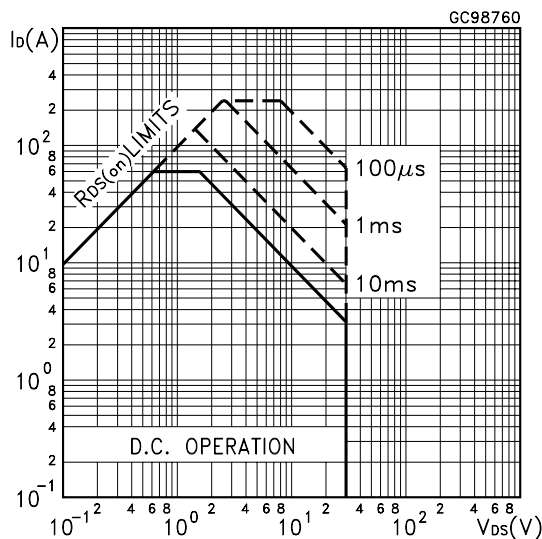
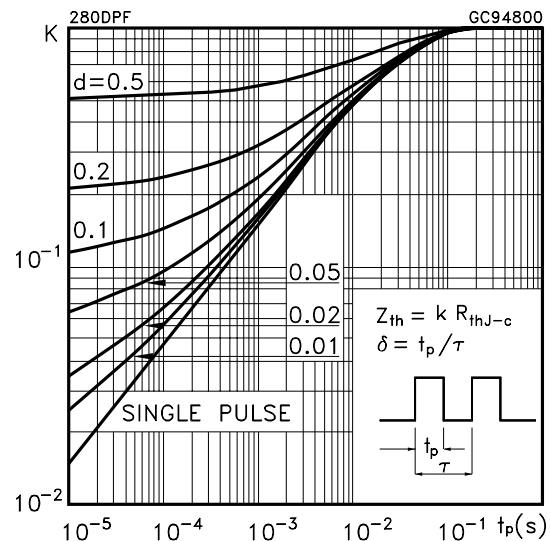
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$		48 23		ns ns

**SOURCE DRAIN DIODE(\*)**

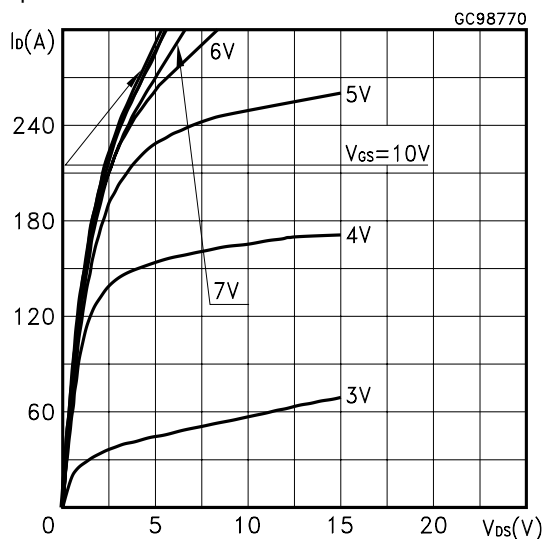
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$	Source-drain Current Source-drain Current (pulsed)				60 240	A A
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD} = 30\text{ A}$ $V_{GS} = 0$			1.4	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 60\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		46 64 2.8	62 86	ns nC A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.(•) Pulse width limited by  $T_{jmax}$ (1)  $Q_{oss} = C_{oss} \cdot \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{ds}$ , See Appendix A

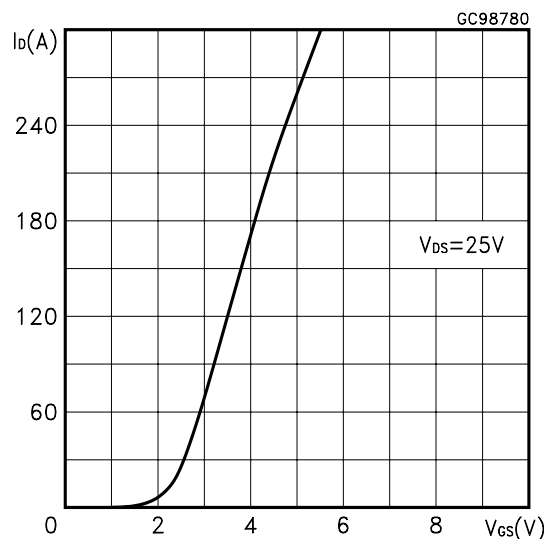
(2) Gate charge for synchronous operation

**Safe Operating Area****Thermal Impedance**

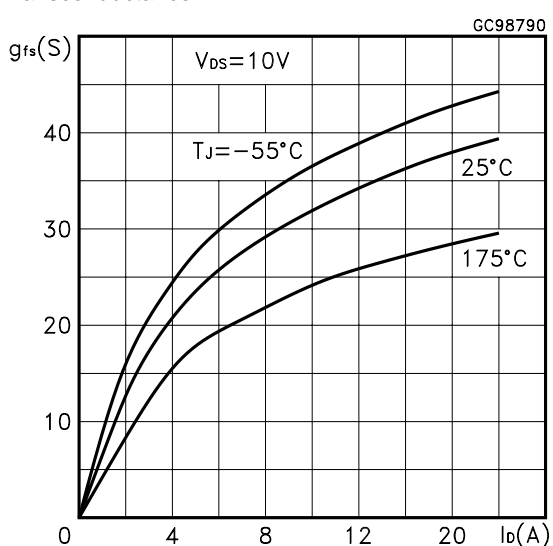
Output Characteristics



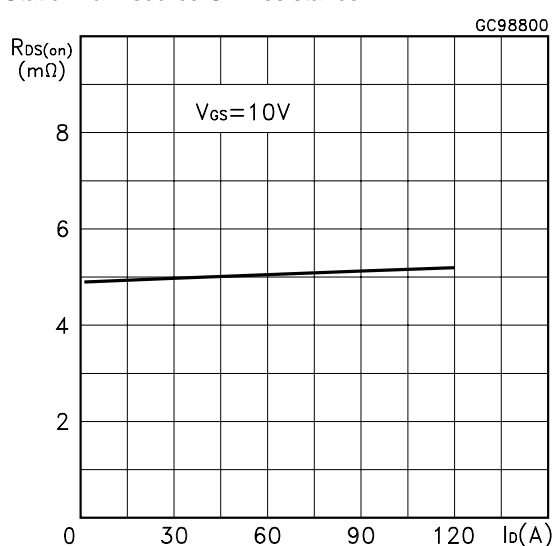
Transfer Characteristics



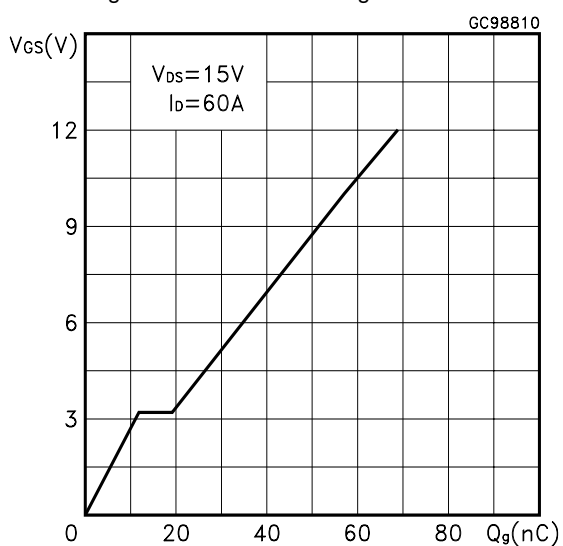
Transconductance



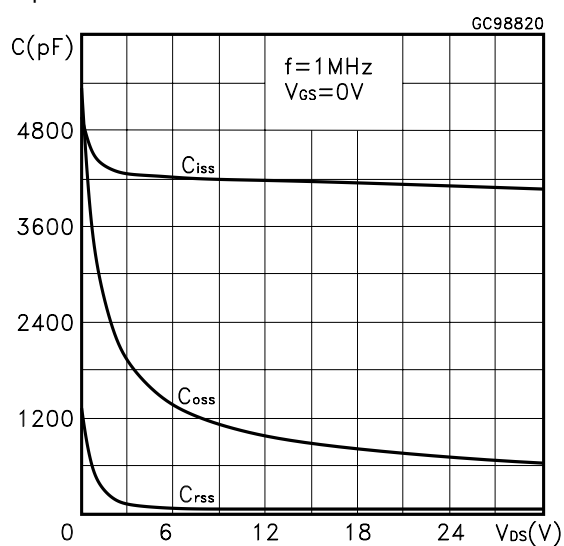
Static Drain-source On Resistance



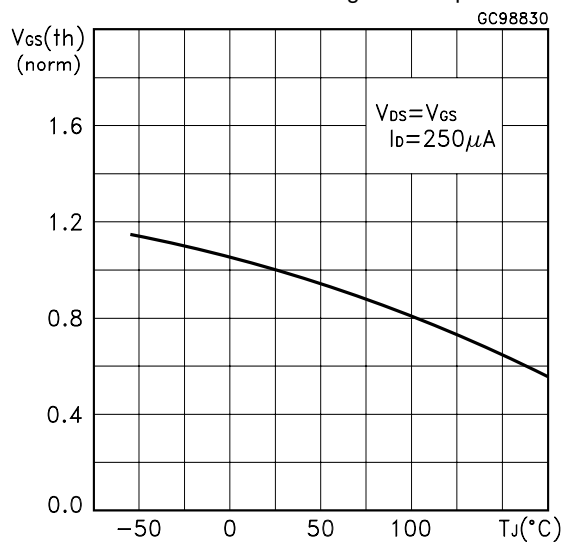
Gate Charge vs Gate-source Voltage



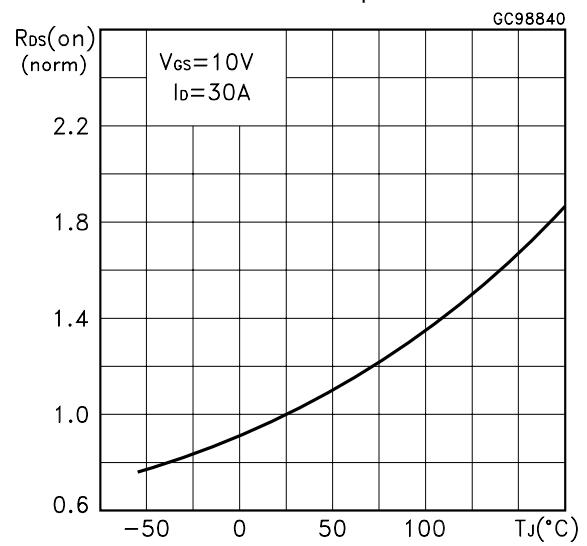
Capacitance Variations



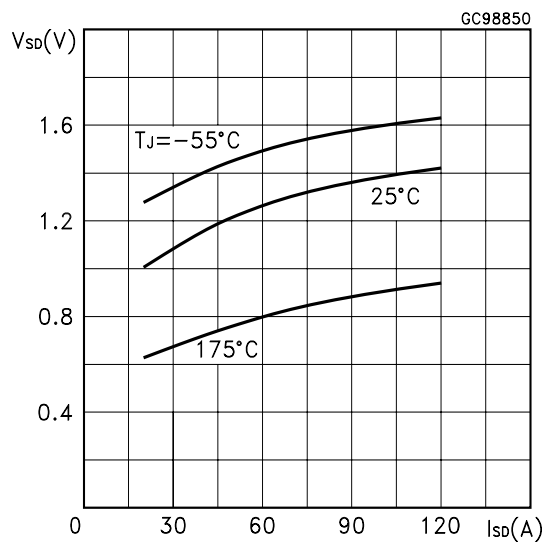
Normalized Gate Threshold Voltage vs Temperature



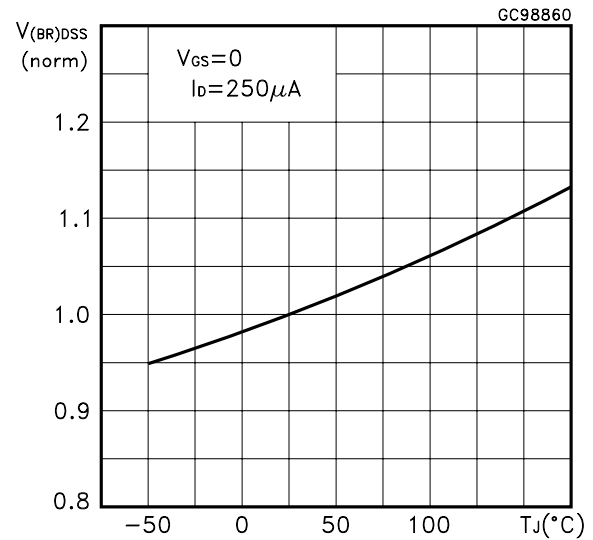
Normalized on Resistance vs Temperature



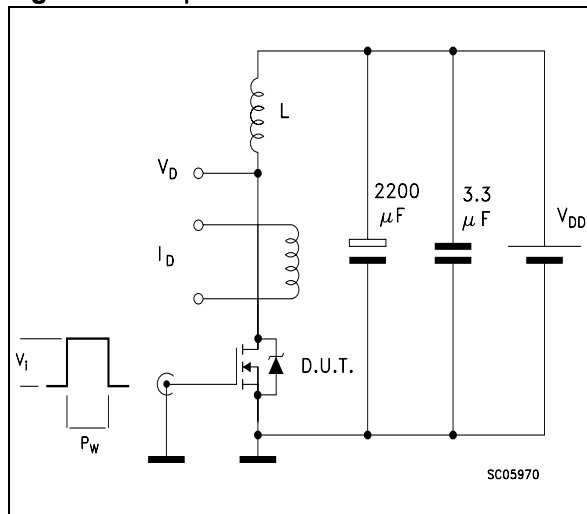
Source-drain Diode Forward Characteristics



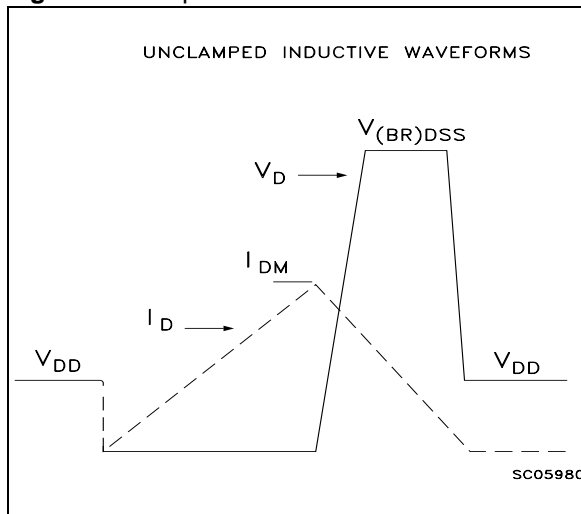
Normalized Breakdown Voltage vs Temperature



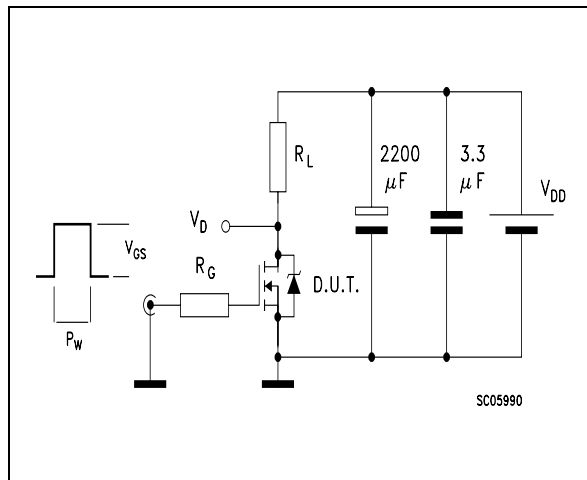
**Fig. 1: Unclamped Inductive Load Test Circuit**



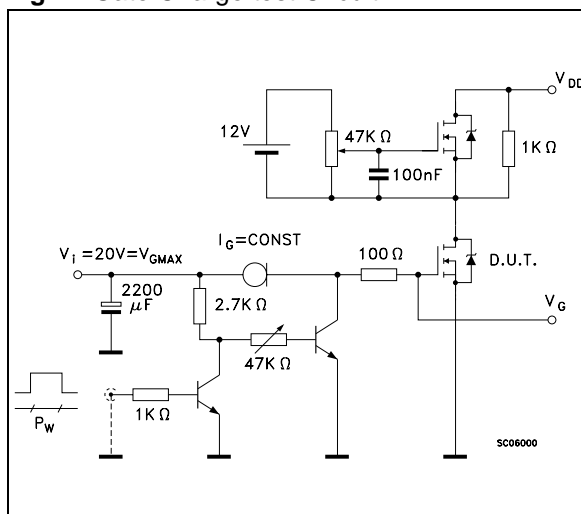
**Fig. 2: Unclamped Inductive Waveform**



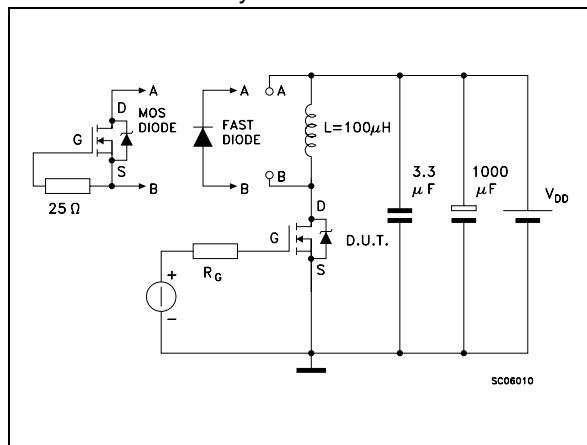
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

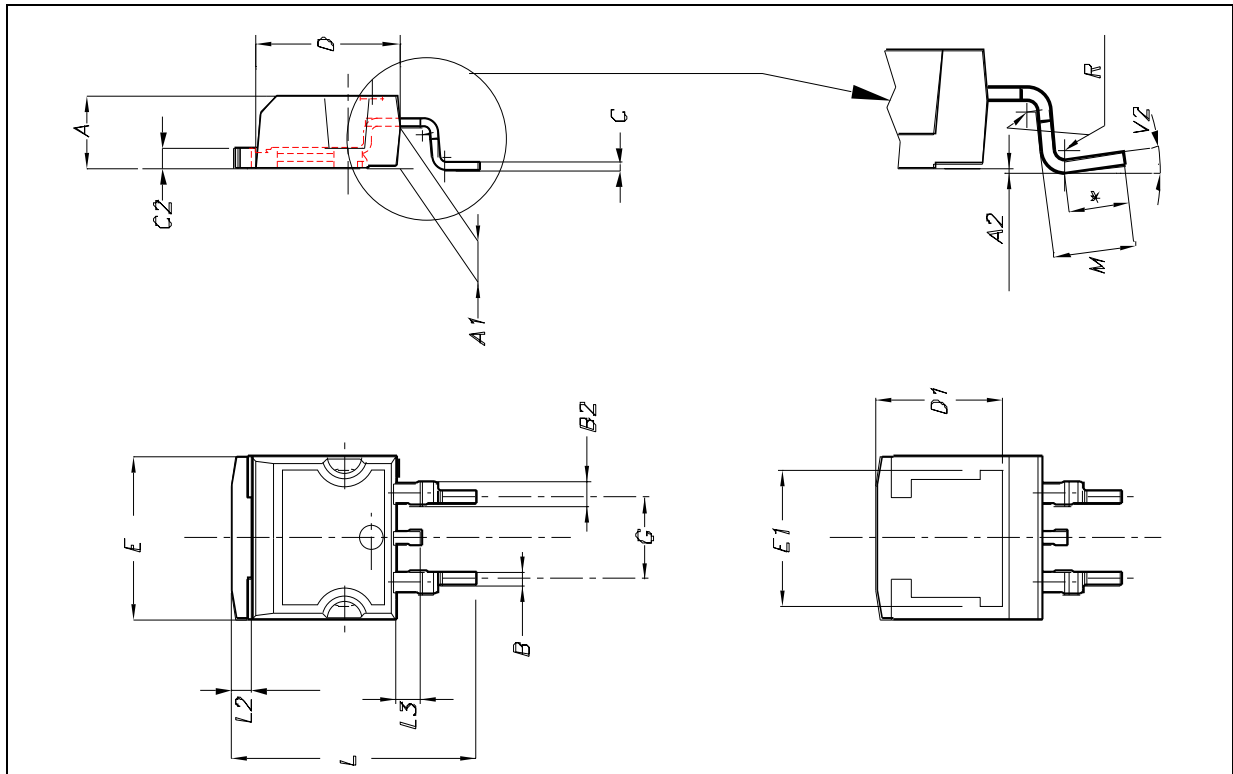


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**

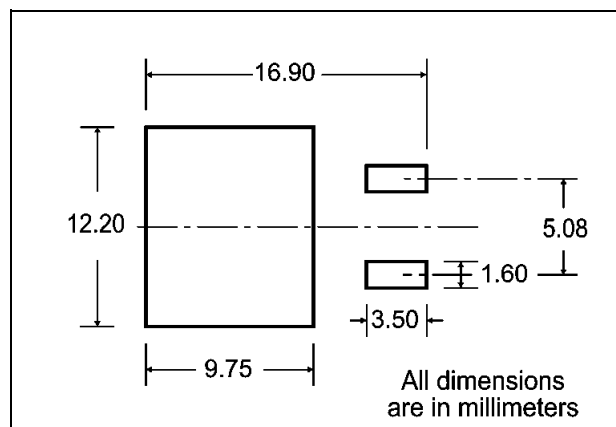


D<sup>2</sup>PAK MECHANICAL DATA

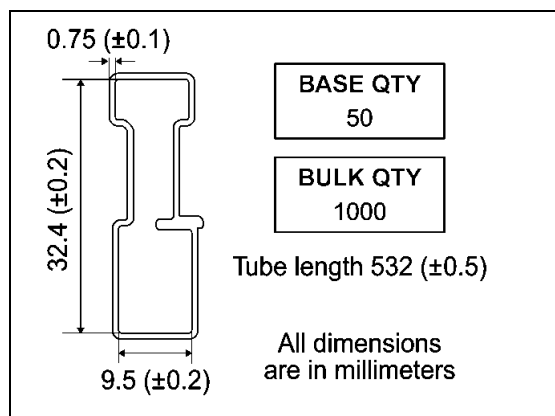
DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°



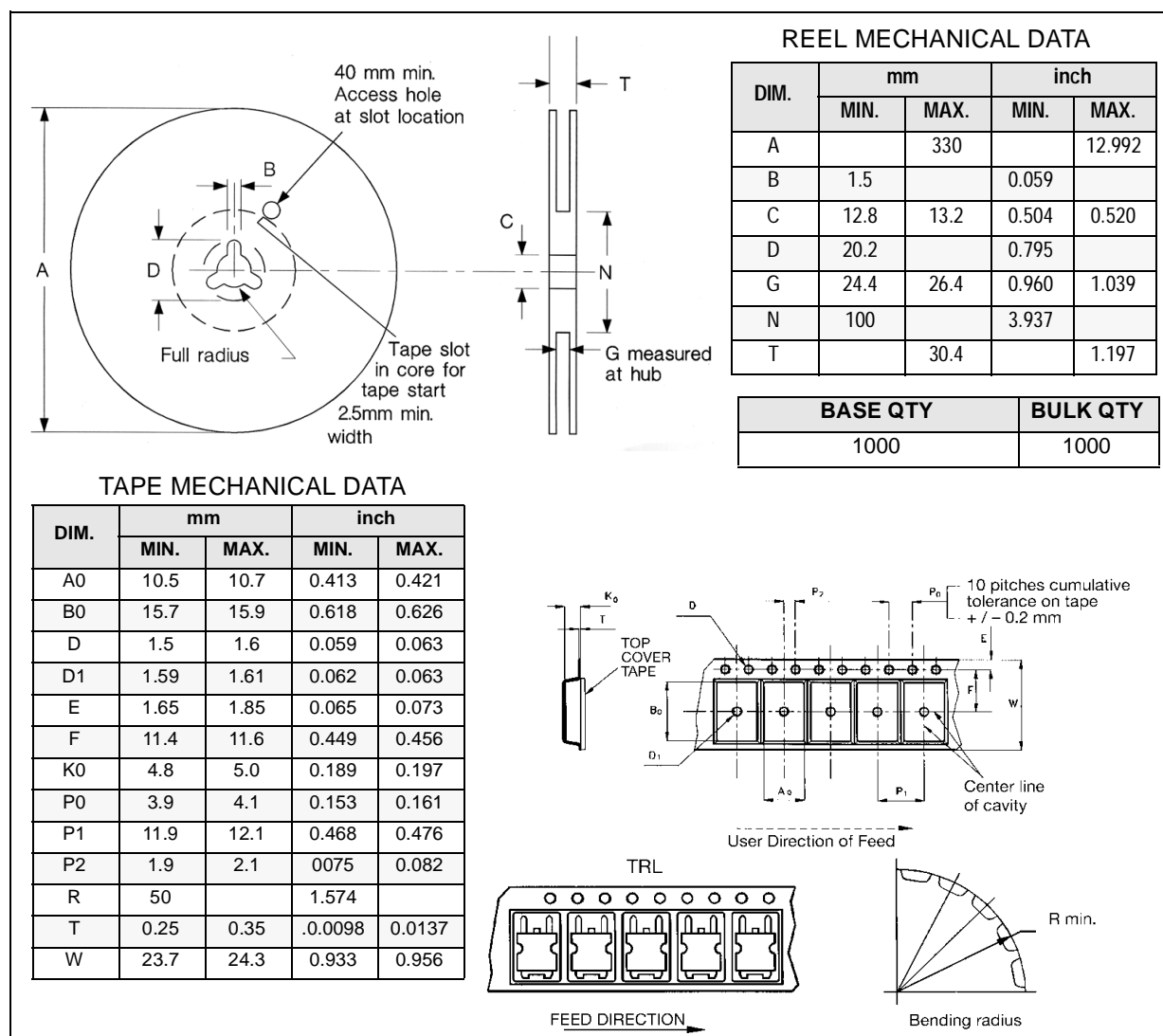
## D2PAK FOOTPRINT



**TUBE SHIPMENT (no suffix)\***



### TAPE AND REEL SHIPMENT (suffix "T4")\*

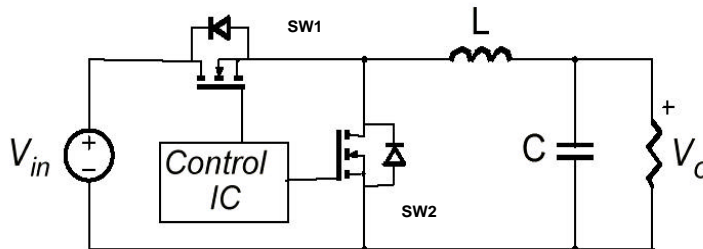


\* on sales type



## APPENDIX A

### Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gs}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW<sub>1</sub> during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
- Low  $R_{DS(on)}$  to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{\text{conduction}}$		$R_{\text{DS(on)SW1}} * I_L^2 * d$	$R_{\text{DS(on)SW2}} * I_L^2 * (1-d)$
$P_{\text{switching}}$		$V_{\text{in}} * (Q_{\text{gsth(SW1)}} + Q_{\text{gd(SW1)}}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
$P_{\text{diode}}$	Recovery	Not Applicable	$^1 V_{\text{in}} * Q_{\text{rr(SW2)}} * f$
	Conduction	Not Applicable	$V_{\text{f(SW2)}} * I_L * t_{\text{deadtime}} * f$
$P_{\text{gate(Q}_G)}$		$Q_{\text{g(SW1)}} * V_{\text{gg}} * f$	$Q_{\text{gls(SW2)}} * V_{\text{gg}} * f$
$P_{\text{Qoss}}$		$\frac{V_{\text{in}} * Q_{\text{oss(SW1)}} * f}{2}$	$\frac{V_{\text{in}} * Q_{\text{oss(SW2)}} * f}{2}$

Parameter	Meaning
d	Duty-cycle
$Q_{\text{gsth}}$	Post threshold gate charge
$Q_{\text{gls}}$	Third quadrant gate charge
<b>Pconduction</b>	On state losses
<b>Pswitching</b>	On-off transition losses
<b>Pdiode</b>	Conduction and reverse recovery diode losses
<b>Pgate</b>	Gate drive losses
<b>PQoss</b>	Output capacitance losses

<sup>1</sup> Dissipated by SW1 during turn-on

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