



STB20PF75

P-CHANNEL 75V - 0.10 Ω - 20A D²PAK

STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB20PF75	75 V	< 0.12 Ω	20 A

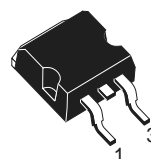
- TYPICAL R_{DS(on)} = 0.10 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

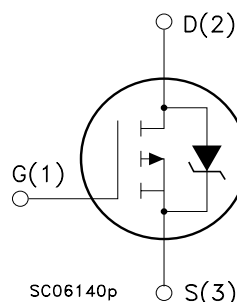
- MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS



**D²PAK
TO-263**
(Suffix "T4")

ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	75	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	75	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	20	A
I _D	Drain Current (continuous) at T _C = 100°C	14	A
I _{DM} (●)	Drain Current (pulsed)	80	A
P _{tot}	Total Dissipation at T _C = 25°C	80	W
	Derating Factor	0.53	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	10	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	350	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1) I_{SD} \leq 20A, di/dt \leq 200A/ μ s, V_{DD} \leq V_{(BR)DSS}, T_j \leq T_{JMAX}

(2) Starting T_j = 25 °C, I_D = 10 A, V_{DD} = 30V

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	1.88	°C/W
R _{thj-PCB}	Thermal Resistance Junction-PCB	Max	34	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose (1.6 mm from case, for 10 sec)	Typ	300	°C

(*) When Mounted on 1 inch² FR-4 board, 2 oz of Cu

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	75			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 µA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 10 A		0.10	0.12	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs}	Forward Transconductance	V _{DS} = 15 V I _D = 10 A		15		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1150 170 70		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON (*)**

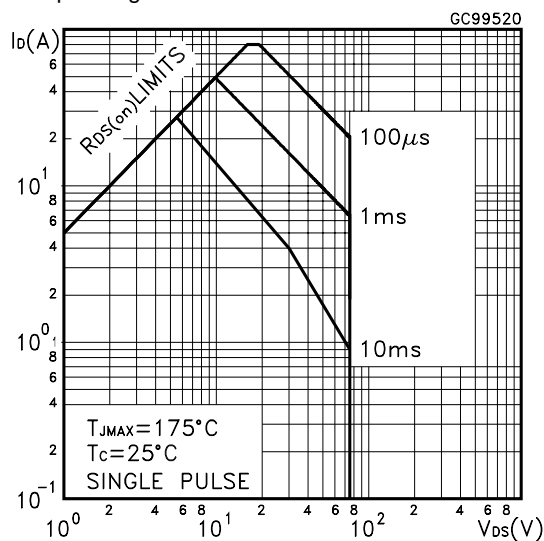
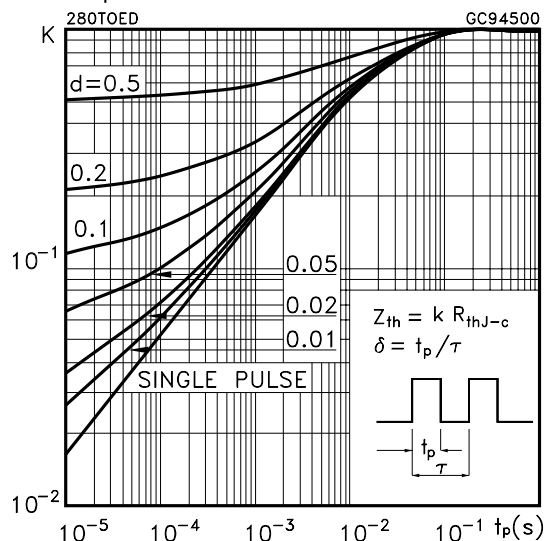
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 37.5\text{ V}$ $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		20 51		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=60\text{V}$ $I_D=20\text{A}$ $V_{GS}=10\text{V}$ (See test circuit, Figure 2)		38 7 10	52	nC nC nC

SWITCHING OFF (*)

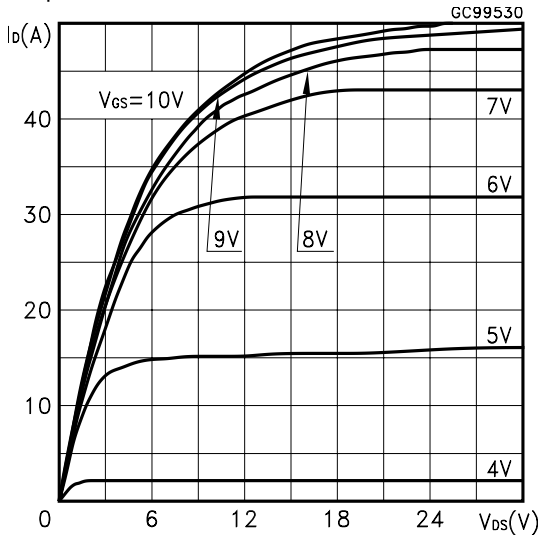
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 60\text{ V}$ $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 1)		40 13		ns ns

SOURCE DRAIN DIODE (*)

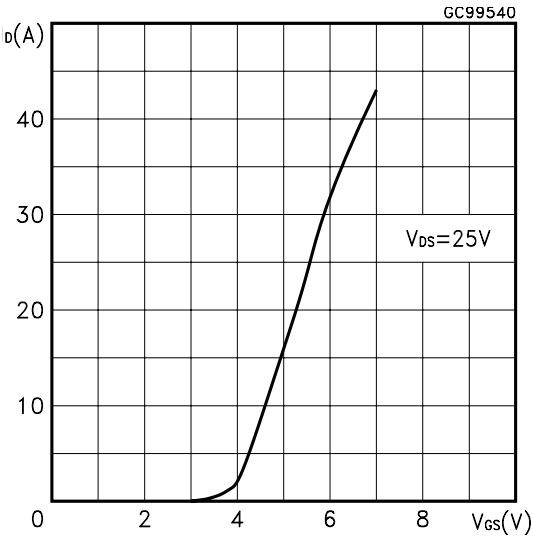
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (*)$	Source-drain Current Source-drain Current (pulsed)				20 80	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 20\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		80 250 6.2		ns nC A

(*) Pulse width $\leq 300\ \mu\text{s}$, duty cycle 1.5 %.(*) Pulse width limited by T_{JMAX} **Safe Operating Area****Thermal Impedance**

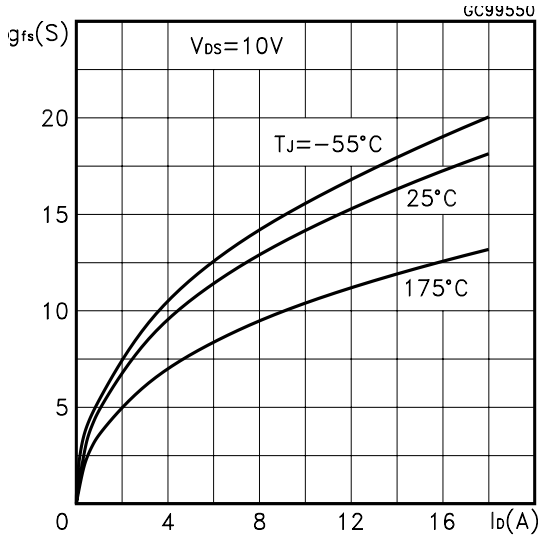
Output Characteristics



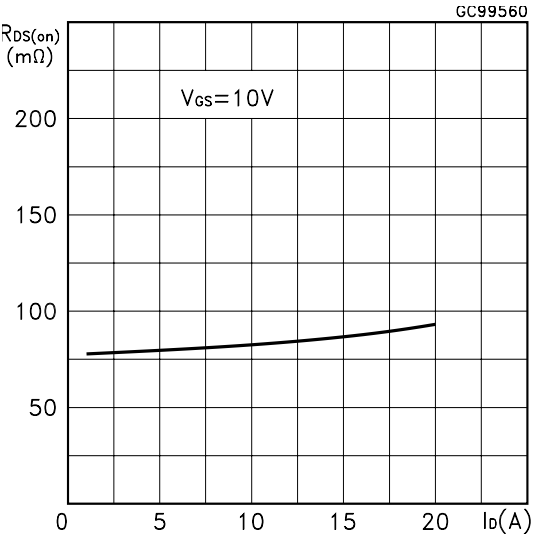
Transfer Characteristics



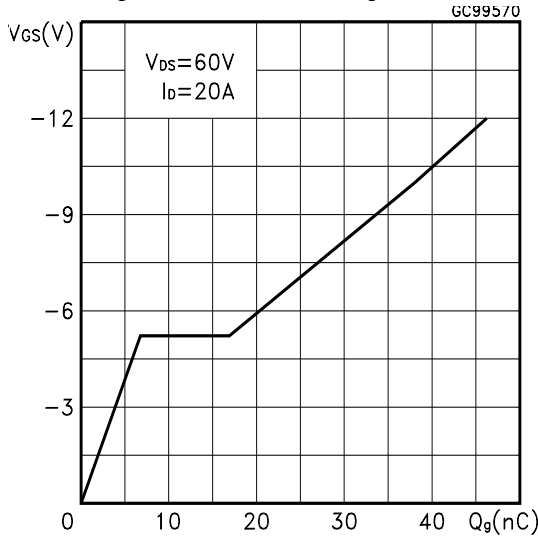
Transconductance



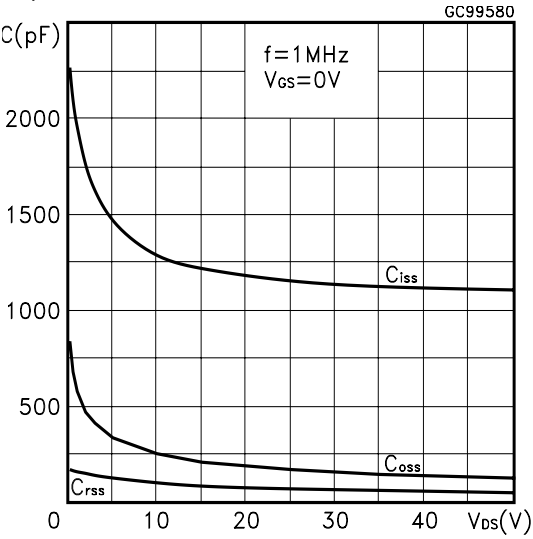
Static Drain-source On Resistance



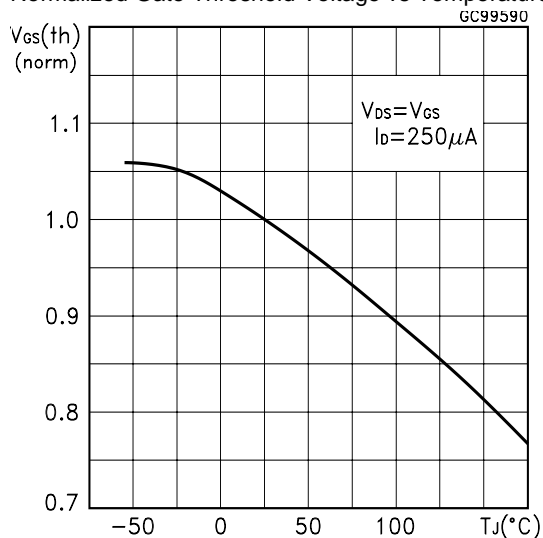
Gate Charge vs Gate-source Voltage



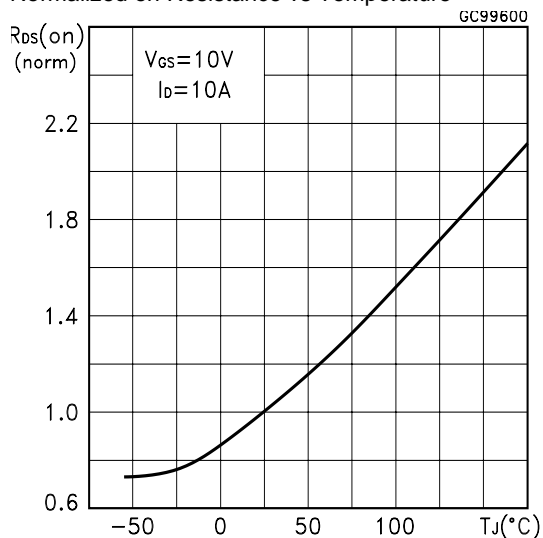
Capacitance Variations



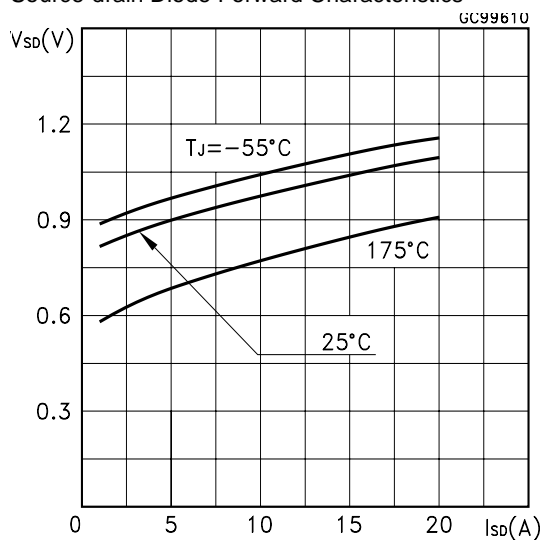
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

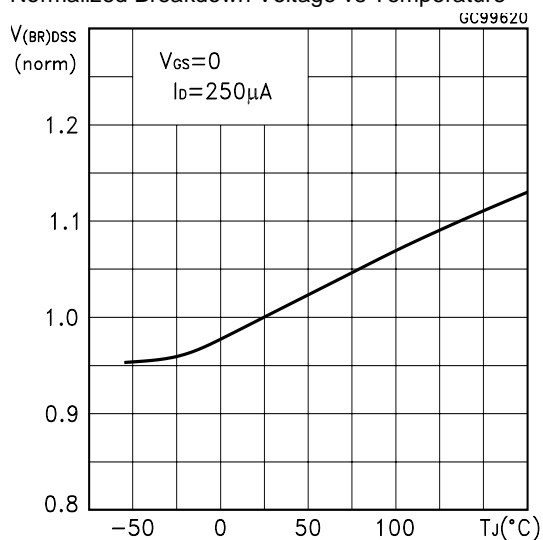


Fig. 1: Switching Times Test Circuits For Resistive Load

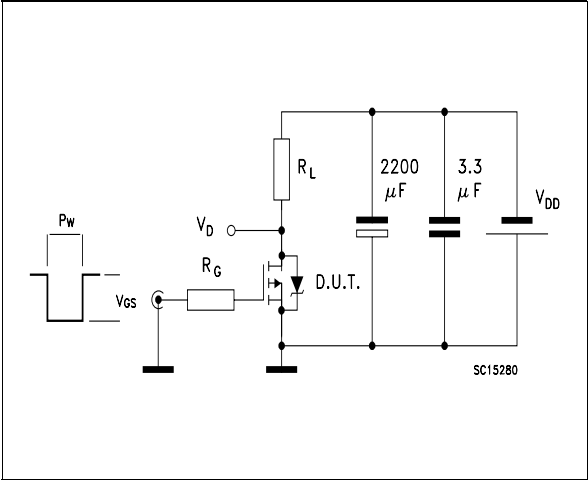


Fig. 2: Gate Charge test Circuit

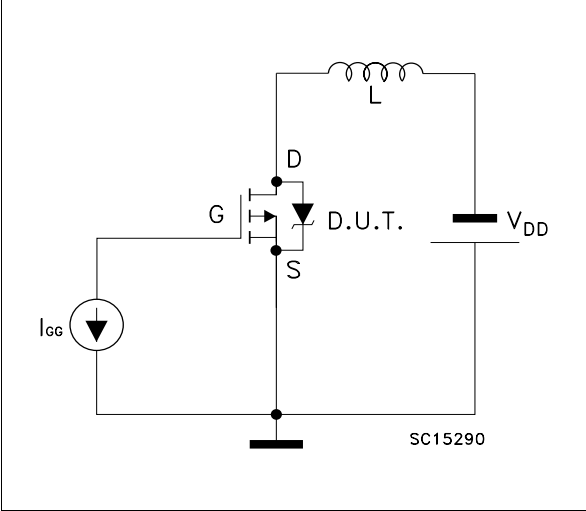
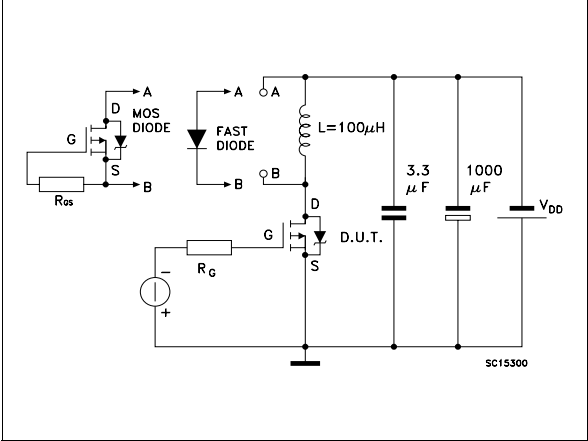
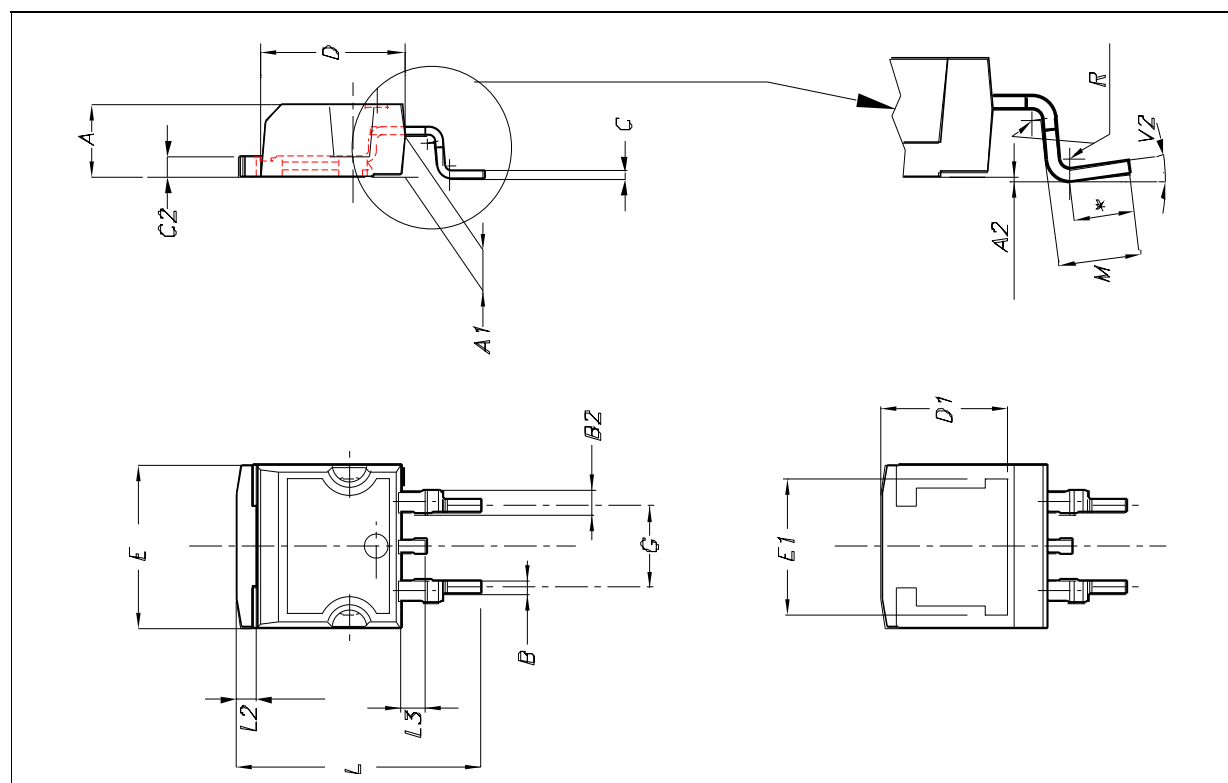


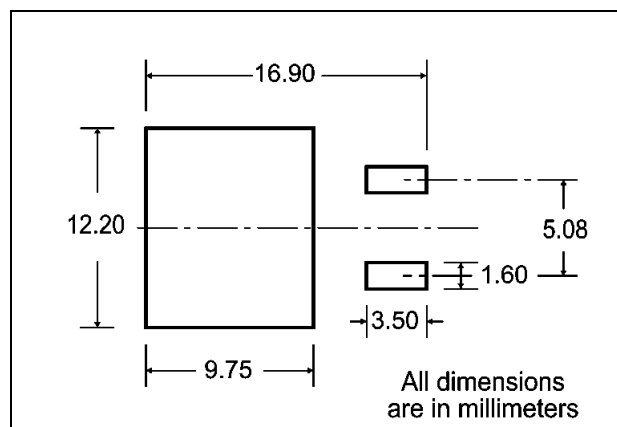
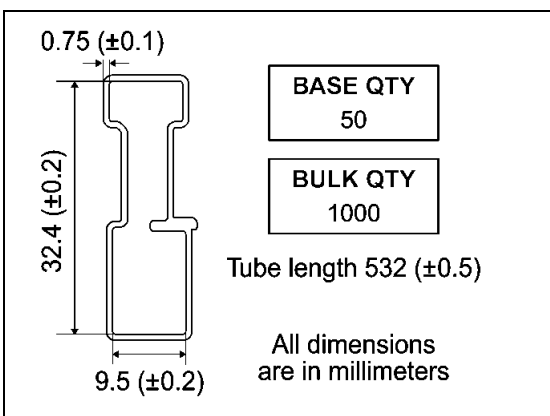
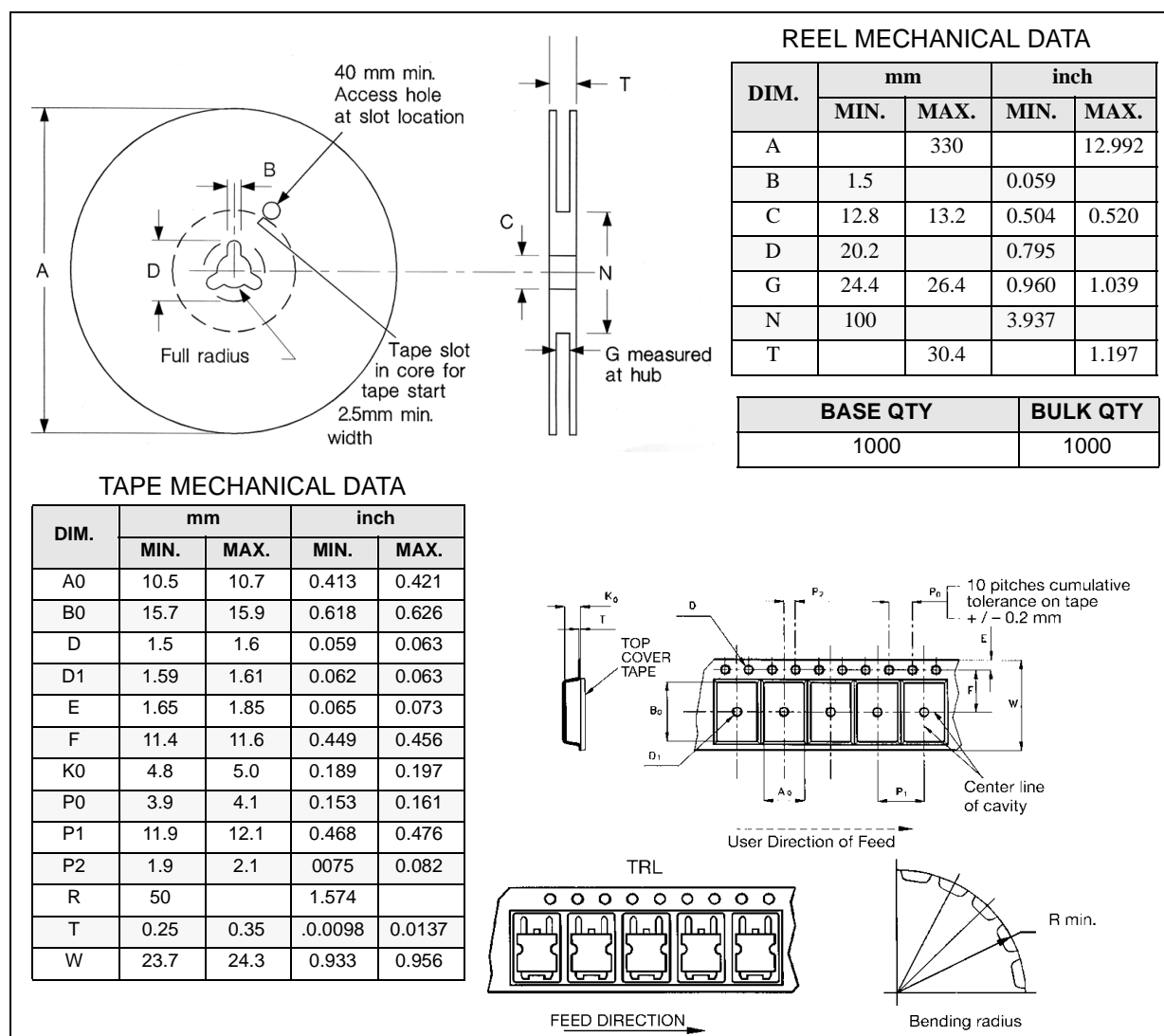
Fig. 3: Test Circuit For Diode Recovery Behaviour



D²PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°



D2PAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type

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