



## STB40NS15

N-CHANNEL 150V - 0.042Ω - 40A D<sup>2</sup>PAK

MESH OVERLAY™ MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB40NS15	150 V	<0.052Ω	40A

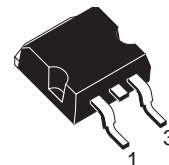
- TYPICAL R<sub>DS(on)</sub> = 0.042Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

### DESCRIPTION

This powermos MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

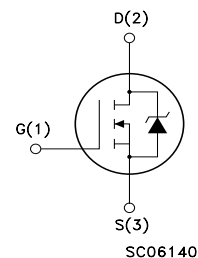
### APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- PRIMARY SWITCH IN ISOLATED DC-DC CONVERTERS



D<sup>2</sup>PAK

### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	150	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	150	V
V <sub>GS</sub>	Gate- source Voltage	±20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	40	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	25	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	160	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	140	W
	Derating Factor	0.933	W/°C
dv/dt	Peak Diode Recovery voltage slope	9	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(•)Pulse width limited by safe operating area

## STB40NS15

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.07	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	40	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	500	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 µA, V <sub>GS</sub> = 0	150			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	µA µA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V			±100	nA

#### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 40 A		0.044	0.052	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)</sub> max, I <sub>D</sub> = 20A		20		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		2400		pF
C <sub>oss</sub>	Output Capacitance			380		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			160		pF

## ELECTRICAL CHARACTERISTICS (CONTINUED)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 75V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		25		ns
$t_r$	Rise Time			45		ns
$Q_g$	Total Gate Charge	$V_{DD} = 120V, I_D = 40A,$ $V_{GS} = 10V$		100	110	nC
$Q_{gs}$	Gate-Source Charge			17		nC
$Q_{gd}$	Gate-Drain Charge			47		nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 75V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		85		ns
$T_f$	Fall Time					
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{clamp} = 120V, I_D = 20A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		47		ns
$t_f$	Fall Time			35		ns
$t_c$	Cross-over Time			70		ns

## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				40	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				160	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 40A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 40A, di/dt = 100A/\mu s,$ $V_{DD} = 50V, T_j = 150^\circ C$ (see test circuit, Figure 5)		270		ns
$Q_{rr}$	Reverse Recovery Charge			200		nC
$I_{RRM}$	Reverse Recovery Current			1.5		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

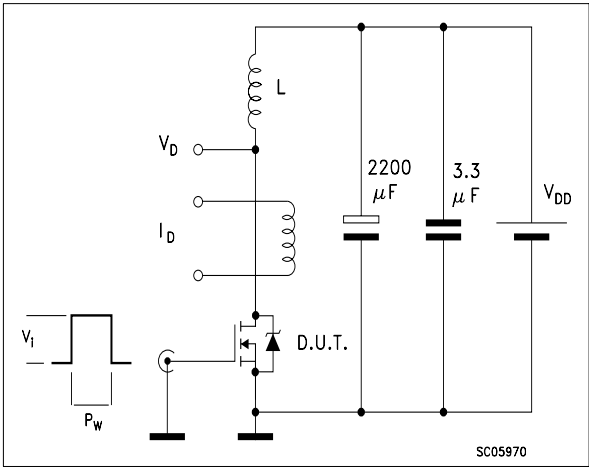


Fig. 2: Unclamped Inductive Waveform

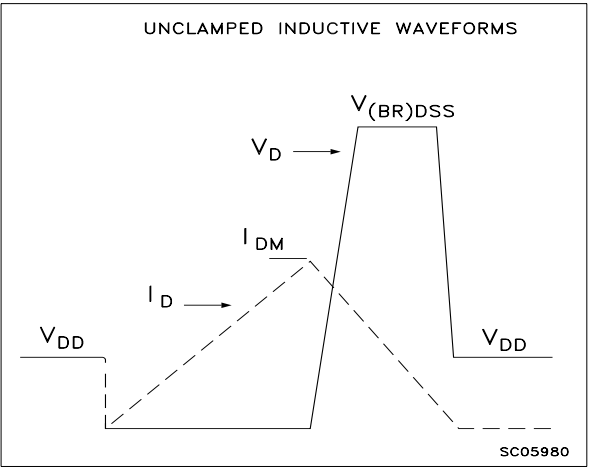


Fig. 3: Switching Times Test Circuit For Resistive Load

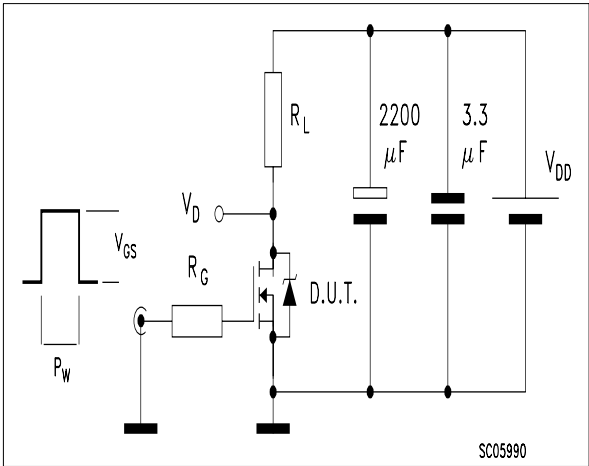


Fig. 4: Gate Charge test Circuit

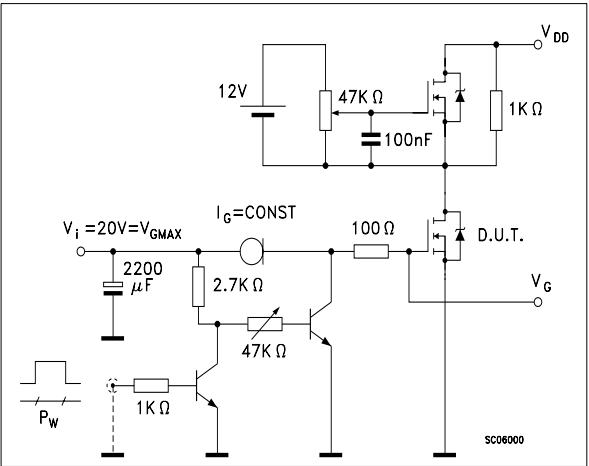
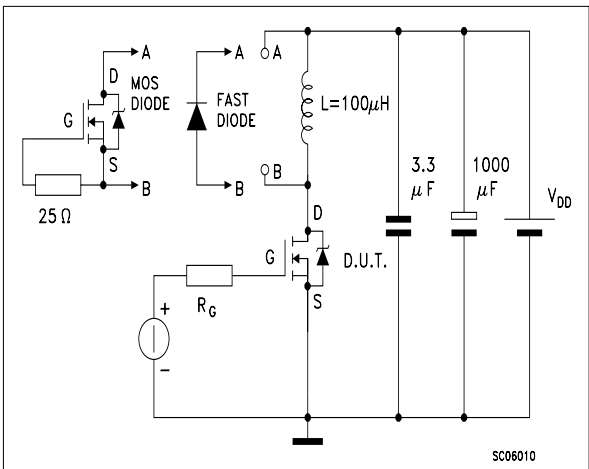
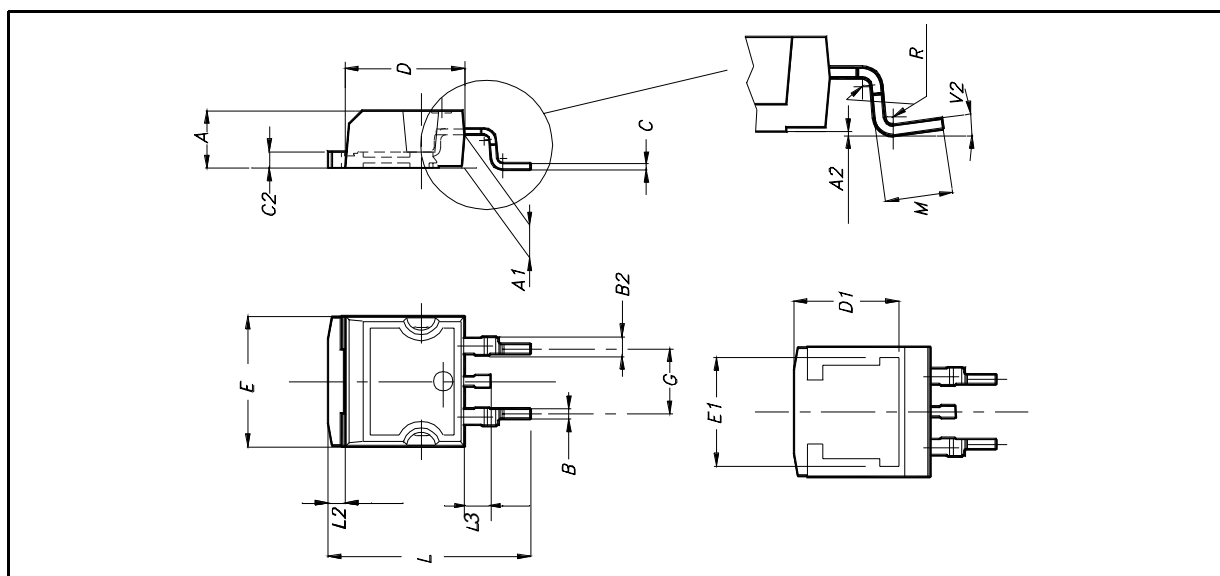


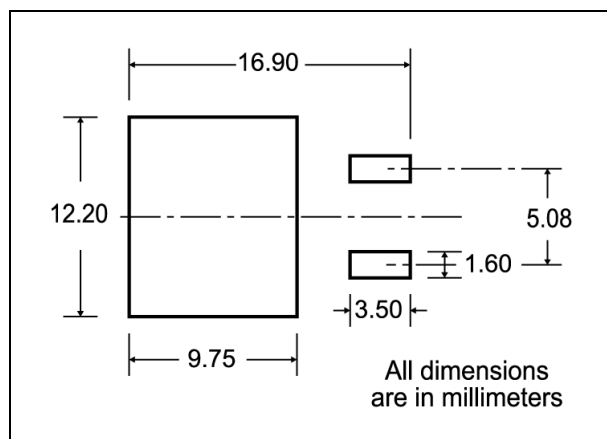
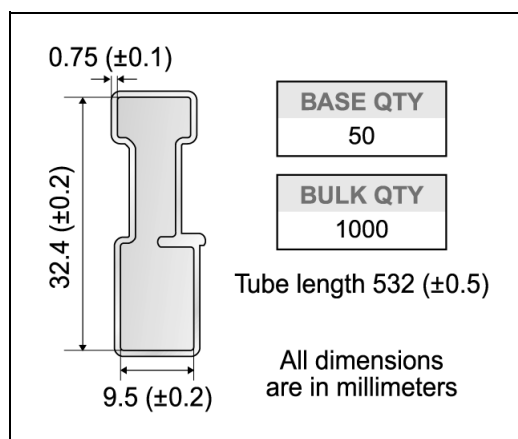
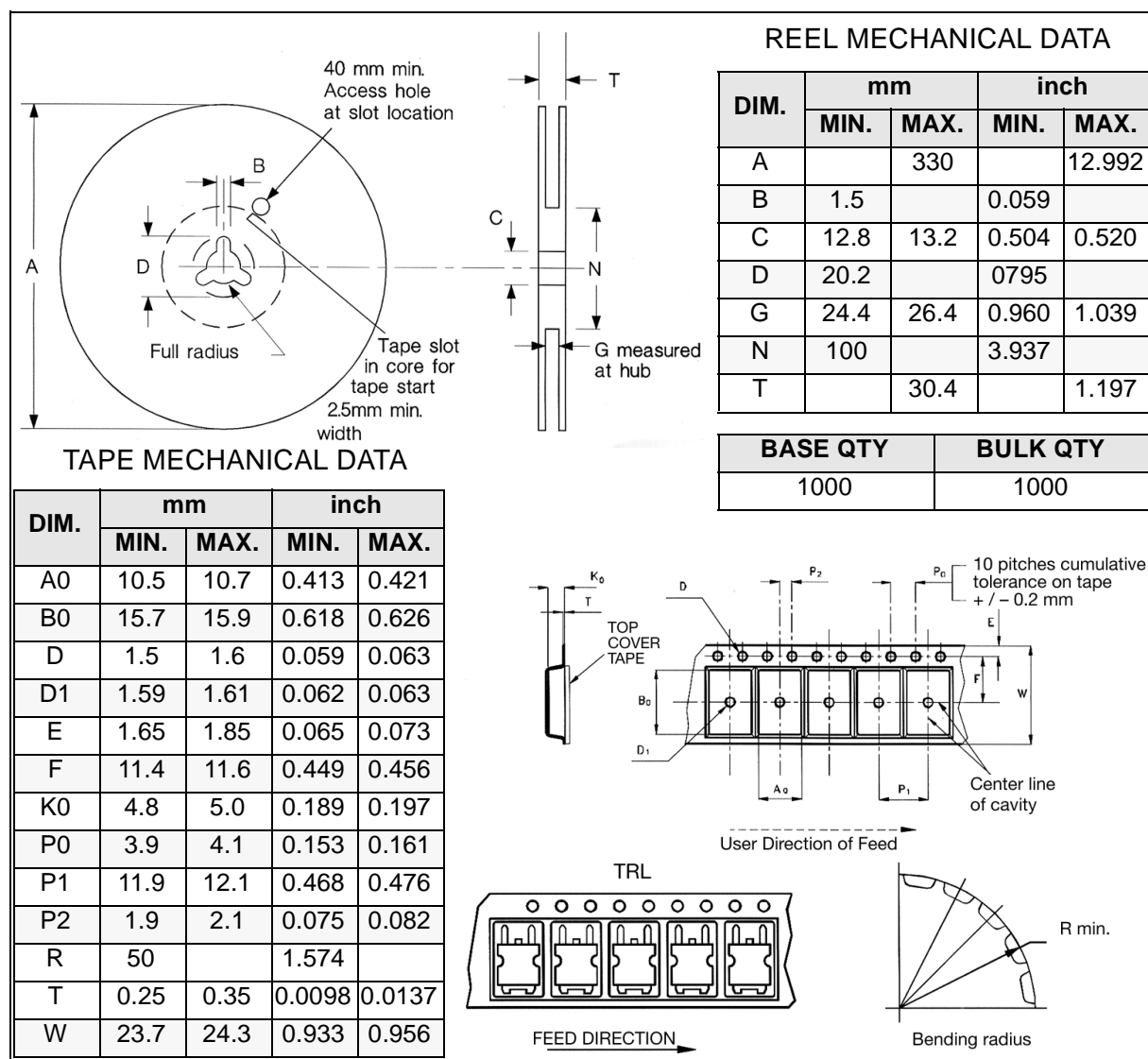
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



## D<sup>2</sup>PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



**D<sup>2</sup>PAK FOOTPRINT****TUBE SHIPMENT (no suffix)\*****TAPE AND REEL SHIPMENT (suffix "T4")\***

\* on sales type

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