



STB8NS25

N-CHANNEL 250V - 0.38Ω - 8A D²PAK MESH OVERLAY™ MOSFET

| TYPE | V _{DSS} | R _{DS(on)} | I _D |
|----------|------------------|---------------------|----------------|
| STB8NS25 | 250 V | < 0.45 Ω | 8 A |

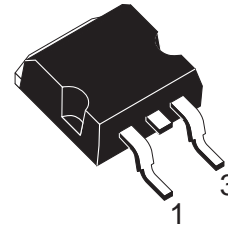
- TYPICAL R_{DS(on)} = 0.38 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performance. The new patented STrip layout coupled with the Company's proprietary edge termination structure, makes it suitable in converters for lighting applications.

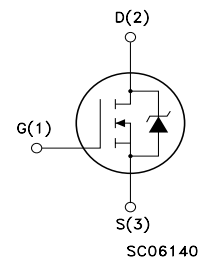
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-DC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT



D²PAK

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------------|--|------------|------|
| V _{DS} | Drain-source Voltage (V _{GS} = 0) | 250 | V |
| V _{DGR} | Drain-gate Voltage (R _{GS} = 20 kΩ) | 250 | V |
| V _{GS} | Gate- source Voltage | ± 20 | V |
| I _D (*) | Drain Current (continuous) at T _C = 25°C | 8 | A |
| I _D | Drain Current (continuous) at T _C = 100°C | 5 | A |
| I _{DM} (•) | Drain Current (pulsed) | 32 | A |
| P _{TOT} | Total Dissipation at T _C = 25°C | 80 | W |
| | Derating Factor | 0.64 | W/°C |
| dv/dt (1) | Peak Diode Recovery voltage slope | 5 | V/ns |
| T _{stg} | Storage Temperature | -65 to 150 | °C |
| T _j | Max. Operating Junction Temperature | 150 | °C |

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 8A, di/dt ≤ 300 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{jMAX}

(*) Limited only by maximum temperature allowed

STB8NS25

THERMAL DATA

| | | | |
|----------------|--|------|------|
| Rthj-case | Thermal Resistance Junction-case Max | 1.56 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 62.5 | °C/W |
| T _I | Maximum Lead Temperature For Soldering Purpose | 300 | °C |

AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|-----------------|--|-----------|------|
| I _{AR} | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max) | 8 | A |
| E _{AS} | Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V) | 300 | mJ |

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|------|---------|----------|
| V _{(BR)DSS} | Drain-source Breakdown Voltage | I _D = 250 µA, V _{GS} = 0 | 250 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current (V _{GS} = 0) | V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C | | | 1 10 | µA µA |
| I _{GSS} | Gate-body Leakage Current (V _{DS} = 0) | V _{GS} = ±20V | | | ±100 | nA |

ON (1)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|--|------|------|------|------|
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} , I _D = 250µA | 2 | 3 | 4 | V |
| R _{DS(on)} | Static Drain-source On Resistance | V _{GS} = 10V, I _D = 4 A | | 0.38 | 0.45 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------|--|------|------|------|------|
| g _{fs} (1) | Forward Transconductance | V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 4A | 7 | 8 | | S |
| C _{iss} | Input Capacitance | V _{DS} = 25V, f = 1 MHz, V _{GS} = 0 | | 770 | | pF |
| C _{oss} | Output Capacitance | | | 118 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 48 | | pF |

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------|--------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD} = 125\text{ V}$, $I_D = 4\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3) | | 13 | | ns |
| t_r | Rise Time | | | 18 | | ns |
| Q_g | Total Gate Charge | $V_{DD} = 200\text{ V}$, $I_D = 8\text{ A}$, $V_{GS} = 10\text{ V}$ | | 37 | 51.8 | nC |
| Q_{gs} | Gate-Source Charge | | | 5.2 | | nC |
| Q_{gd} | Gate-Drain Charge | | | 14.8 | | nC |

SWITCHING OFF

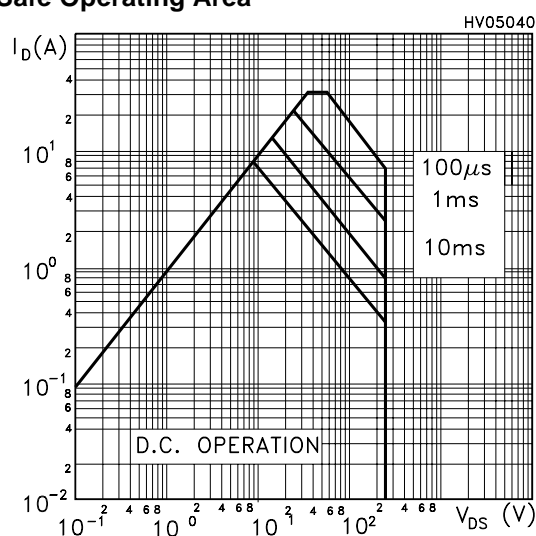
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------|---|------|------|------|------|
| $t_{d(Voff)}$ | Turn-off Delay Time | $V_{DD} = 125\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3) | | 51 | | ns |
| t_f | Fall Time | | | 16 | | ns |
| $t_{r(Voff)}$ | Off-voltage Rise Time | $V_{clamp} = 200\text{ V}$, $I_D = 8\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5) | | 12.5 | | ns |
| t_f | Fall Time | | | 12.5 | | ns |
| t_c | Cross-over Time | | | 28 | | ns |

SOURCE DRAIN DIODE

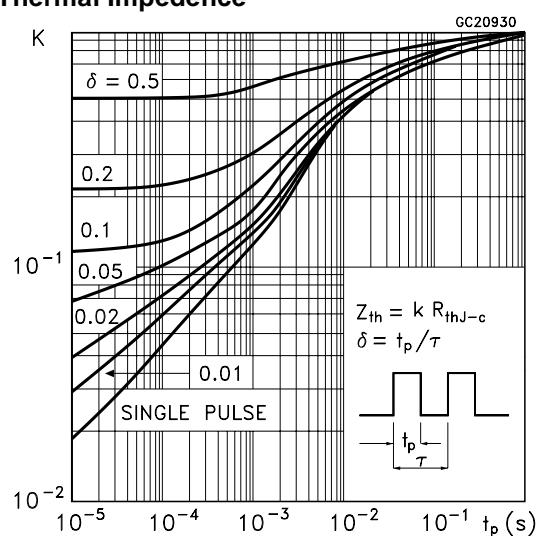
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain Current | | | | 8 | A |
| $I_{SDM(2)}$ | Source-drain Current (pulsed) | | | | 32 | A |
| $V_{SD(1)}$ | Forward On Voltage | $I_{SD} = 8\text{ A}$, $V_{GS} = 0$ | | | 1.7 | V |
| t_{rr} | Reverse Recovery Time | $I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$, $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5) | | 198 | | ns |
| Q_{rr} | Reverse Recovery Charge | | | 1.1 | | μC |
| I_{RRM} | Reverse Recovery Current | | | 11.3 | | A |

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

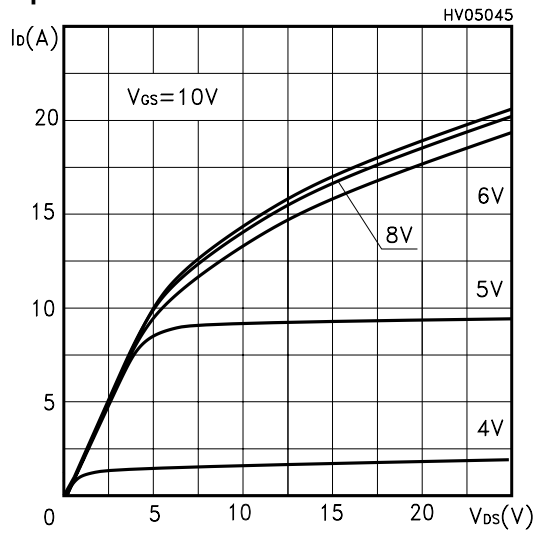
Safe Operating Area



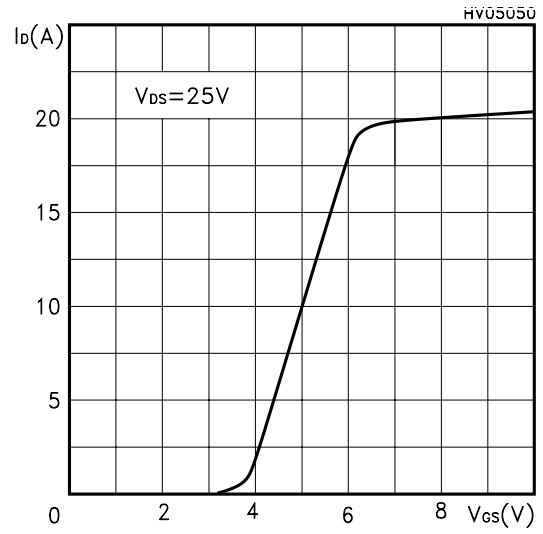
Thermal Impedance



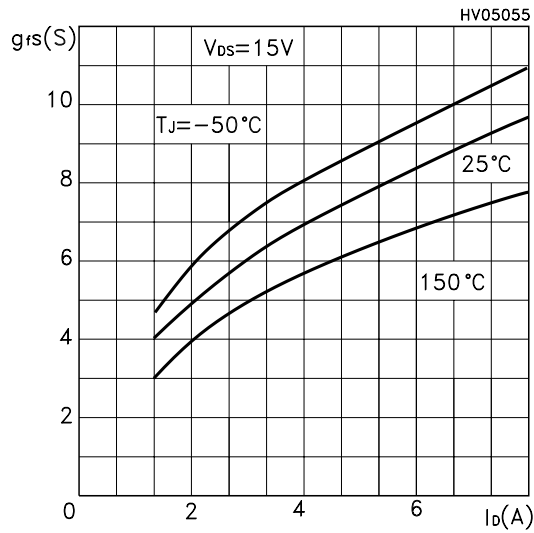
Output Characteristics



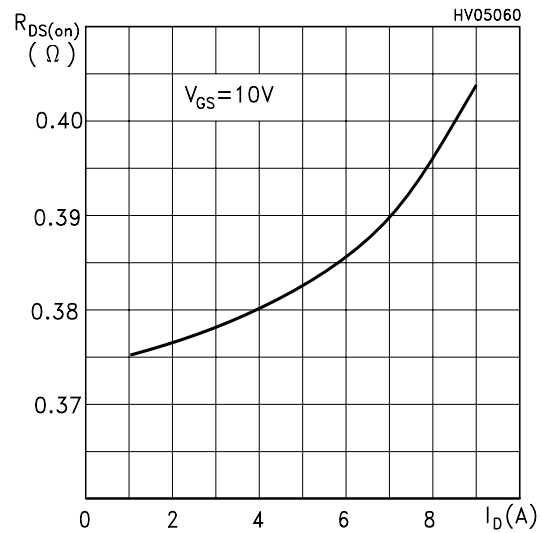
Transfer Characteristics



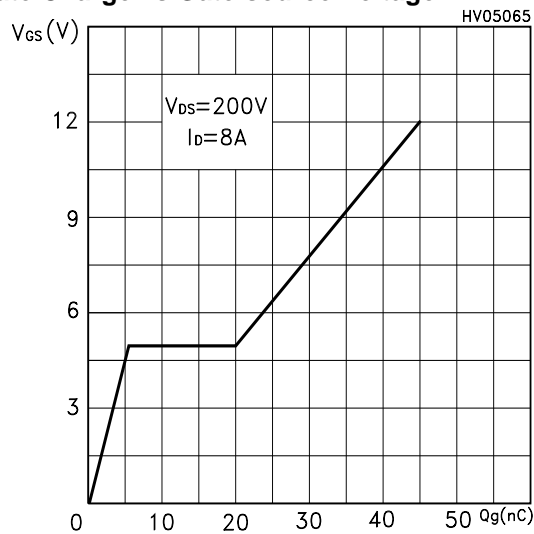
Transconductance



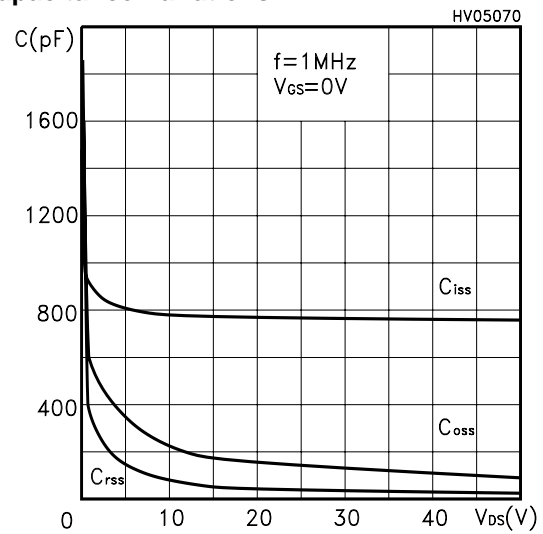
Static Drain-source On Resistance



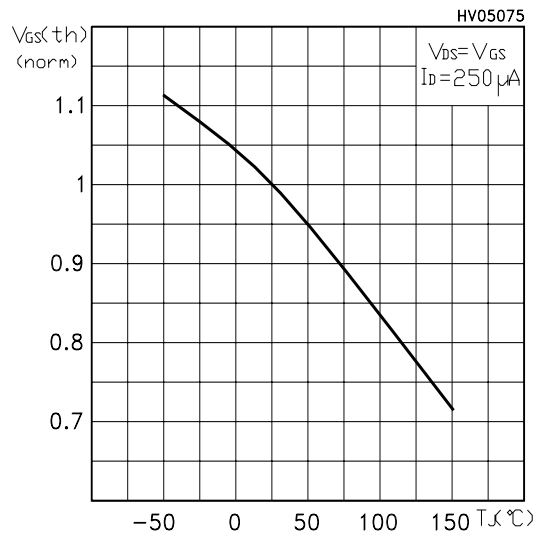
Gate Charge vs Gate-source Voltage



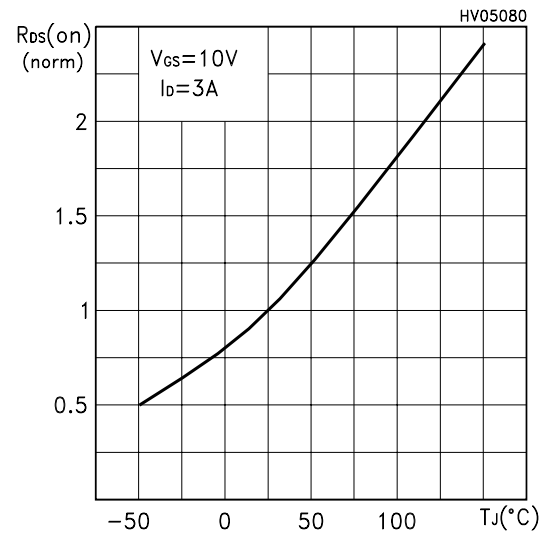
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

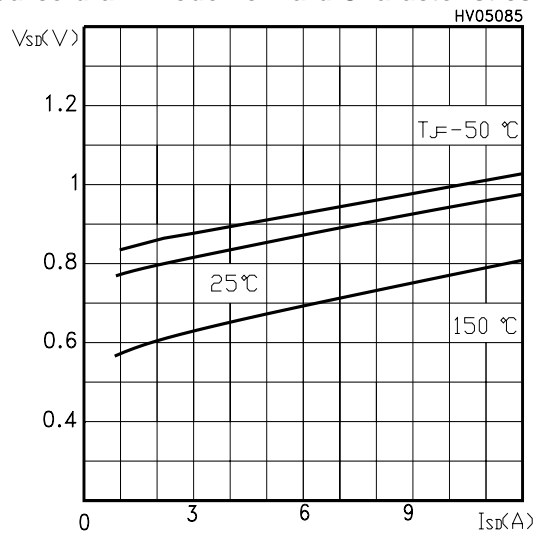


Fig. 1: Unclamped Inductive Load Test Circuit

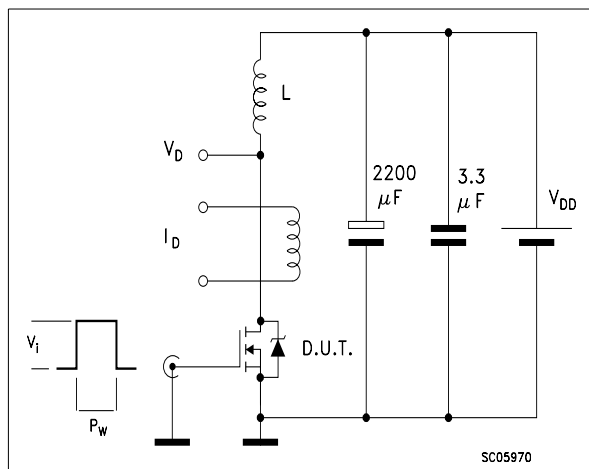


Fig. 2: Unclamped Inductive Waveform

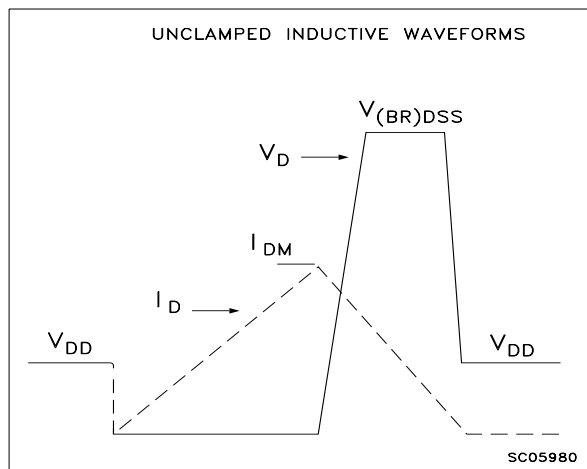


Fig. 3: Switching Times Test Circuit For Resistive Load

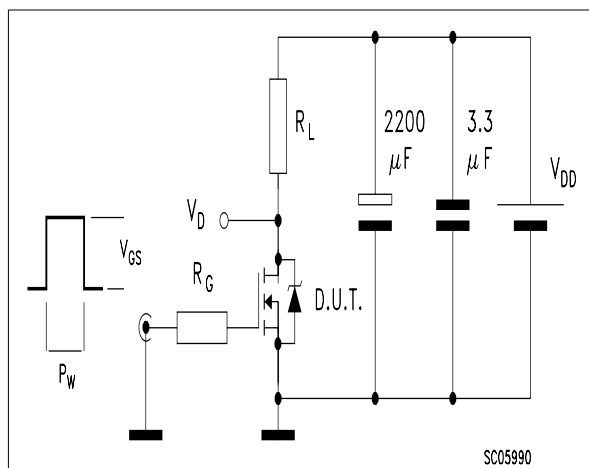


Fig. 4: Gate Charge test Circuit

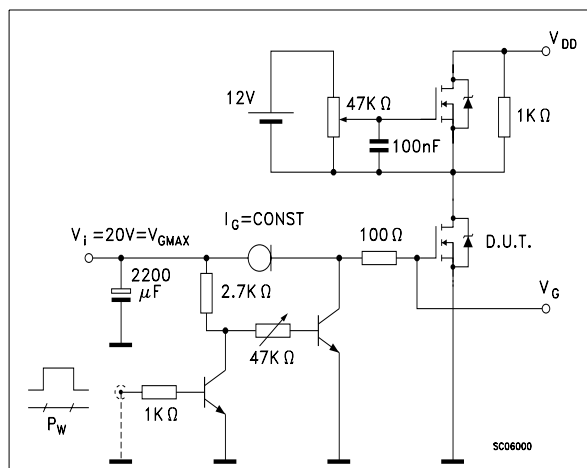
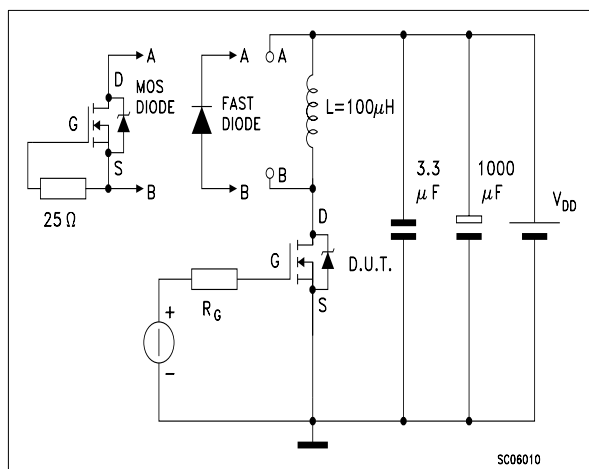
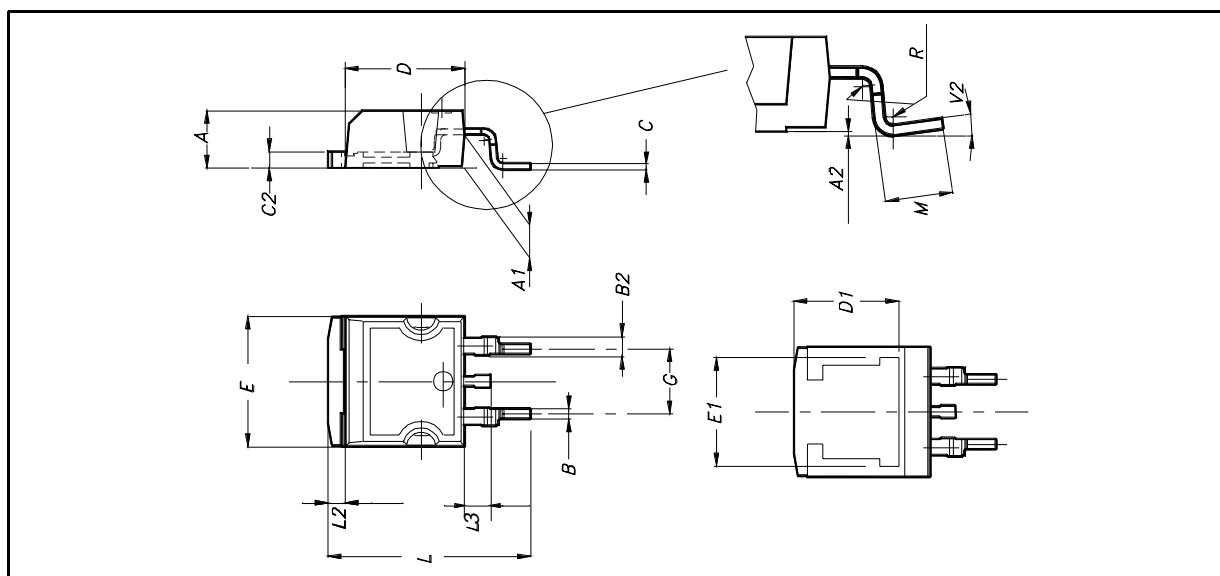


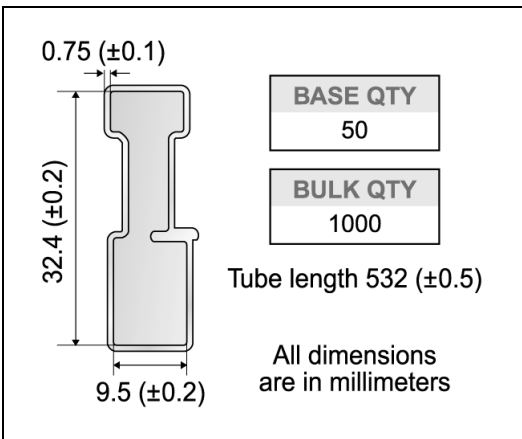
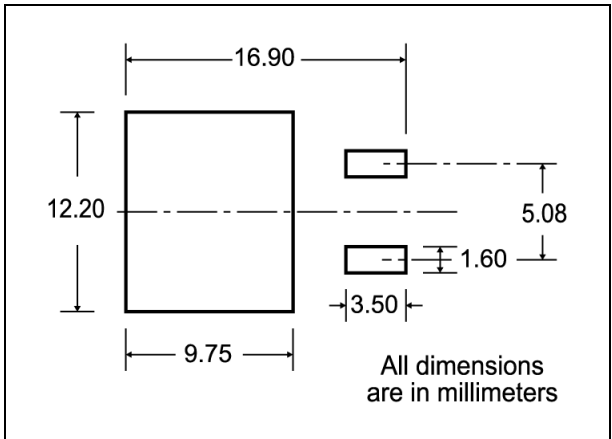
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



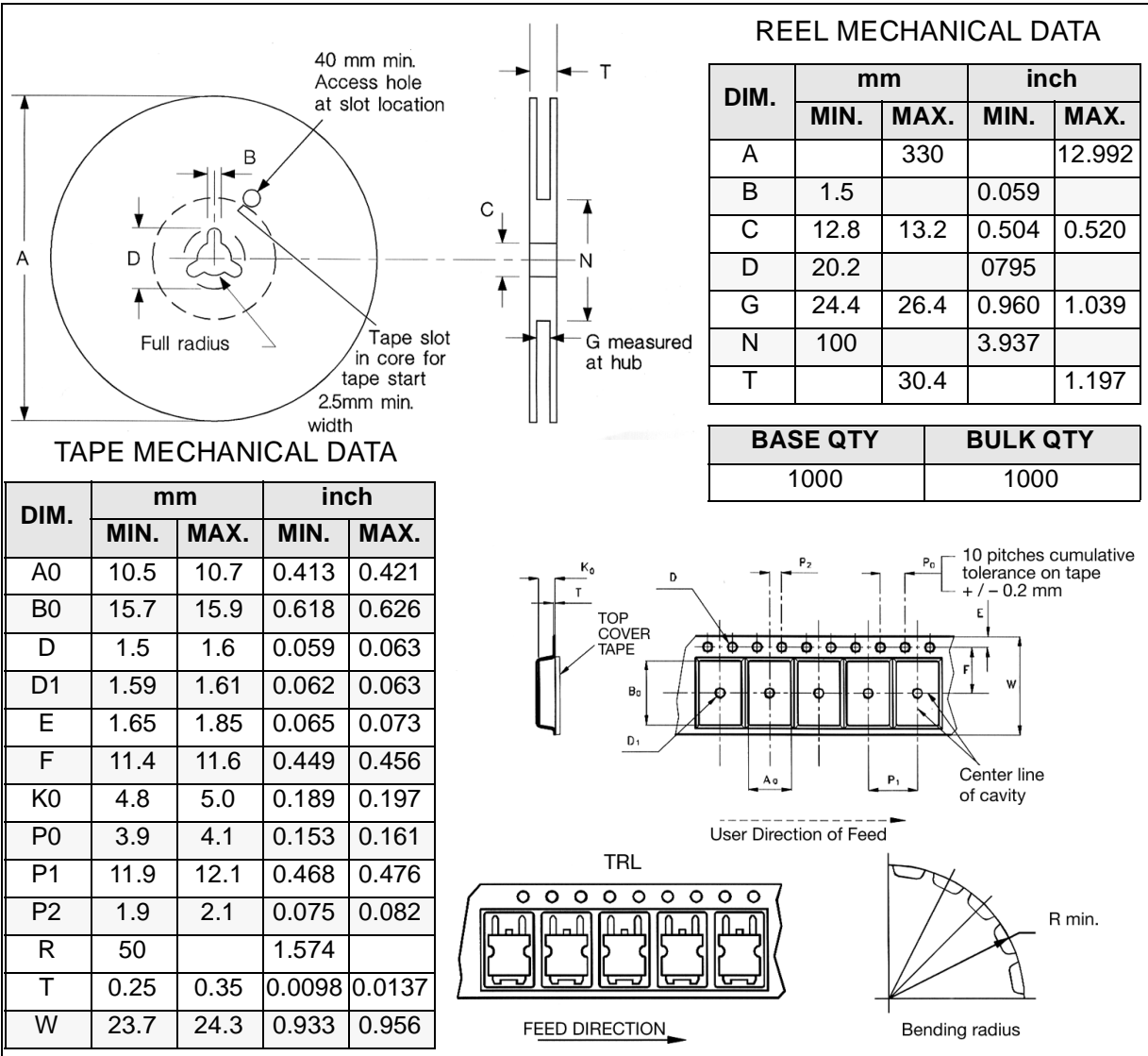
D²PAK MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|-------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.4 | | 4.6 | 0.173 | | 0.181 |
| A1 | 2.49 | | 2.69 | 0.098 | | 0.106 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.7 | | 0.93 | 0.027 | | 0.036 |
| B2 | 1.14 | | 1.7 | 0.044 | | 0.067 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 1.23 | | 1.36 | 0.048 | | 0.053 |
| D | 8.95 | | 9.35 | 0.352 | | 0.368 |
| D1 | | 8 | | | 0.315 | |
| E | 10 | | 10.4 | 0.393 | | |
| E1 | | 8.5 | | | 0.334 | |
| G | 4.88 | | 5.28 | 0.192 | | 0.208 |
| L | 15 | | 15.85 | 0.590 | | 0.625 |
| L2 | 1.27 | | 1.4 | 0.050 | | 0.055 |
| L3 | 1.4 | | 1.75 | 0.055 | | 0.068 |
| M | 2.4 | | 3.2 | 0.094 | | 0.126 |
| R | | 0.4 | | | 0.015 | |
| V2 | 0° | | 8° | | | |





TAPE AND REEL SHIPMENT (suffix "T4")*



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