



## STD12N10L

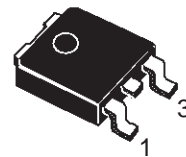
### N - CHANNEL 100V - 0.12 $\Omega$ - 12A TO-252 LOW THRESHOLD POWER MOS TRANSISTOR

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD12N10L	100 V	< 0.15 $\Omega$	12 A

- TYPICAL R<sub>DS(on)</sub> = 0.12  $\Omega$
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- HIGH CURRENT CAPABILITY
- 175 °C OPERATING TEMPERATURE
- LOW THRESHOLD DRIVE
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

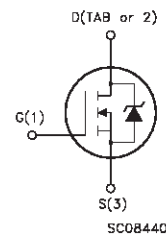
#### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE ENVIRONMENT(INJECTION, ABS, AIR-BG, LAMPDRIVERS, Etc.)



**DPAK  
TO-252**  
(Suffix "T4")

#### INTERNAL SCHEMATIC DIAGRAM



#### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100	V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	100	V
V <sub>GS</sub>	Gate-source Voltage	$\pm 15$	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	12	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	8	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	48	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	50	W
	Derating Factor	0.33	W/°C
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

## STD12N10L

### THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	3	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	100	$^{\circ}C/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	1.5	$^{\circ}C/W$
$T_I$	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}C$ unless otherwise specified)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 15 V$			$\pm 100$	nA

#### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 6 A$ $V_{GS} = 5V$ $I_D = 6 A$		0.12 0.17	0.15 0.2	$\Omega$ $\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	12			A

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 6 A$	6.5	10		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		800 150 50		pF pF pF

**ELECTRICAL CHARACTERISTICS** (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 6\text{ A}$		15		ns
$t_r$	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, see fig. 3)		40		ns
$Q_g$	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 12\text{ A}$ $V_{GS} = 5\text{ V}$		20	30	nC
$Q_{gs}$	Gate-Source Charge			6		nC
$Q_{gd}$	Gate-Drain Charge			10		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 12\text{ A}$		12		ns
$t_f$	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$		12		ns
$t_c$	Cross-over Time	(Inductive Load, see fig. 5)		25		ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				12	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				48	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 12\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 12\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		145		ns
$Q_{rr}$	Reverse Recovery Charge			580		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			8		A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

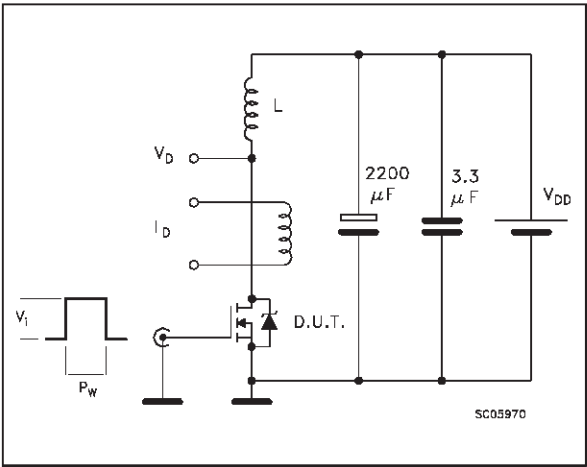


Fig. 2: Unclamped Inductive Waveform

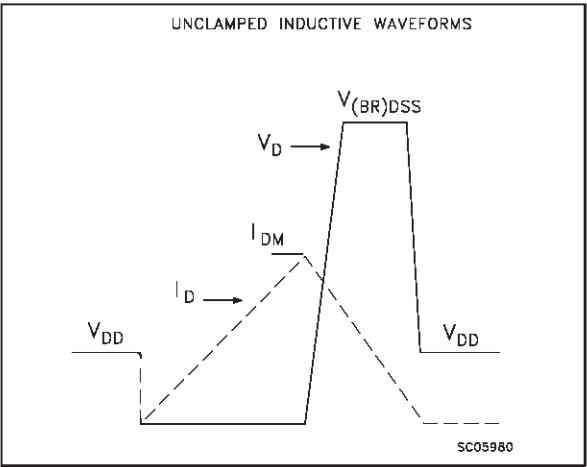


Fig. 3: Switching Times Test Circuits For Resistive Load

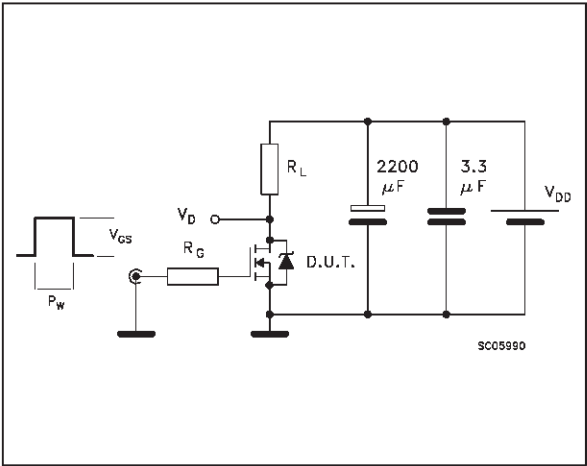


Fig. 4: Gate Charge test Circuit

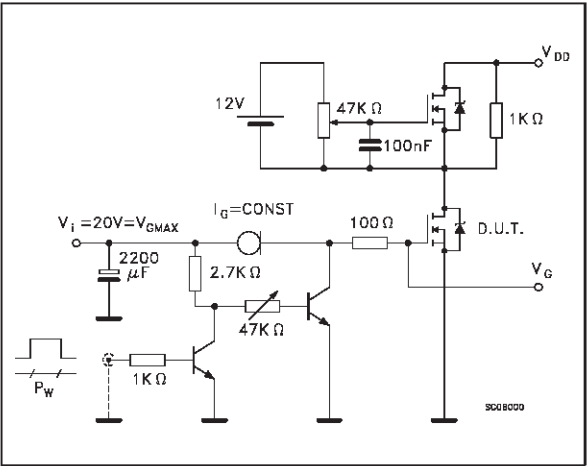
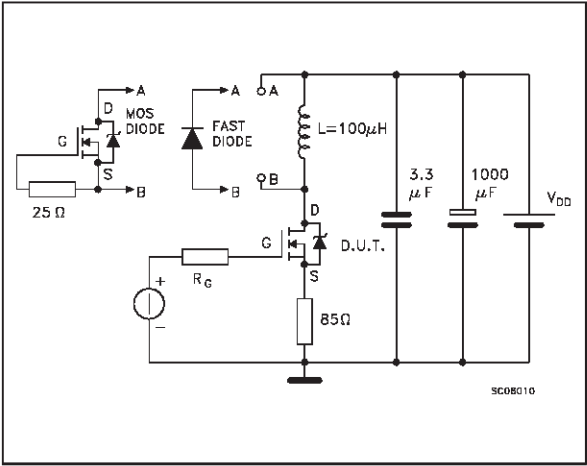
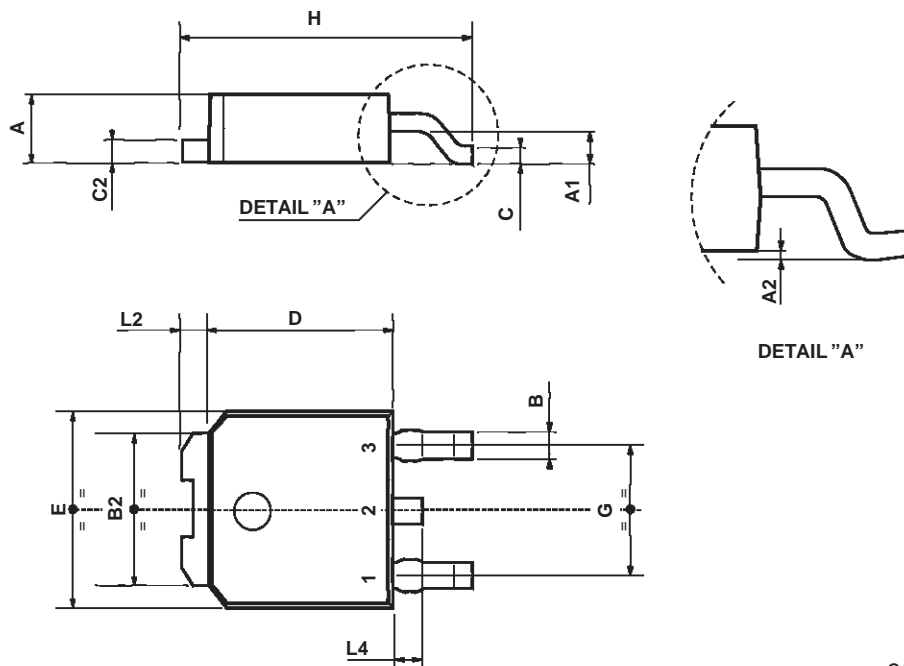


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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