



STP2NC70Z, STP2NC70ZFP STD1NC70Z, STD1NC70Z-1

N-CHANNEL 700V - 7.3Ω - 1.4A TO-220/FP/DPAK/IPAK
Zener-Protected PowerMESH™III MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP2NC70Z	700 V	< 8.5 Ω	1.4 A	50 W
STP2NC70ZFP	700 V	< 8.5 Ω	1.4 A	25 W
STD1NC70Z	700 V	< 8.5 Ω	1.4 A	45 W
STD1NC70Z-1	700 V	< 8.5 Ω	1.4 A	45 W

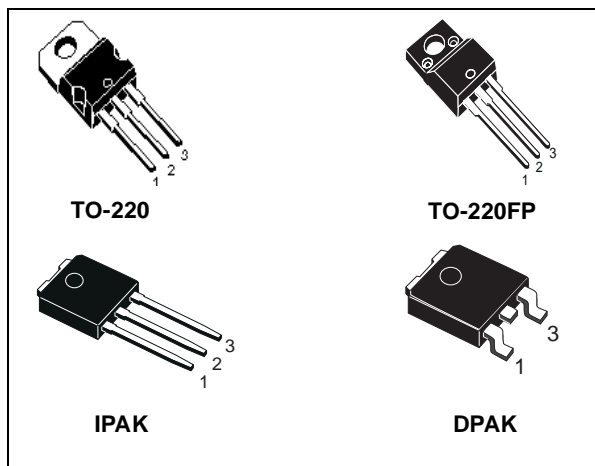
- TYPICAL R_{DS(on)} = 7.3 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES

DESCRIPTION

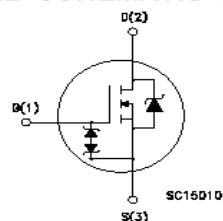
The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications..

APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP2NC70Z	P2NC70Z	TO-220	TUBE
STP2NC70ZFP	P2NC70ZFP	TO-220FP	TUBE
STD1NC70ZT4	D1NC70Z	DPAK	TAPE & REEL
STD1NC70Z-1	D1NC70Z	IPAK	TUBE

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP2NC70Z	STP2NC70ZFP	STD1NC70Z STD1NC70Z-1	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	700			V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	700			V
V _{GS}	Gate- source Voltage	± 25			V
I _D	Drain Current (continuous) at T _C = 25°C	1.4	1.4 (*)	1.4	A
I _D	Drain Current (continuous) at T _C = 100°C	0.9	0.9 (*)	0.9	A
I _{DM} (•)	Drain Current (pulsed)	5.6	5.6 (*)	5.6	A
P _{TOT}	Total Dissipation at T _C = 25°C	50	25	45	W
	Derating Factor	0.4	0.2	0.36	W/°C
I _{GS}	Gate-source Current (DC)	± 50			mA
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000			V
dv/dt (1)	Peak Diode Recovery voltage slope	3			V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	-	V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-65 to 150 -65 to 150			°C °C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 10A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220	TO-220FP	DPAK IPAK	
R _{thj-case}	Thermal Resistance Junction-case Max	2.5	5	2.75	°C/W
R _{thj-pcb}	Thermal Resistance Junction-pcb Max (for SMD) (#)			100	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		100	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		275	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	1.4	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	60	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} =± 1mA (Open Drain)	25			V
α _T	Voltage Thermal Coefficient	T=25°C Note(3)		1.3		10 ⁻⁴ /°C

Note: 3. ΔV_{BV} = α_T (25°-T) BV_{GSO}(25°)

(#) When mounted on minimum Footprint

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to souce. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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ELECTRICAL CHARACTERISTICS (TCASE = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$, $V_{GS} = 0$	700			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$, $I_D = 0.7 A$		7.3	8.5	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 V$, $I_D = 0.7 A$		1.2		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		305 34 3.6		pF pF pF
$C_{oss \text{ eq. (3)}}$	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V \text{ to } 560V$		28		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 350 V$, $I_D = 0.8 A$ $R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (Resistive Load see, Figure 3)		11 8		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 560V$, $I_D = 1.6 A$, $V_{GS} = 10V$		8 2 3.8	12	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 350 V$, $I_D = 0.8 A$ $R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (Resistive Load see, Figure 3)		27 30		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 560V$, $I_D = 1.6 A$, $R_G = 4.7 \Omega$, $V_{GS} = 10V$ (Inductive Load see, Figure 5)		20 5 25		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				1.4 5.6	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 1.4 A$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 1.6 A$, $di/dt = 100A/\mu s$ $V_{DD} = 30V$, $T_J = 150^\circ C$ (see test circuit, Figure 5)		370 1.3 6.8		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

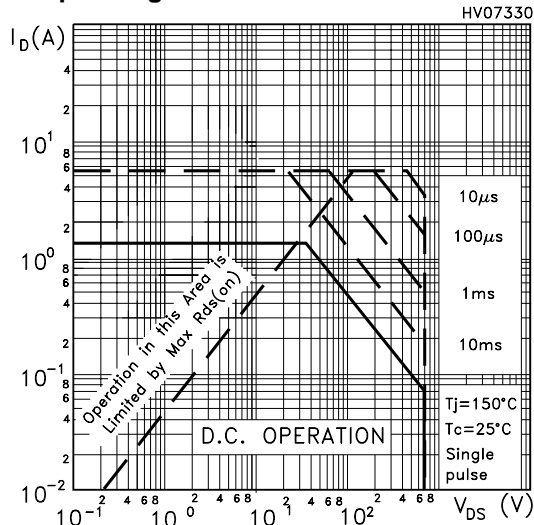
2. Pulse width limited by safe operating area.

3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

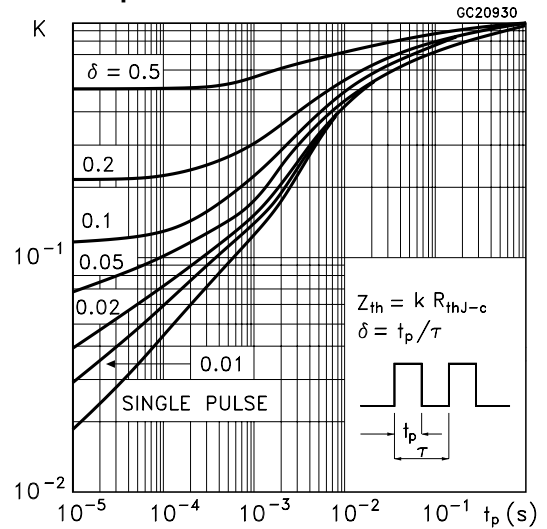


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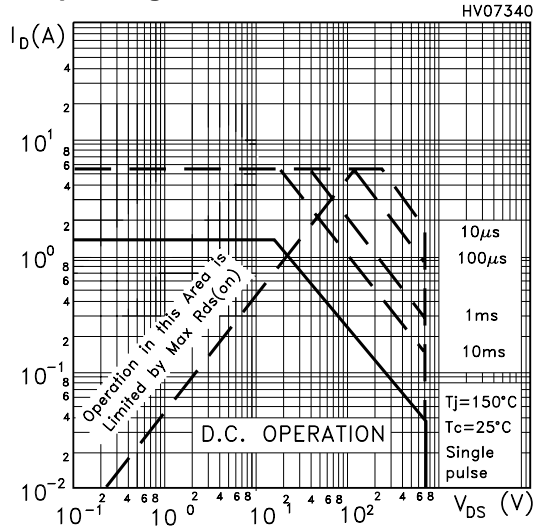
Safe Operating Area For TO-220



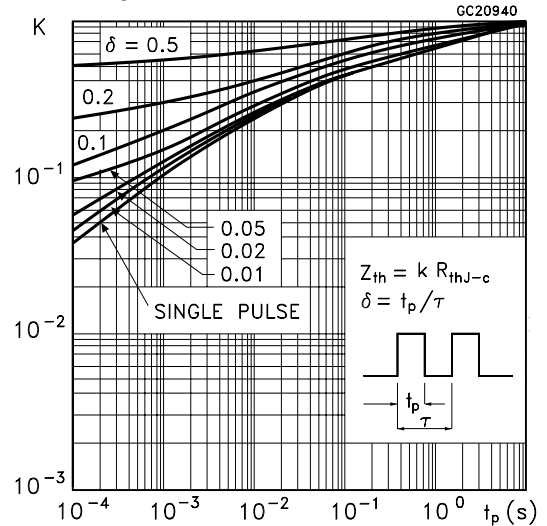
Thermal Impedance For TO-220



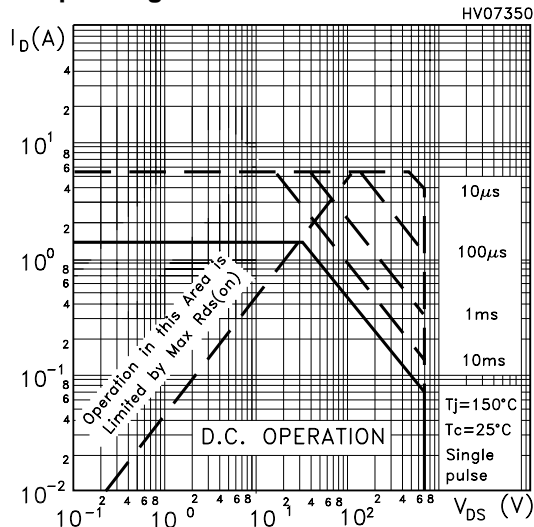
Safe Operating Area For TO-220FP



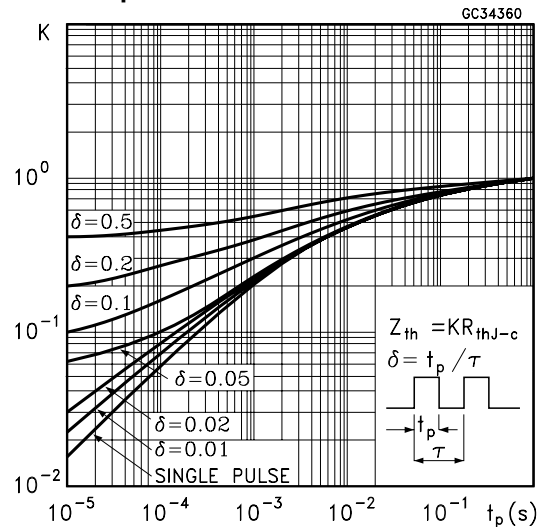
Thermal Impedance For TO-220FP



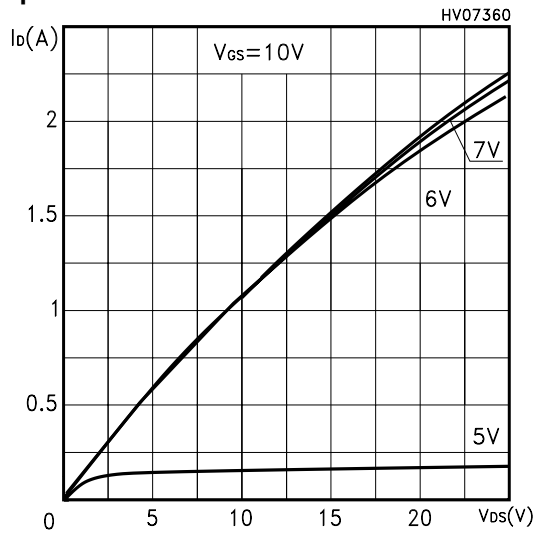
Safe Operating Area For DPAK/IPAK



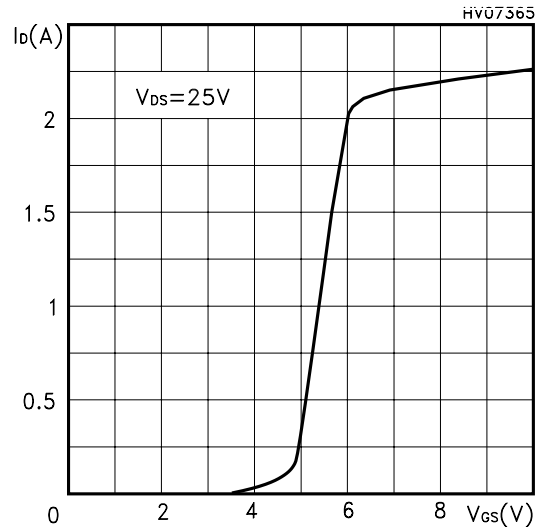
Thermal Impedance For DPAK/IPAK



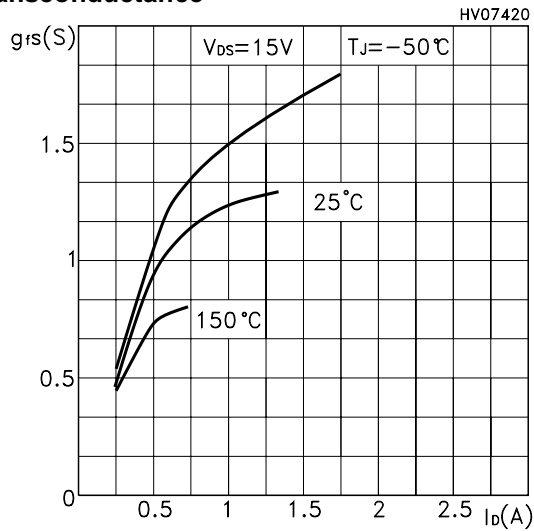
Output Characteristics



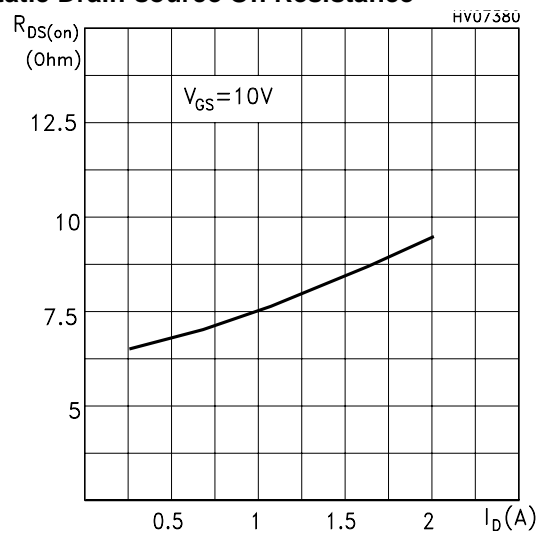
Transfer Characteristics



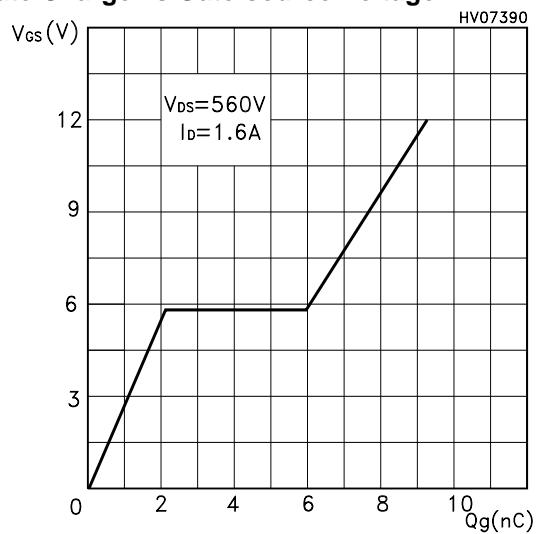
Transconductance



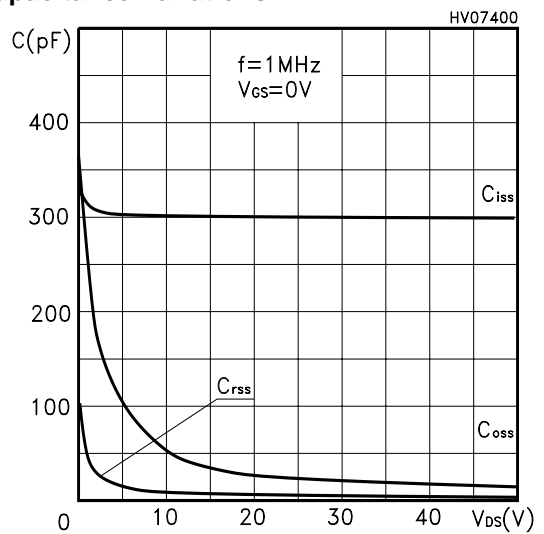
Static Drain-source On Resistance



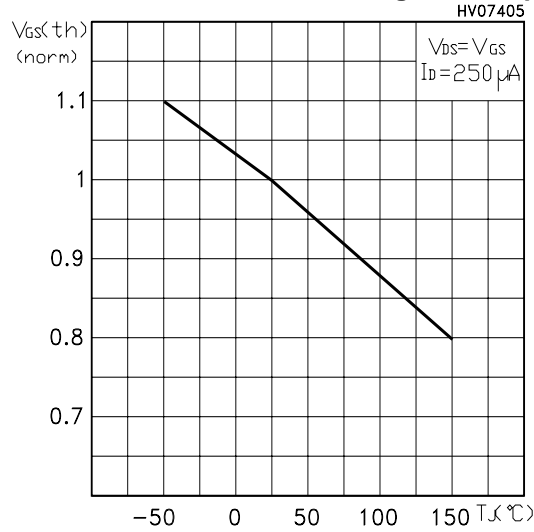
Gate Charge vs Gate-source Voltage



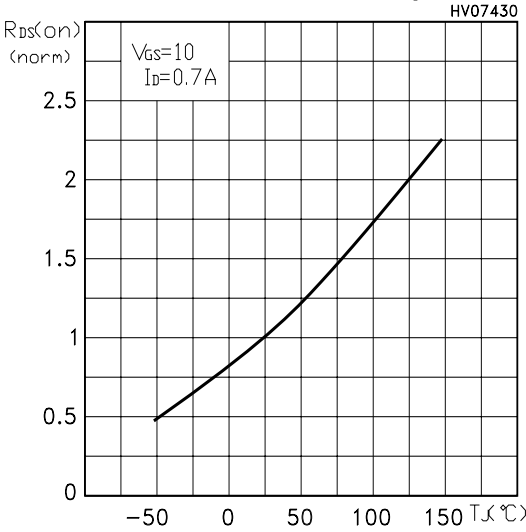
Capacitance Variations



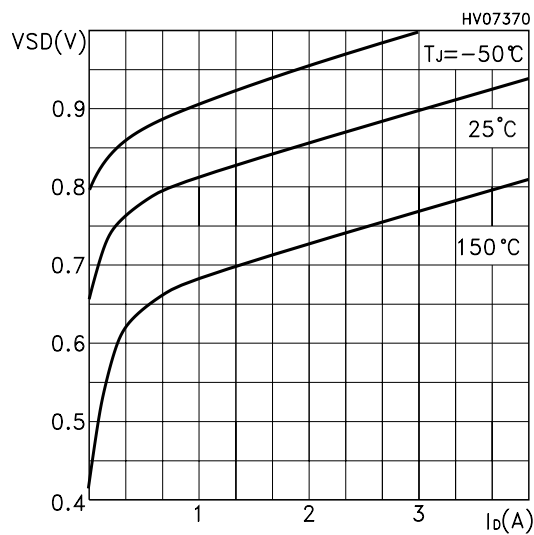
Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature

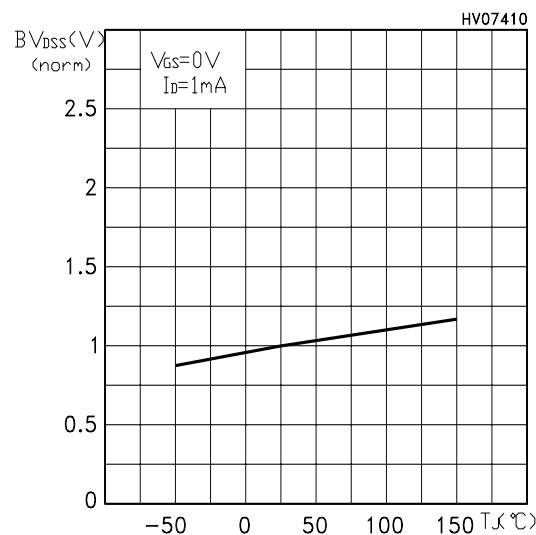


Fig. 1: Unclamped Inductive Load Test Circuit

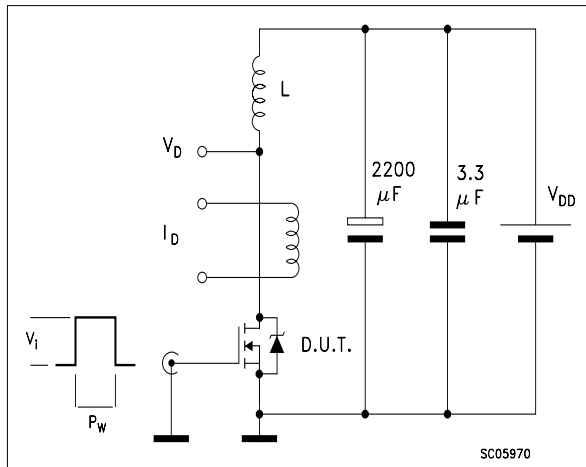


Fig. 2: Unclamped Inductive Waveform

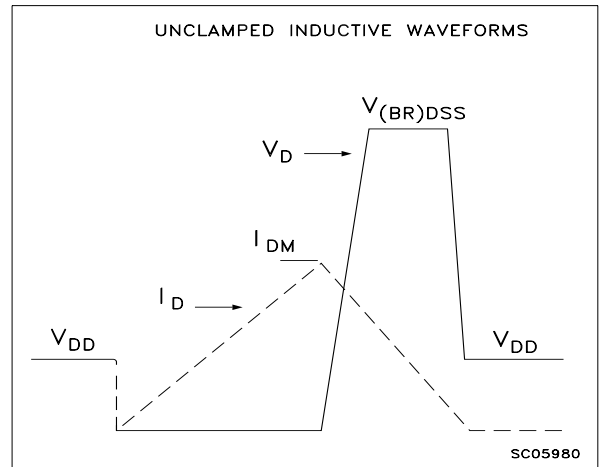


Fig. 3: Switching Times Test Circuit For Resistive Load

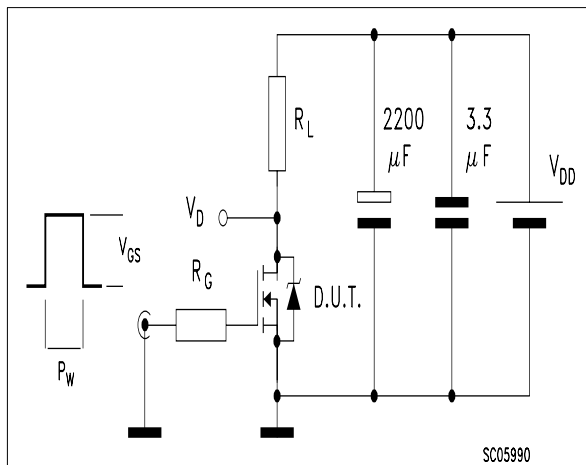


Fig. 4: Gate Charge test Circuit

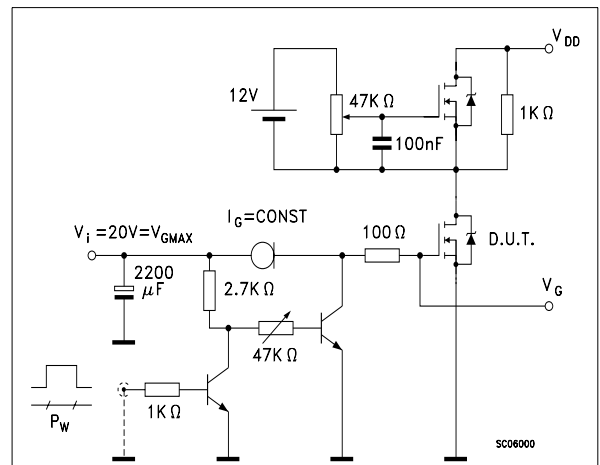
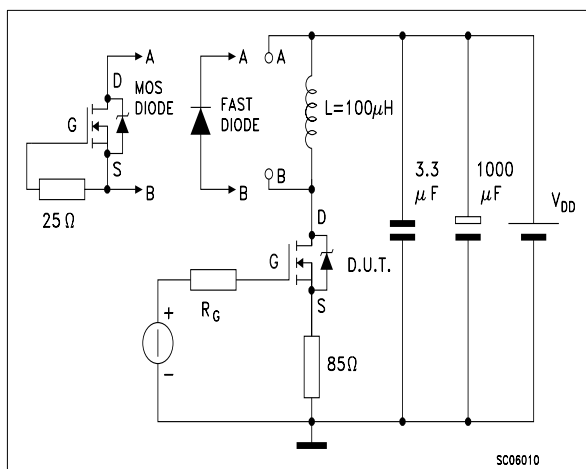
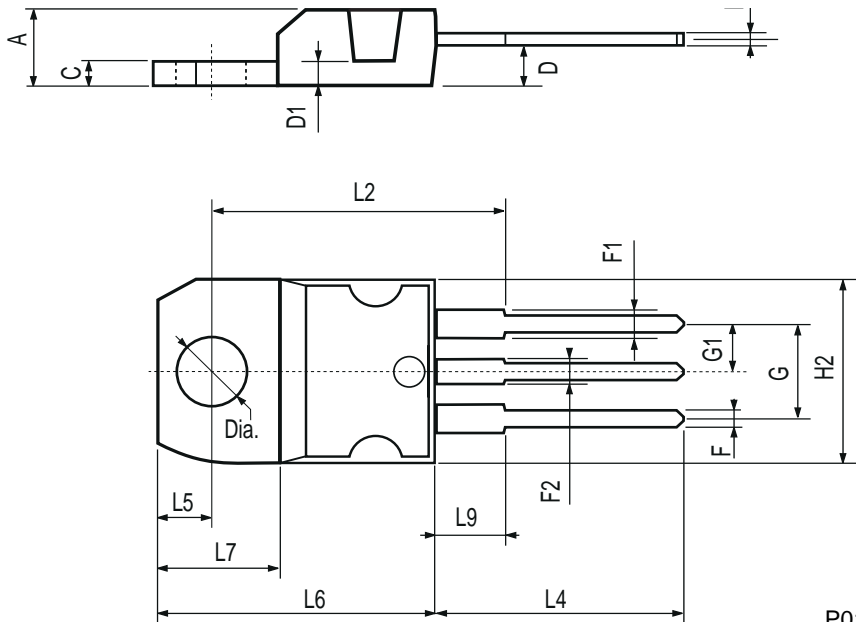


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



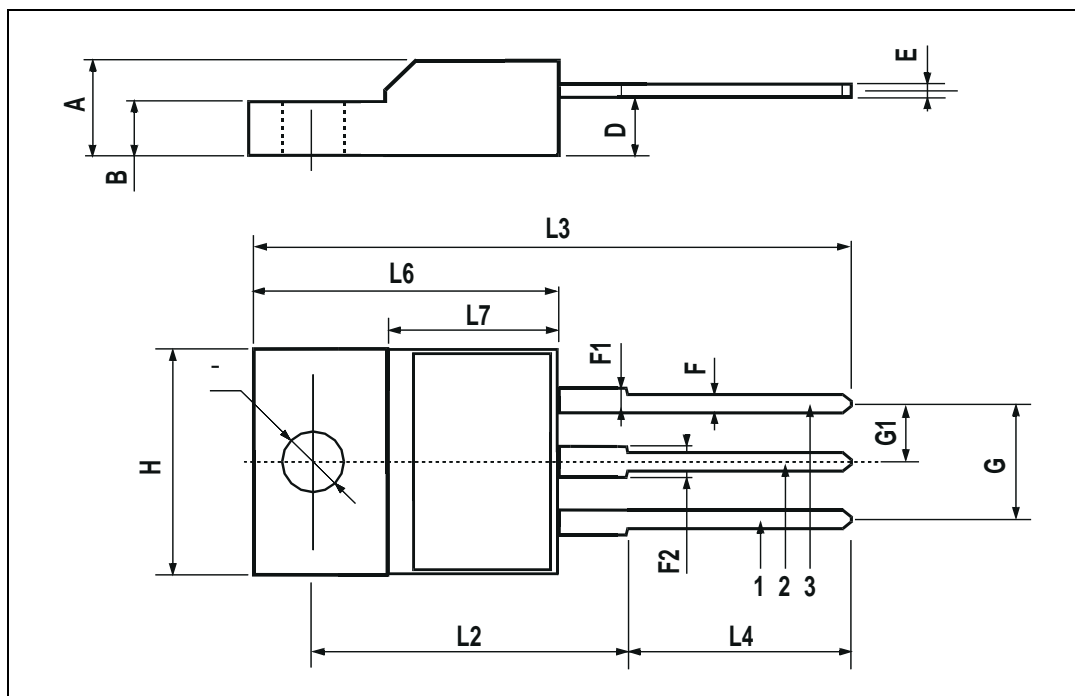
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



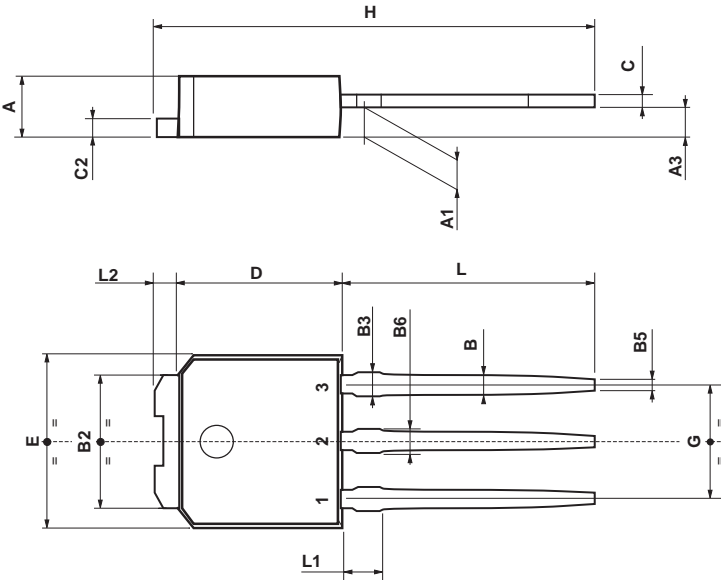
TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-251 (IPAK) MECHANICAL DATA

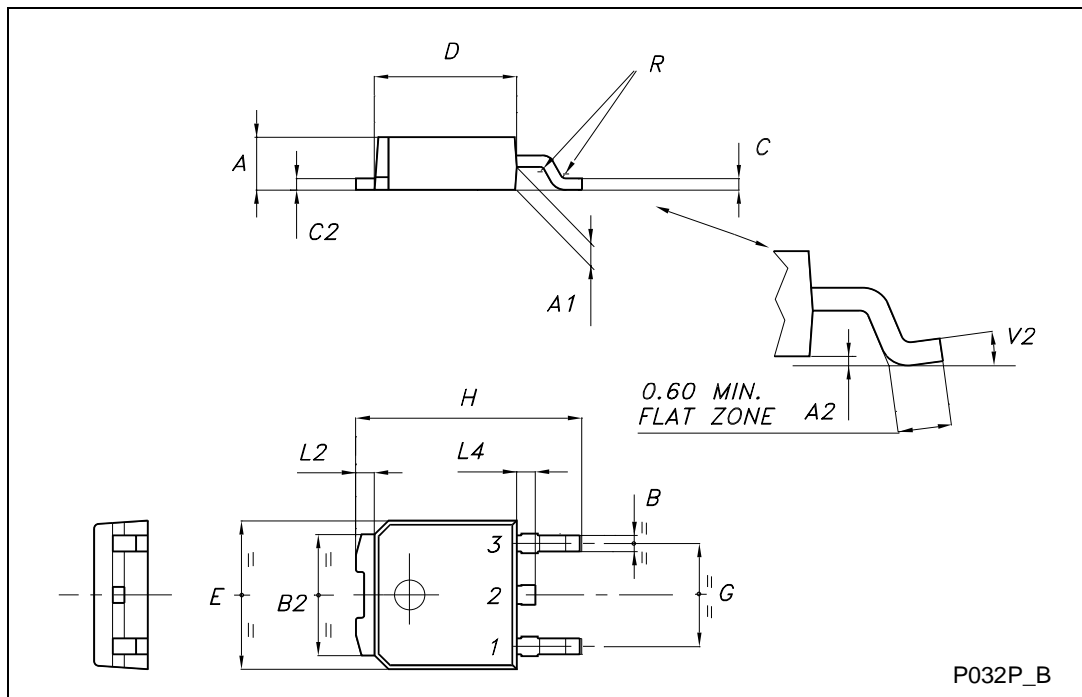
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



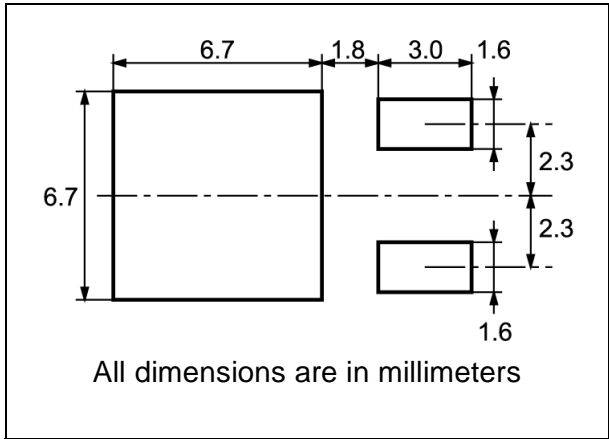
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TO-252 (DPAK) MECHANICAL DATA

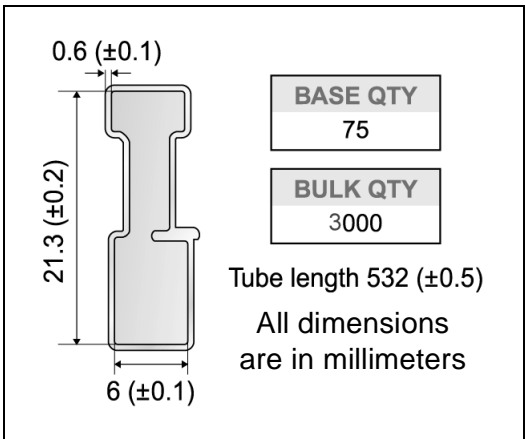
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



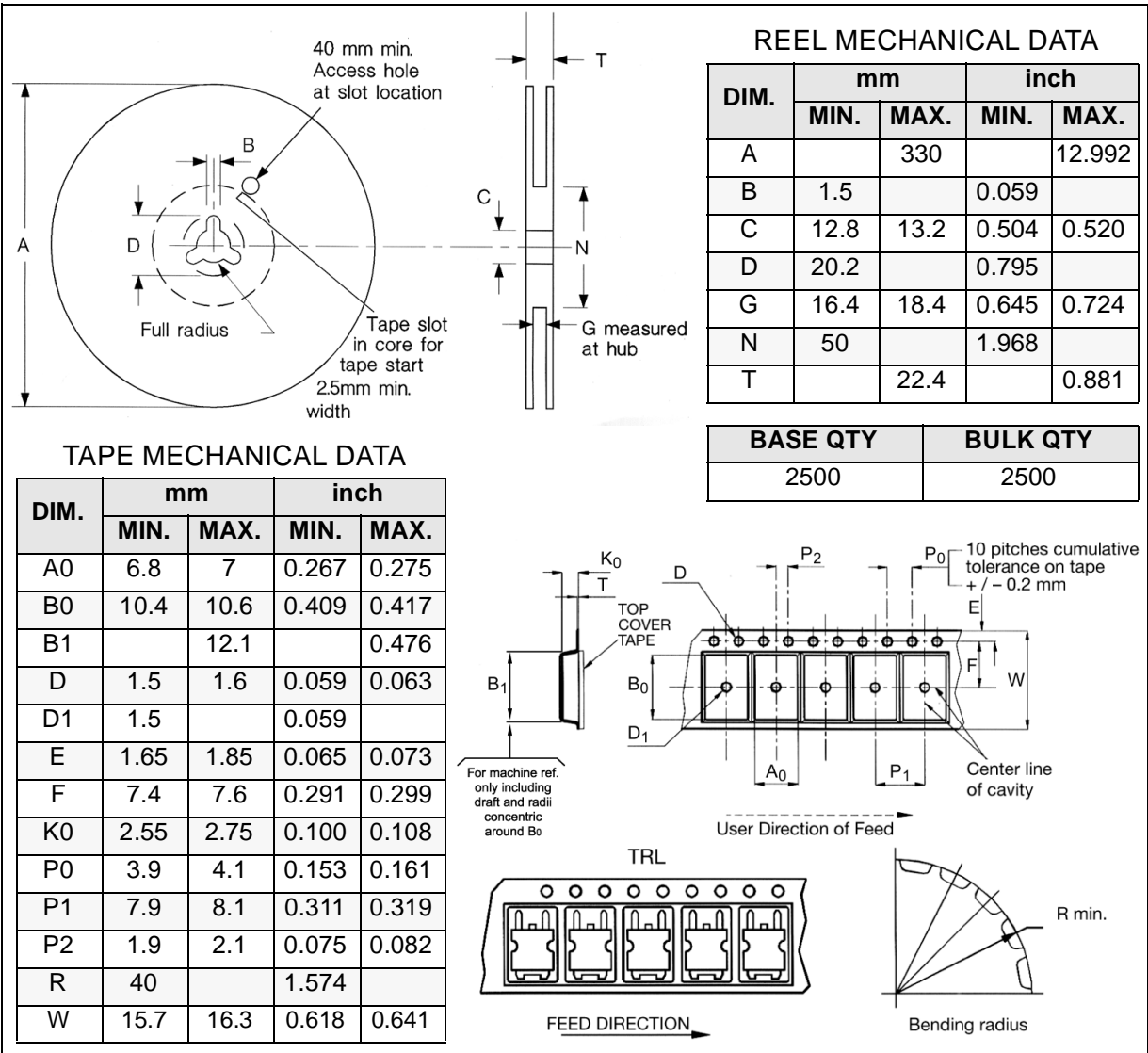
DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



* on sales type

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