



STD25NF10L

N-CHANNEL 100V - 0.030 Ω - 25A DPAK LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD25NF10L	100 V	< 0.035 Ω	25 A

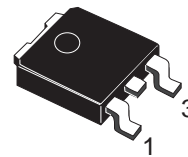
- TYPICAL R_{DS(on)} = 0.030 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW THRESHOLD DEVICE
- LOGIC LEVEL DEVICE
- SURFACE-MOUNTING DPAK (TO-252)
POWER PACKAGE IN TAPE & REEL
(SUFFIX "T4")

DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements

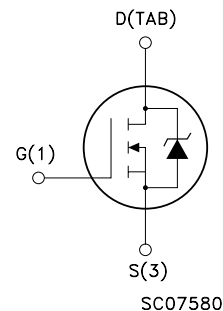
APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



**DPAK
TO-252**
(Suffix "T4")

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	100	V
V _{GS}	Gate- source Voltage	± 16	V
I _D (*)	Drain Current (continuous) at T _C = 25°C	25	A
I _D	Drain Current (continuous) at T _C = 100°C	25	A
I _{DM} (•)	Drain Current (pulsed)	100	A
P _{tot}	Total Dissipation at T _C = 25°C	100	W
	Derating Factor	0.67	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	450	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

(*) Current Limited by Package

(1) I_{SD} \leq 25A, di/dt \leq 300A/ μ s, V_{DD} \leq V_{(BR)DSS}, T_j \leq T_{JMAX}

(2) Starting T_j = 25 °C, I_D = 12.5A, V_{DD} = 50V

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.5	°C/W
Rthj-pcb	Thermal Resistance Junction-pcb(#)	Max	50	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		275	°C

(#) When Mounted on 1 inch² FR-4 board, 2 oz of Cu.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 µA	1		2.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 12.5 A V _{GS} = 4.5 V I _D = 12.5 A		0.030 0.035	0.035 0.040	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 12.5 A		24		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		1710 250 110		pF pF pF

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ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 12.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 3)		20 40		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 80\text{ V}$ $I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}$		38 8.5 21	52	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 50\text{ V}$ $I_D = 12.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 3)		58 20		ns ns

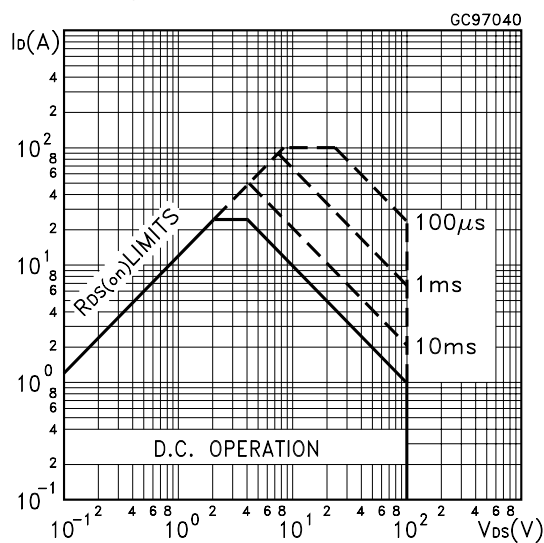
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				25 100	A A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 25\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		88 317 7.2		ns nC A

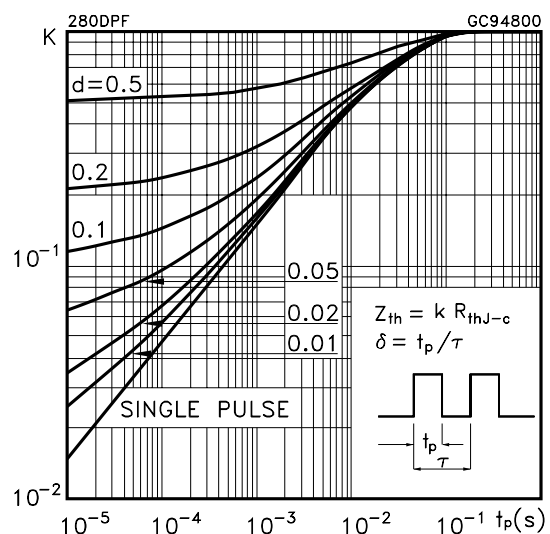
(\ast) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(\bullet) Pulse width limited by safe operating area.

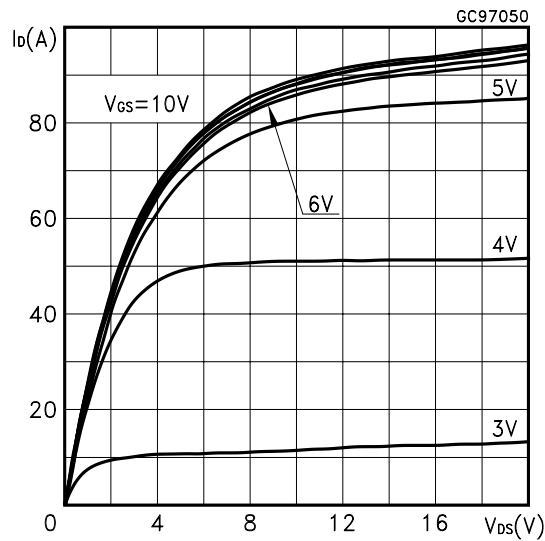
Safe Operating Area



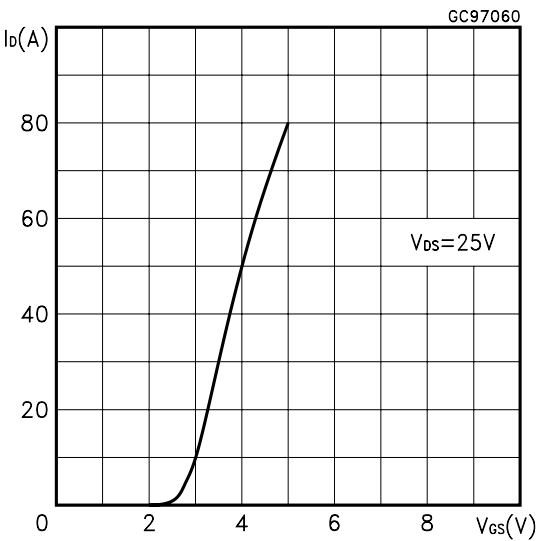
Thermal Impedance



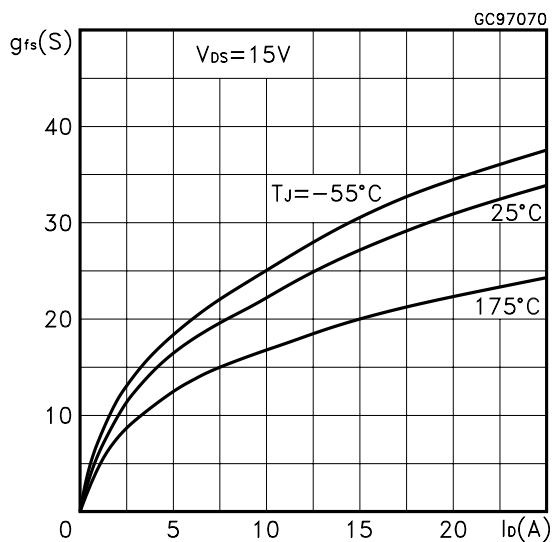
Output Characteristics



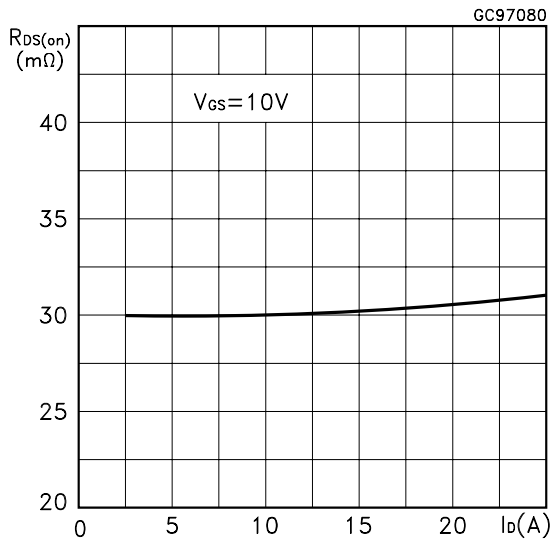
Transfer Characteristics



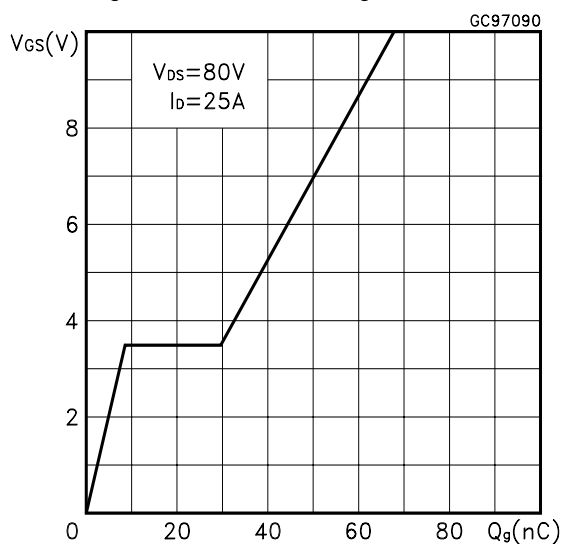
Transconductance



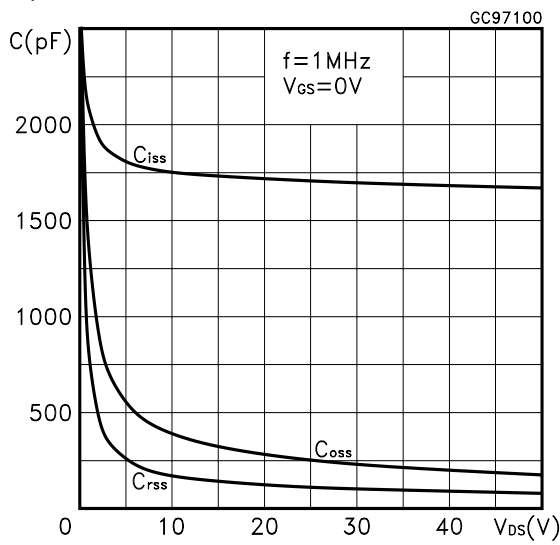
Static Drain-source On Resistance



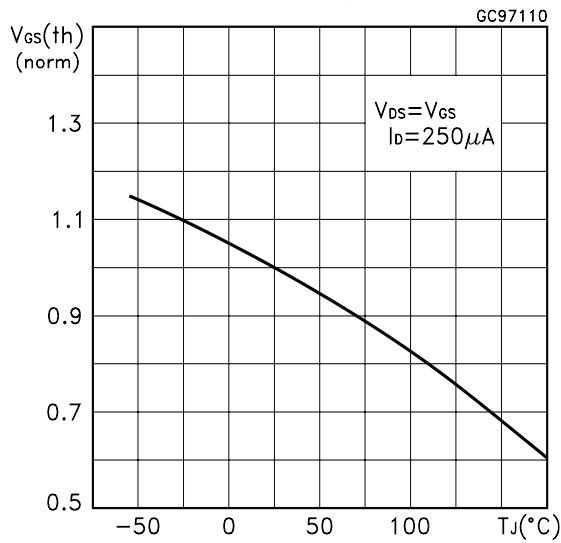
Gate Charge vs Gate-source Voltage



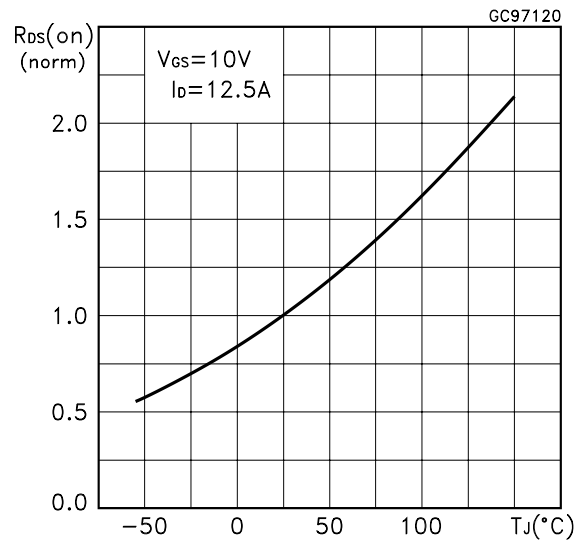
Capacitance Variations



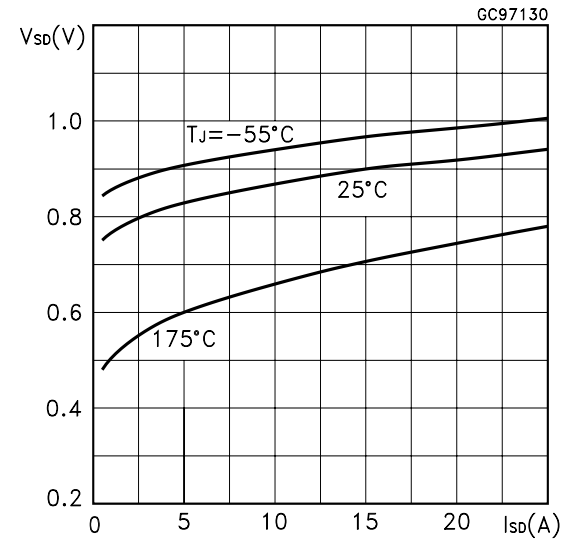
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

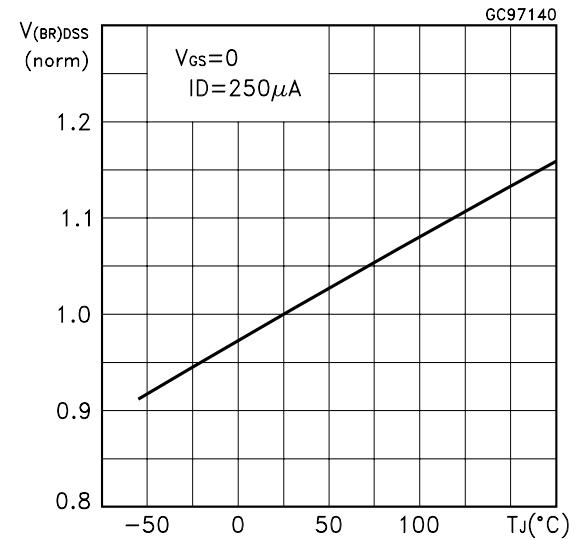


Fig. 1: Unclamped Inductive Load Test Circuit

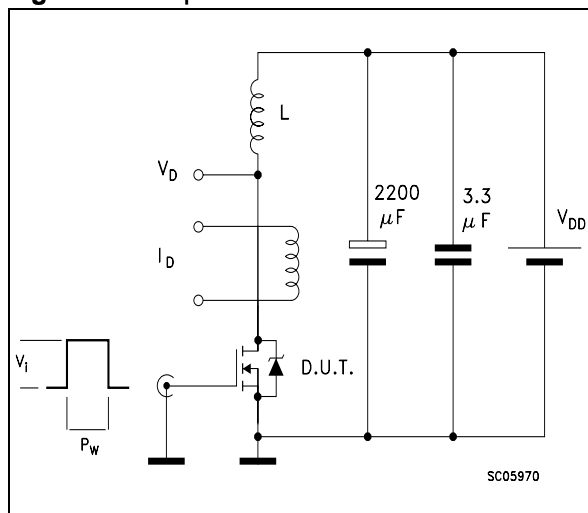


Fig. 2: Unclamped Inductive Waveform

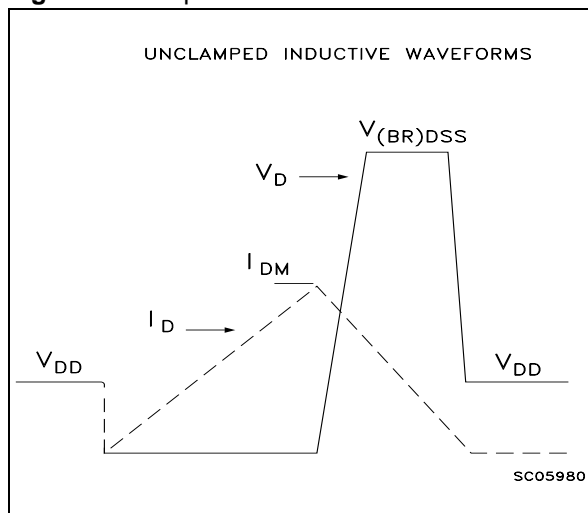


Fig. 3: Switching Times Test Circuits For Resistive Load

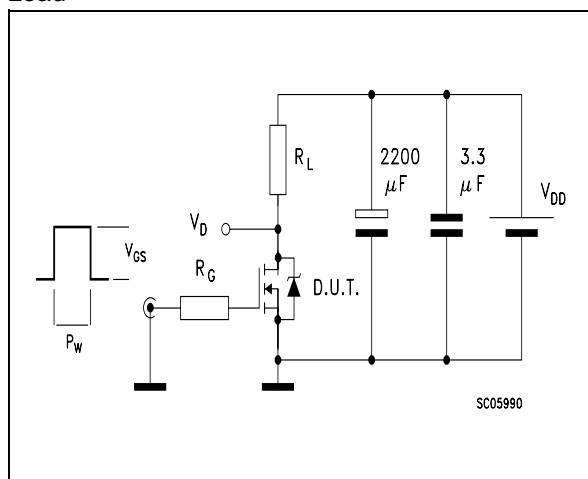


Fig. 4: Gate Charge test Circuit

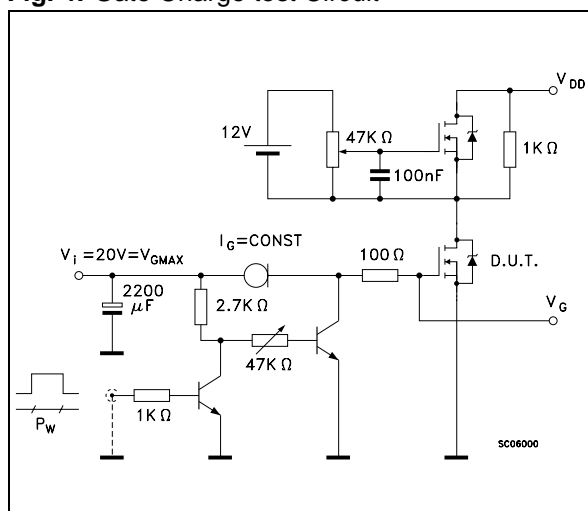
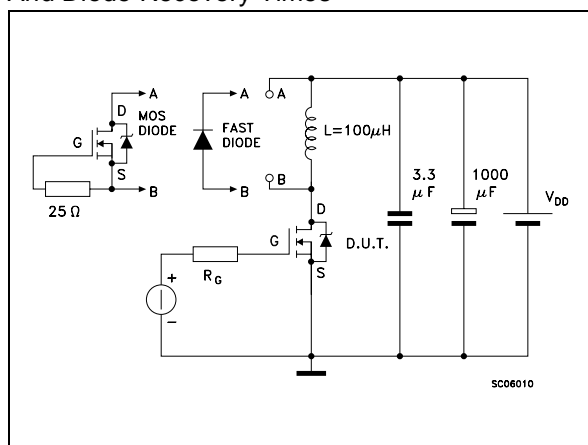
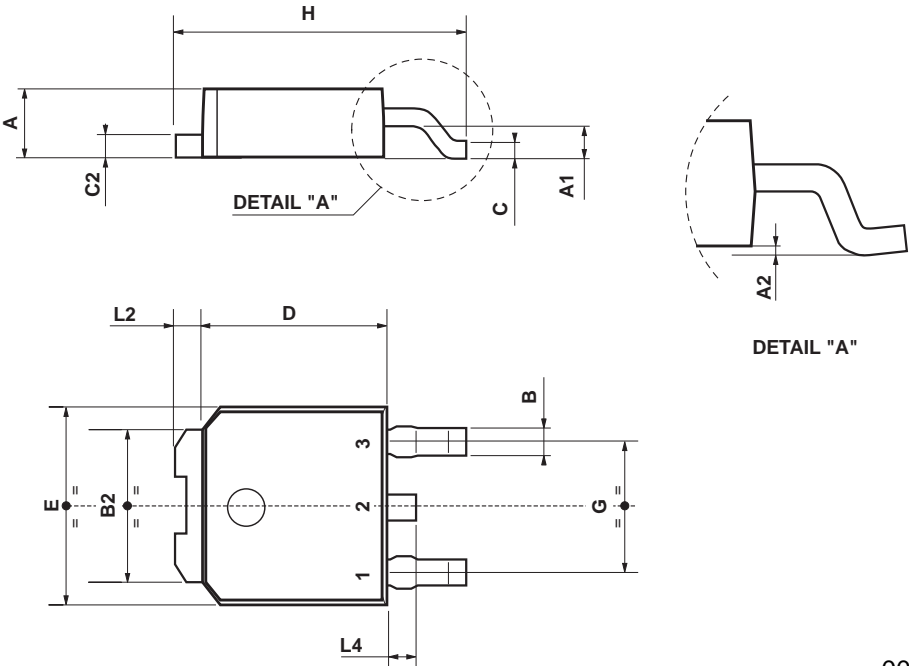


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



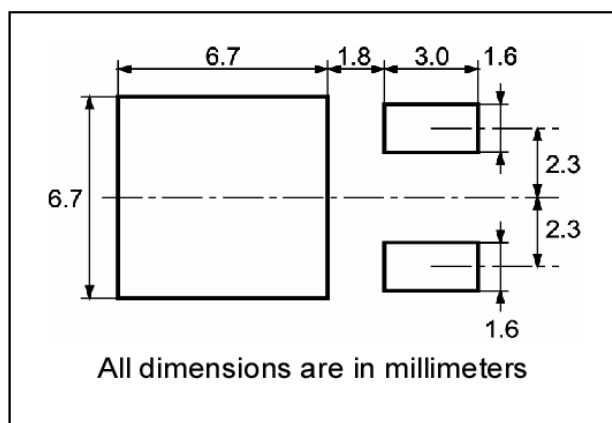
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039

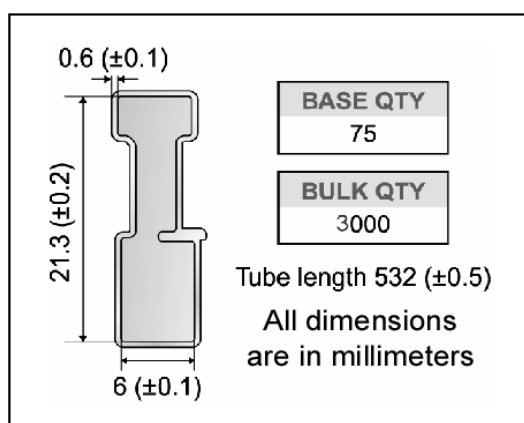
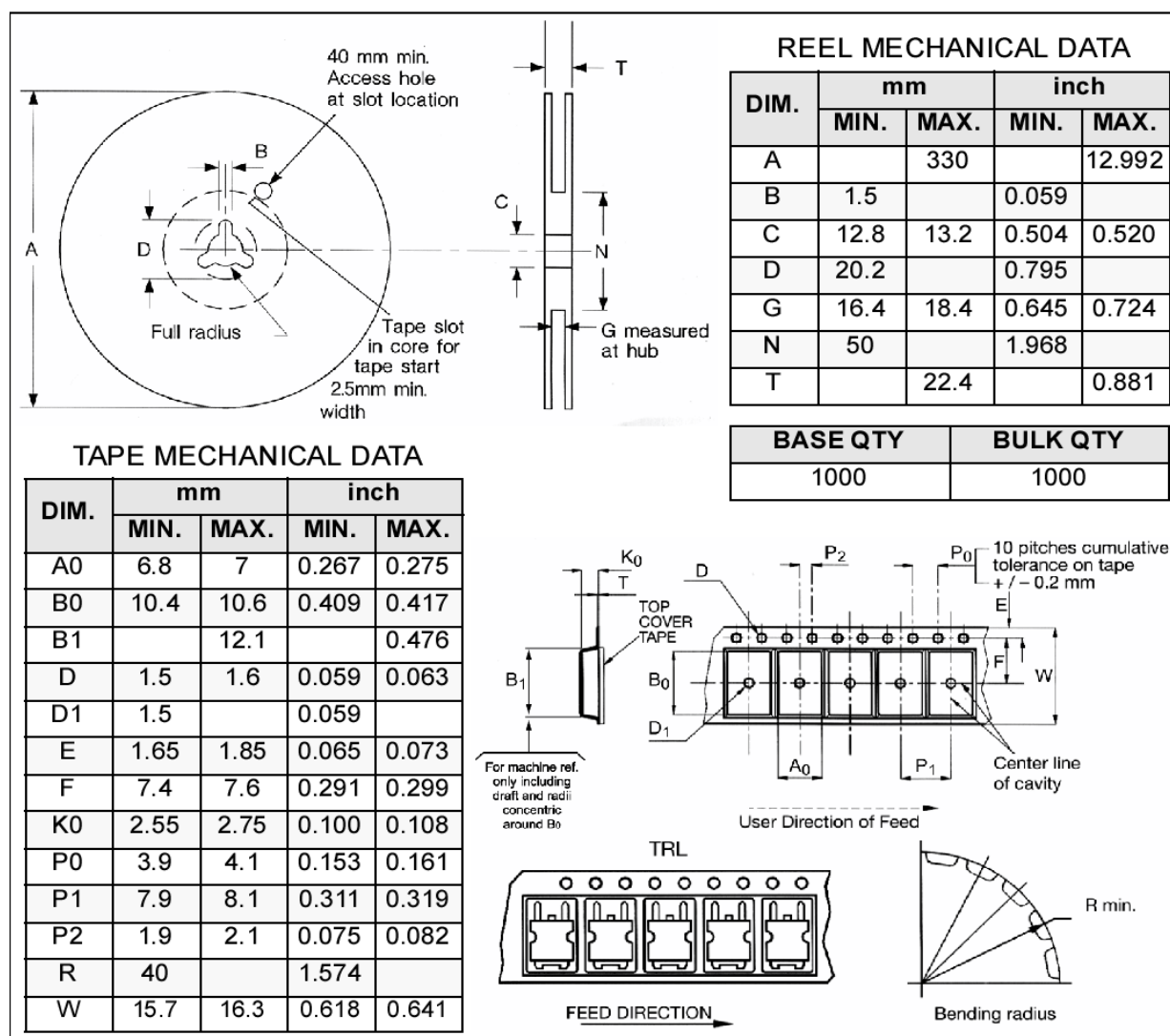


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DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*

**TAPE AND REEL SHIPMENT (suffix "T4")***

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