



# STD40NF06LZ

## N-CHANNEL 60V - 0.020 $\Omega$ - 40A DPAK Zener-Protected STripFET™ II POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD40NF06LZ	60 V	< 25 m $\Omega$	40 A

- TYPICAL R<sub>DS(on)</sub> = 0.020 $\Omega$
- 100% AVALANCHE TESTED
- LOW GATE CHARGE
- LOGIC LEVEL GATE DRIVE
- SURFACE-MOUNTING DPAK (TO-252)  
POWER PACKAGE IN TAPE & REEL  
(SUFFIX "T4")
- BUILT-IN ZENER DIODES TO IMPROVE ESD  
PROTECTION UP TO 2kV

### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

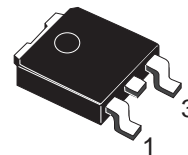
- SINGLE-ENDED SMPS IN MONITOTS,  
COMPUTER AND INDUSTRIAL  
APPLICATION
- WELDING EQUIPMENT
- AUTOMOTIVE

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	60	V
V <sub>GS</sub>	Gate- source Voltage	± 16	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	40	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	28	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	160	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	100	W
	Derating Factor	0.67	W/°C
V <sub>ESD</sub> (G-S)	Gate-source ESD(HBM-C=100pF, R=15k $\Omega$ )	± 2.5	kV
dv/dt <sup>(1)</sup>	Peak Diode Recovery voltage slope	9	V/ns
E <sub>AS</sub> <sup>(2)</sup>	Single Pulse Avalanche Energy	450	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

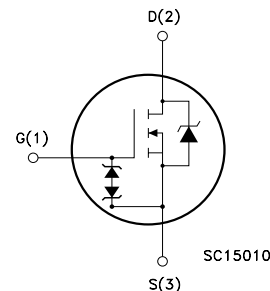
(•) Pulse width limited by safe operating area.

<sup>(1)</sup> I<sub>SD</sub> ≤ 40A, di/dt ≤ 100A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.  
<sup>(2)</sup> Starting T<sub>j</sub> = 25 °C I<sub>D</sub> = 20A V<sub>DD</sub> = 45V



**DPAK  
TO-252**  
(Suffix "T4")

### INTERNAL SCHEMATIC DIAGRAM



## STD40NF06LZ

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.5	°C/W
Rthj-PCB	Thermal Resistance Junction-PCB (#)	Max	50	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

(#) When Mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu.

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 µA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 50	µA µA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16 V			±10	µA

#### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 µA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 5 V I <sub>D</sub> = 20 A V <sub>GS</sub> = 10 V I <sub>D</sub> = 20 A			0.030 0.025	Ω Ω

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 15 V I <sub>D</sub> = 20 A		25		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		1360 302 115		pF pF pF

**ELECTRICAL CHARACTERISTICS** (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		17 75		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 48\text{ V}$ $I_D = 40\text{ A}$ $V_{GS} = 10\text{ V}$		54 11 12		nC nC nC

**SWITCHING OFF**

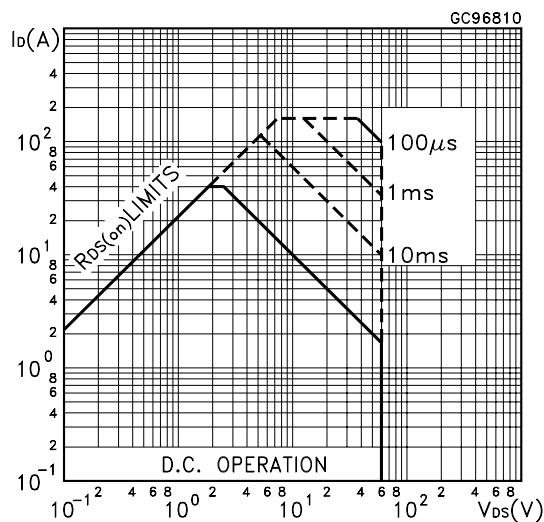
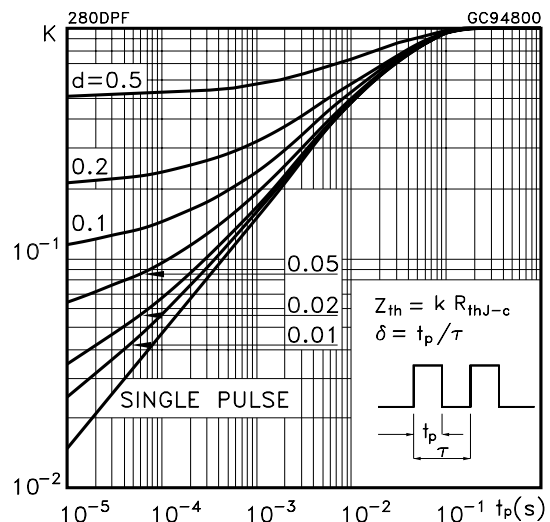
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 30\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		38 23		ns ns

**SOURCE DRAIN DIODE**

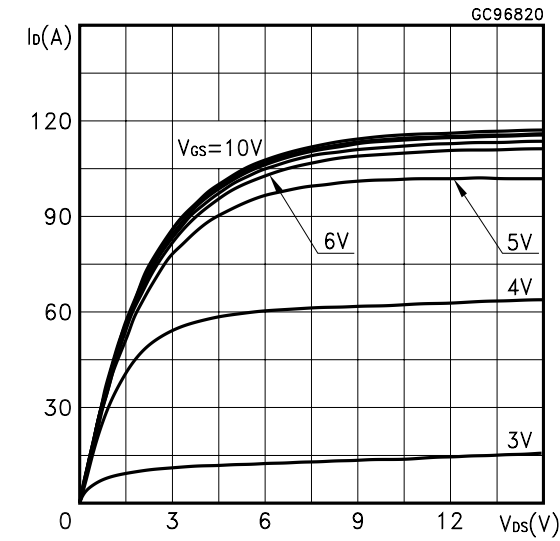
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				40 160	A A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 40\text{ A}$ $V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		66 142 4.3		ns nC A

( $\ast$ ) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

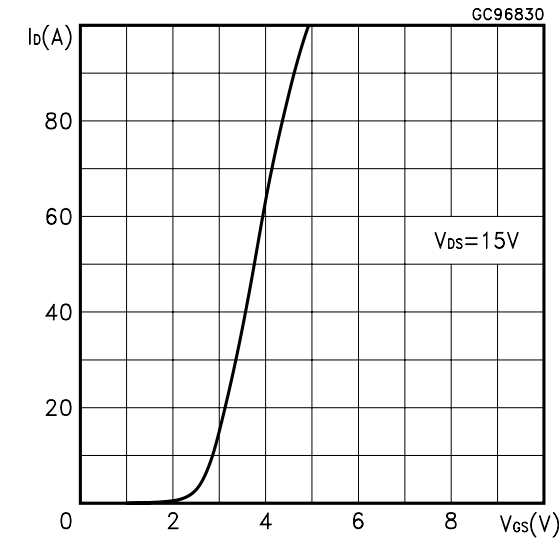
( $\bullet$ ) Pulse width limited by safe operating area.

**Safe Operating Area****Thermal Impedance**

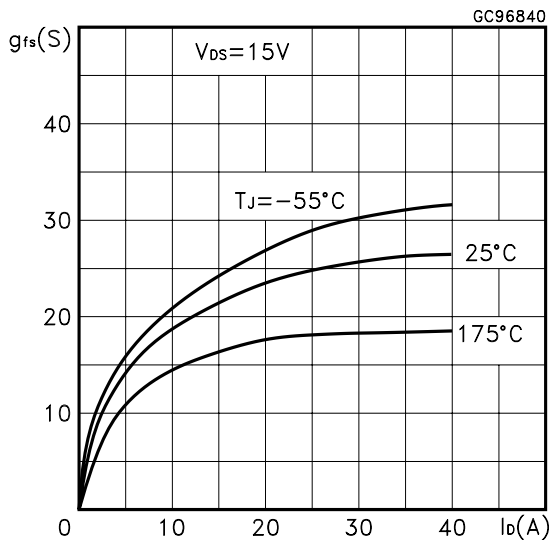
Output Characteristics



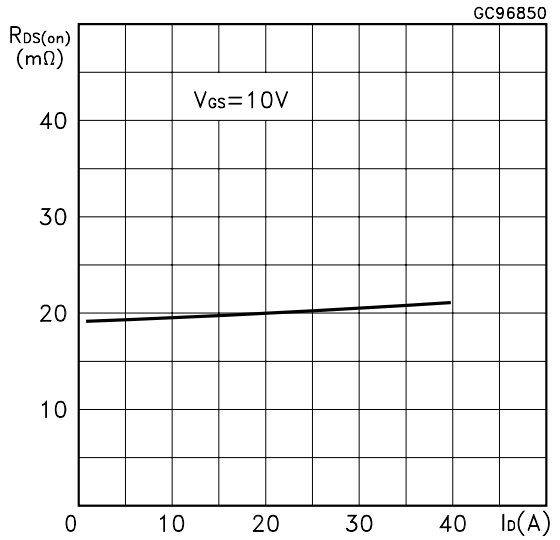
Transfer Characteristics



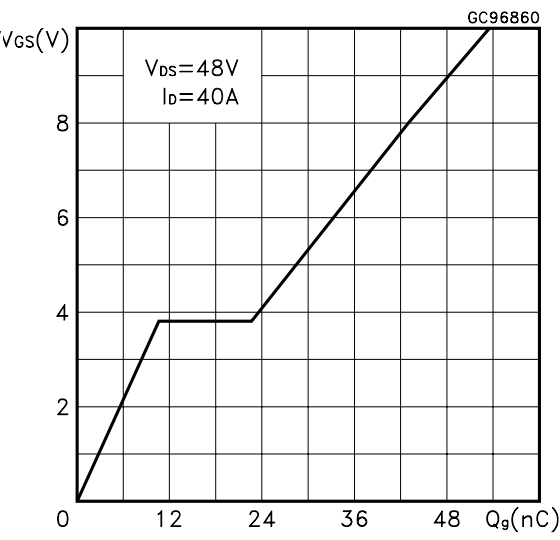
Transconductance



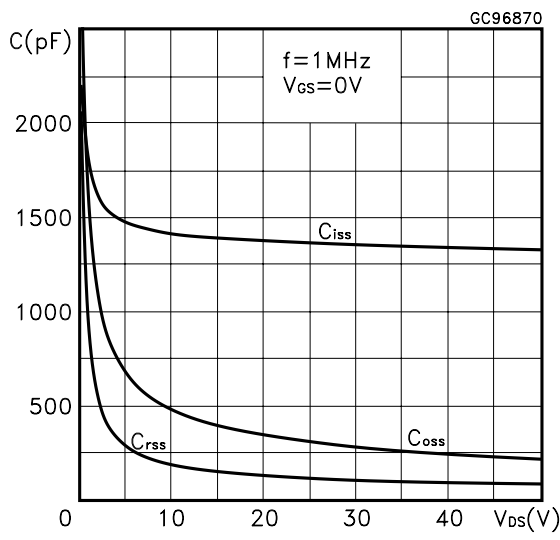
Static Drain-source On Resistance

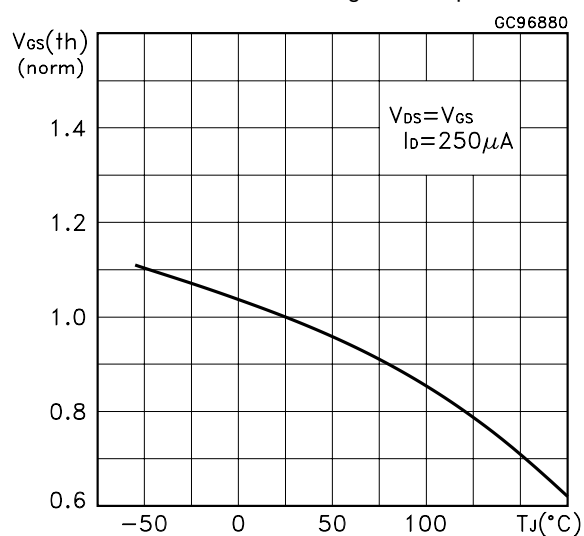
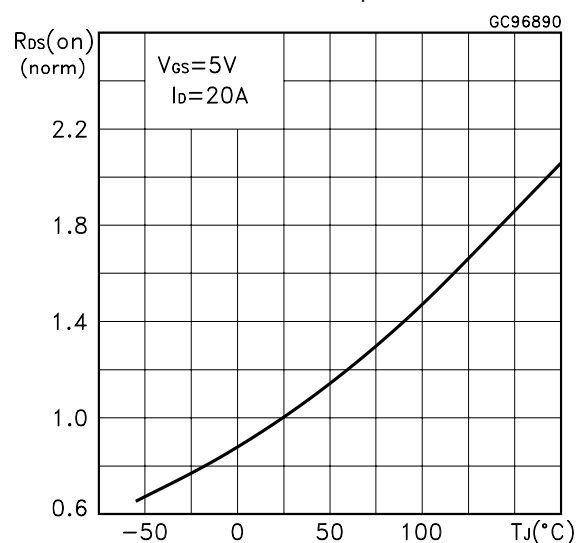
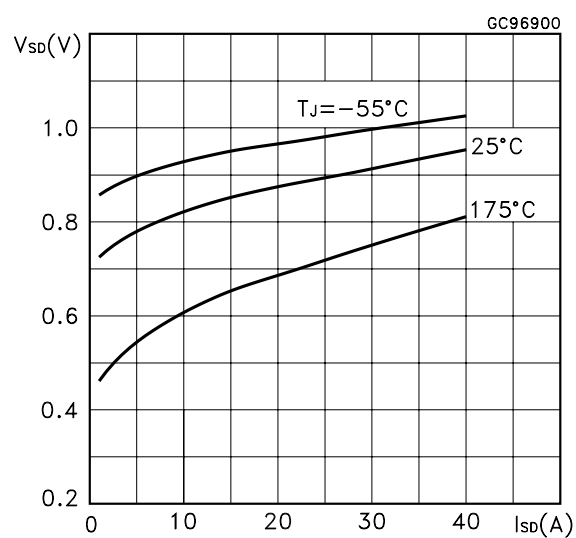
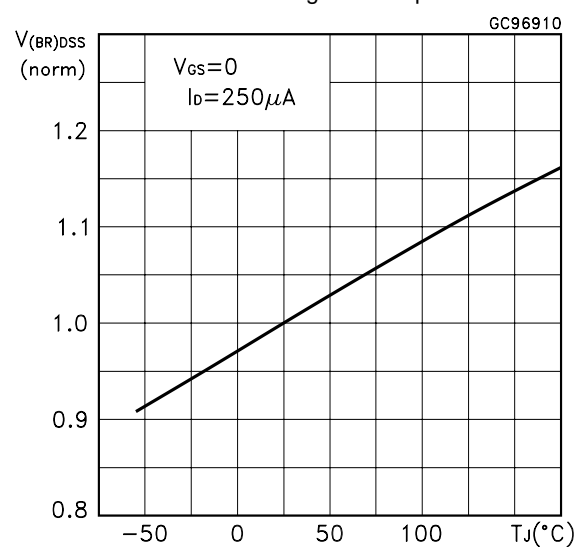


Gate Charge vs Gate-source Voltage

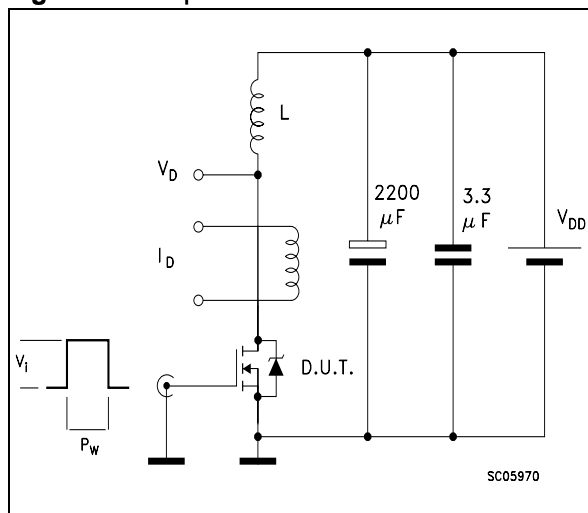


Capacitance Variations

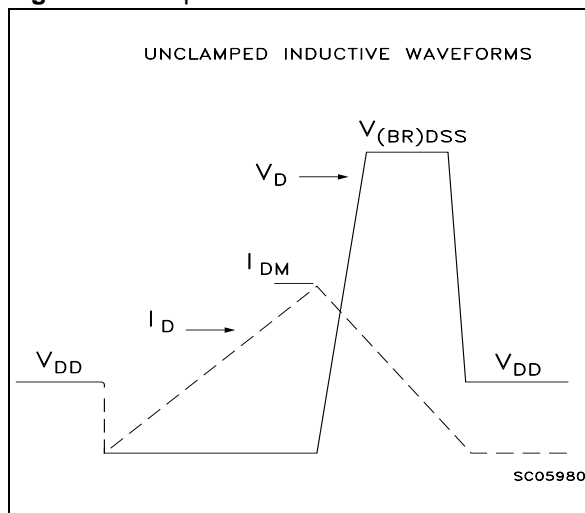


**Normalized Gate Threshold Voltage vs Temperature**

**Normalized on Resistance vs Temperature**

**Source-drain Diode Forward Characteristics**

**Normalized Breakdown Voltage vs Temperature.**


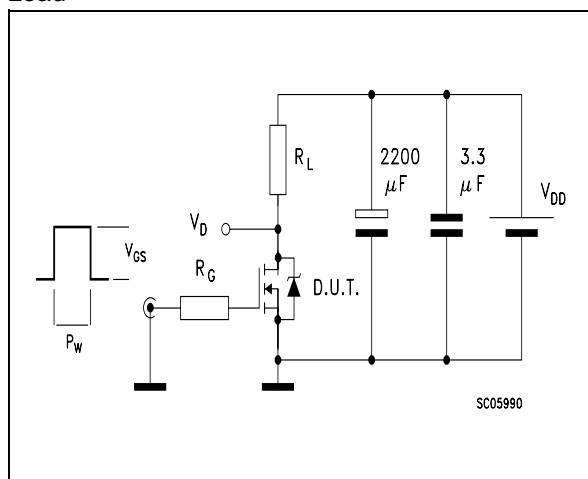
**Fig. 1: Unclamped Inductive Load Test Circuit**



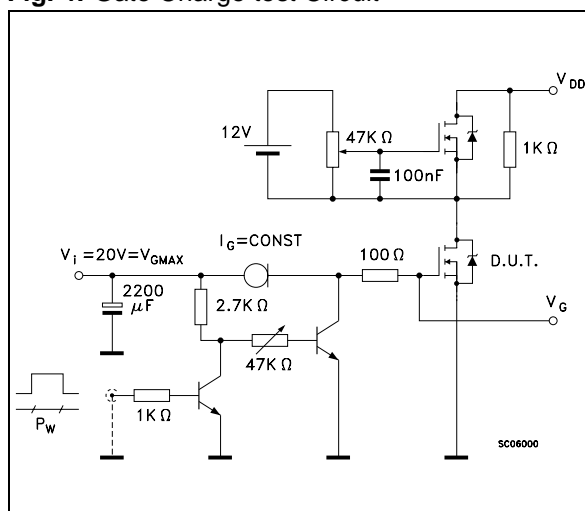
**Fig. 2: Unclamped Inductive Waveform**



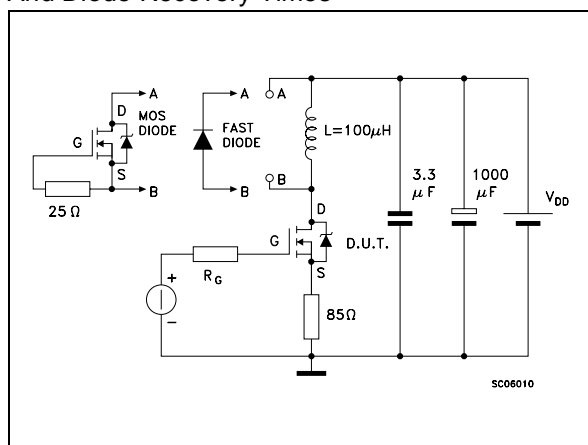
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

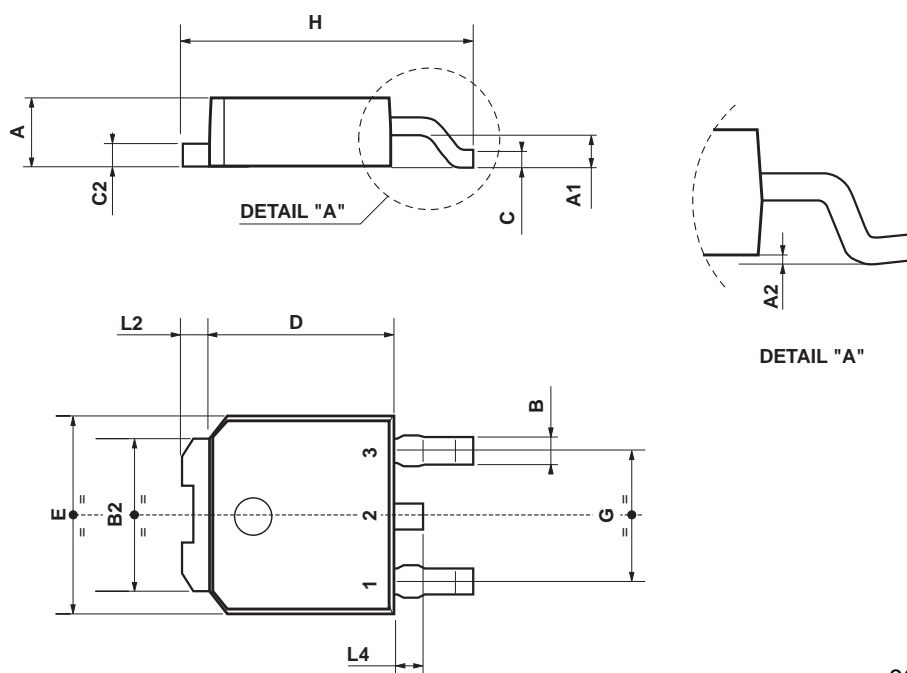


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



## TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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