



STD45NF03L

N - CHANNEL 30V - 0.011 Ω - 45A DPAK STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD45NF03L	30 V	< 0.013 Ω	45 A

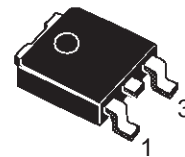
- TYPICAL R_{DS(on)} = 0.011 Ω
- LOW THRESHOLD DRIVE
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

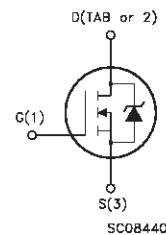
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS



**DPAK
TO-252**
(Suffix "T4")

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 k Ω)	30	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	45	A
I _D	Drain Current (continuous) at T _c = 100 °C	31.5	A
I _{DM} (•)	Drain Current (pulsed)	180	A
P _{tot}	Total Dissipation at T _c = 25 °C	55	W
	Derating Factor	0.37	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	200	mJ
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

(1) starting T_j = 25 °C, I_b = 22.5A, V_{DD} = 20V

STD45NF03L

THERMAL DATA

$R_{thj-pcb}$	Thermal Resistance Junction-PC Board	Max	2.7	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}\text{C}/\text{W}$
$R_{thj-sink}$	Thermal Resistance Case-sink	Typ	0.5	$^{\circ}\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	1	1.5	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\ \text{V}$ $I_D = 22.5\ \text{A}$ $V_{GS} = 4.5\ \text{V}$ $I_D = 22.5\ \text{A}$		0.011 0.013	0.013 0.018	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\ \text{V}$	30			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 22.5\ \text{A}$		60		S
C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$ $f = 1\ \text{MHz}$ $V_{GS} = 0\ \text{V}$		2550		pF
C_{oss}	Output Capacitance			630		pF
C_{rss}	Reverse Transfer Capacitance			215		pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 22.5\text{ A}$		40		ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		250		ns
Q_g	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 22.5\text{ A}$ $V_{GS} = 5\text{ V}$		43	58	nC
Q_{gs}	Gate-Source Charge			12		nC
Q_{gd}	Gate-Drain Charge			21		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 22.5\text{ A}$		60		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		70		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				45	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				180	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 45\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 45\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		75		ns
Q_{rr}	Reverse Recovery Charge			100		nC
I_{RRM}	Reverse Recovery Current			2.6		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

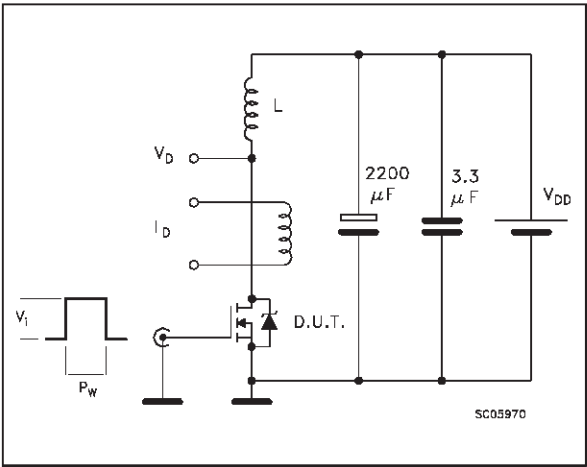


Fig. 2: Unclamped Inductive Waveform

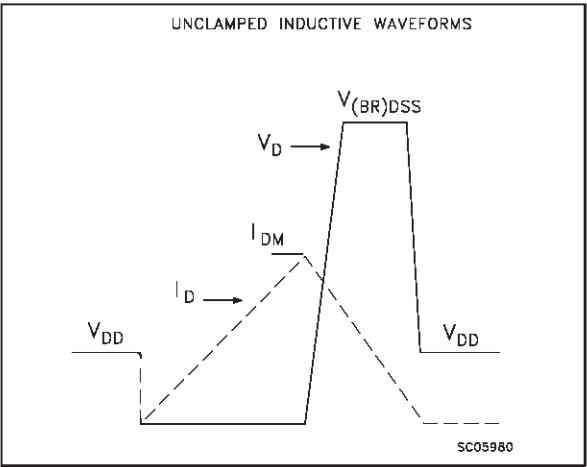


Fig. 3: Switching Times Test Circuits For Resistive Load

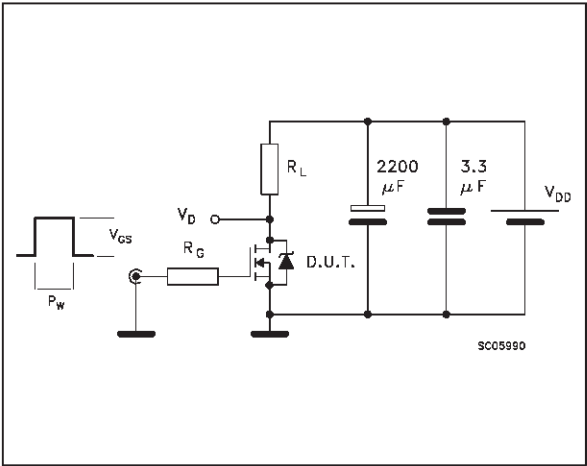


Fig. 4: Gate Charge test Circuit

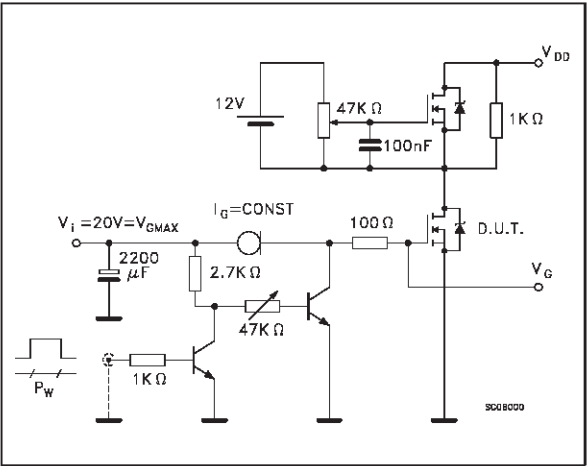
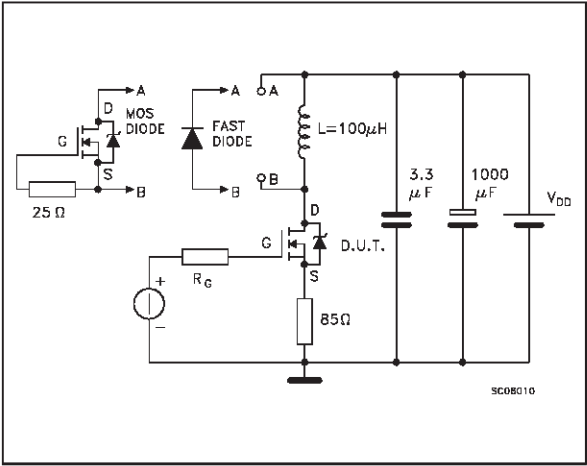
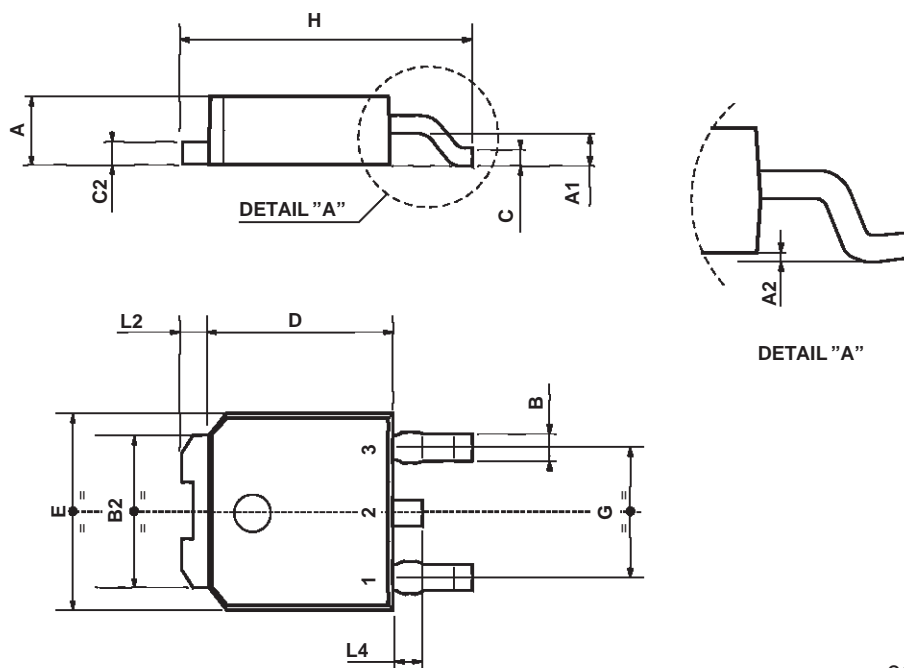


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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