



# STD5NM50 STD5NM50-1

N-CHANNEL 500V - 0.7Ω - 7.5A DPAK/IPAK  
MDmesh™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD5NM50	500V	<0.8Ω	7.5 A
STD5NM50-1	500V	<0.8Ω	7.5 A

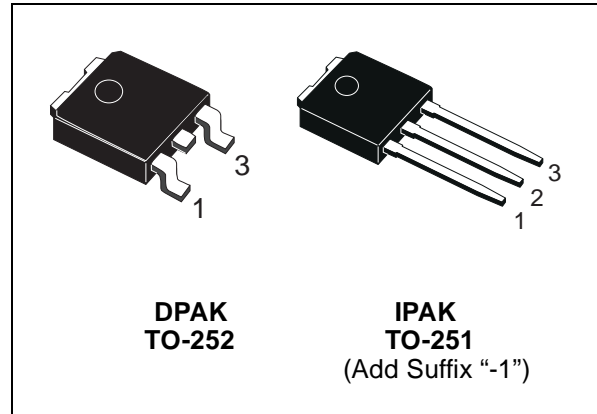
- TYPICAL R<sub>DS(on)</sub> = 0.7Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

## DESCRIPTION

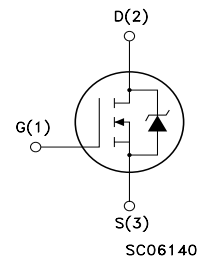
The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

## APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



## INTERNAL SCHEMATIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	500	V
V <sub>GS</sub>	Gate- source Voltage	±30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	7.5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	4.7	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	30	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	100	W
	Derating Factor	0.8	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T <sub>stg</sub>	Storage Temperature	– 55 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

(•)Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 5A, di/dt ≤ 400A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

## STD5NM50/STD5NM50-1

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.25	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	2.5	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	300	mJ

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 µA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	µA µA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.5A		0.7	0.8	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 25V <sub>x</sub> , I <sub>D</sub> = 2.5A		3.5		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		415		pF
C <sub>oss</sub>	Output Capacitance			88		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			12		pF
C <sub>oss</sub> eq. (2)	Equivalent Output Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 400V		50		pF
R <sub>G</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3		Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

2. C<sub>oss</sub> eq. is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**  
**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V$ , $I_D = 2.5A$		16		ns
$t_r$	Rise Time	$R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see test circuit, Figure 3)		8		ns
$Q_g$	Total Gate Charge	$V_{DD} = 400V$ , $I_D = 7.5A$		13		nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 10V$		5		nC
$Q_{gd}$	Gate-Drain Charge			6		nC

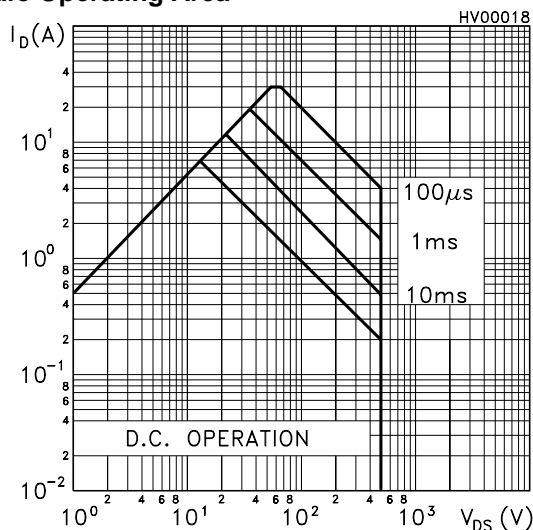
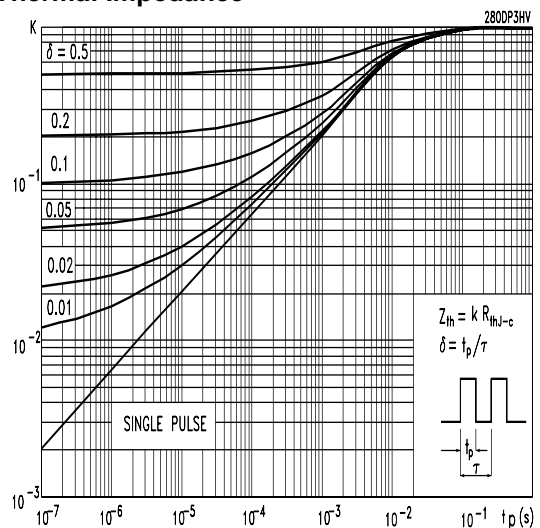
**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_r(V_{off})$	Off-voltage Rise Time	$V_{DD} = 400V$ , $I_D = 5A$ ,		14		ns
$t_f$	Fall Time	$R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see test circuit, Figure 5)		6		ns
$t_c$	Cross-over Time			13		ns

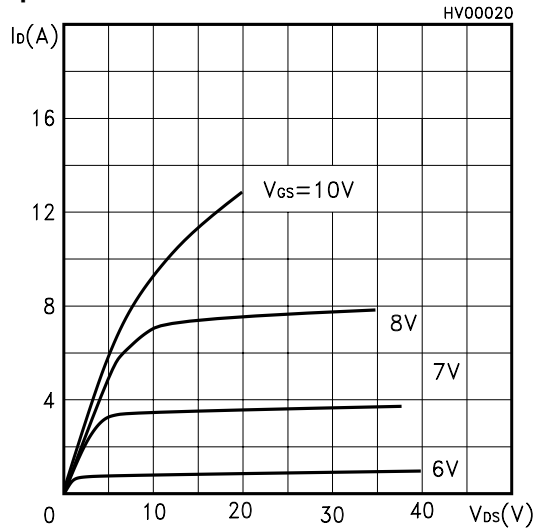
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				7.5	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				30	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 7.5A$ , $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 5A$ , $di/dt = 100A/\mu s$ ,		185		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 100V$ , $T_j = 25^\circ C$ (see test circuit, Figure 5)		1.1		$\mu C$
$I_{RRM}$	Reverse Recovery Current			11.5		A
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 5A$ , $di/dt = 100A/\mu s$ ,		270		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 100V$ , $T_j = 150^\circ C$ (see test circuit, Figure 5)		1.6		$\mu C$
$I_{RRM}$	Reverse Recovery Current			12		A

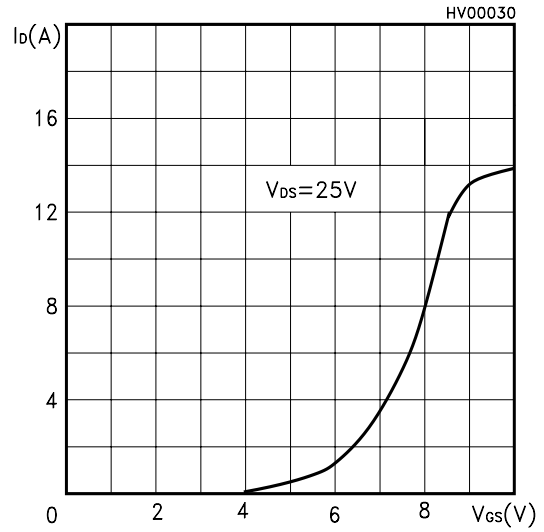
Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
 2. Pulse width limited by safe operating area.

**Safe Operating Area**

**Thermal Impedance**


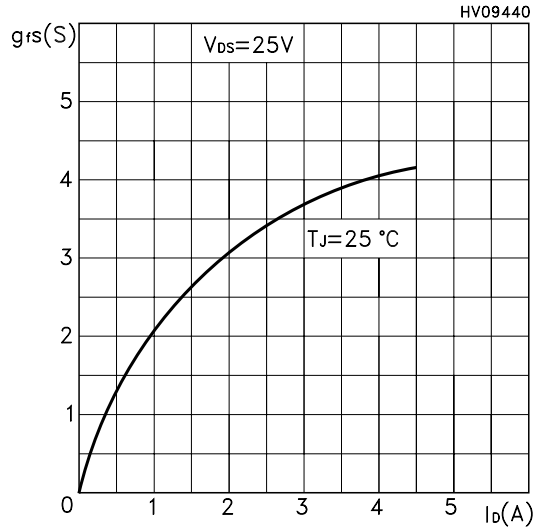
Output Characteristics



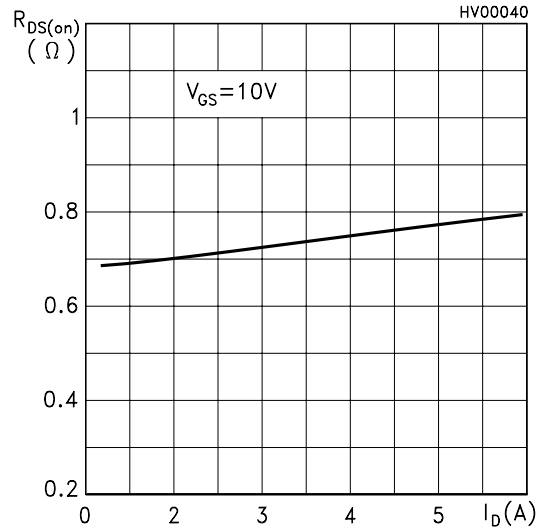
Transfer Characteristics



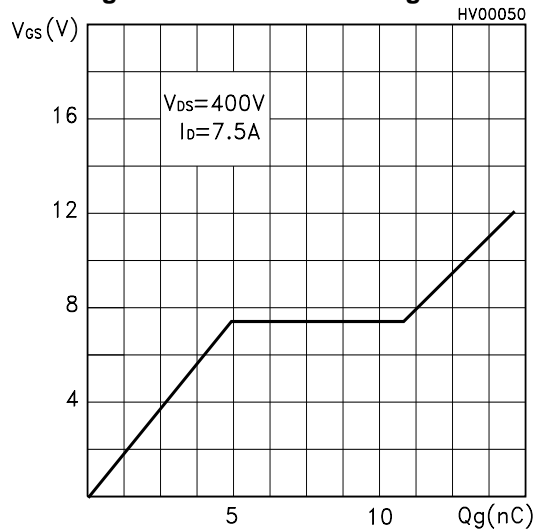
Transconductance



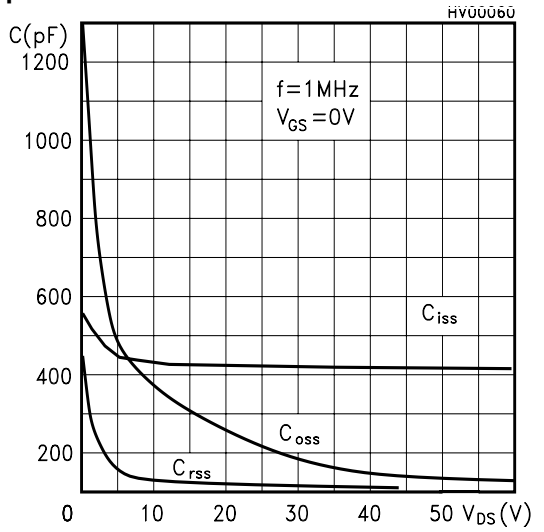
Static Drain-source On Resistance



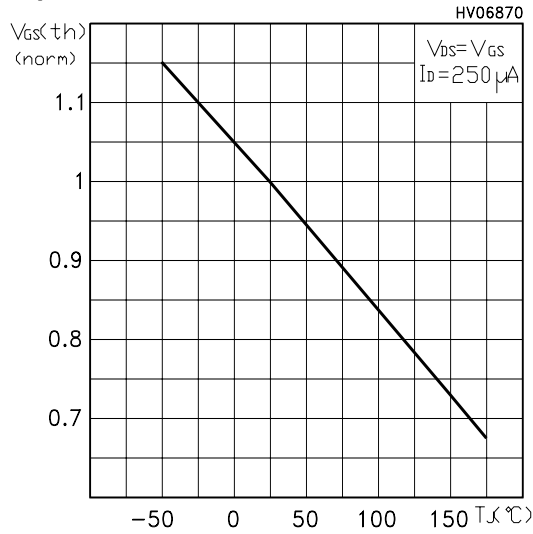
Gate Charge vs Gate-source Voltage



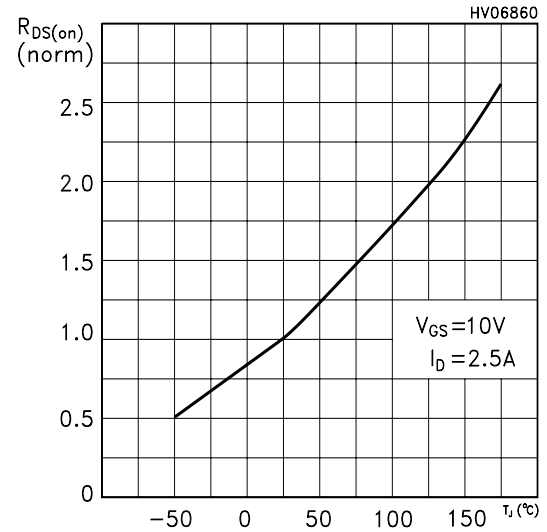
Capacitance Variations



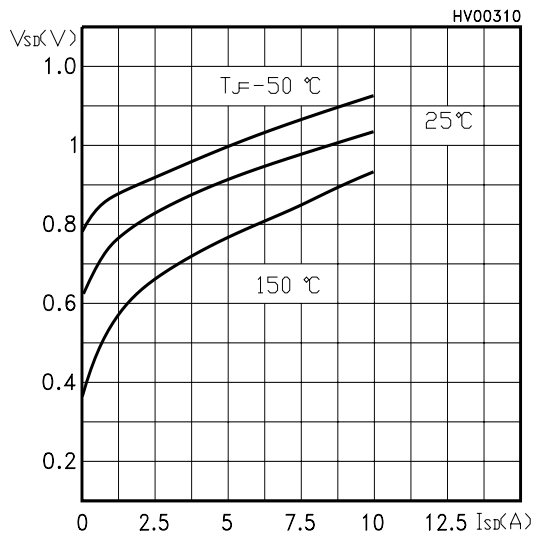
**Normalized Gate Threshold Voltage vs Temperature**



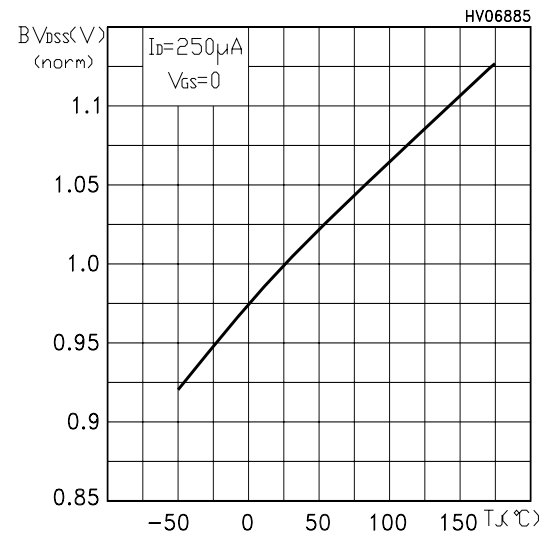
**Normalized On Resistance vs Temperature**



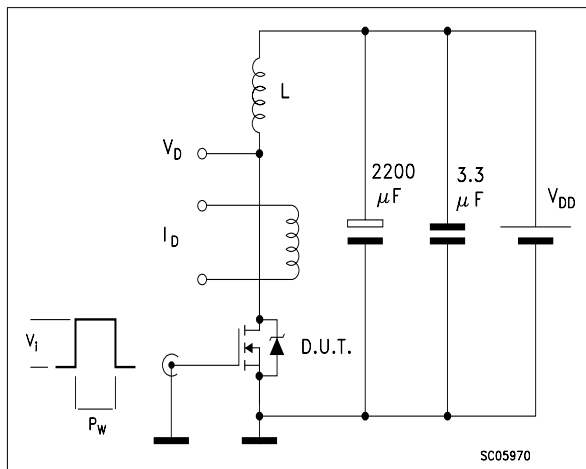
**Source-drain Diode Forward Characteristics**



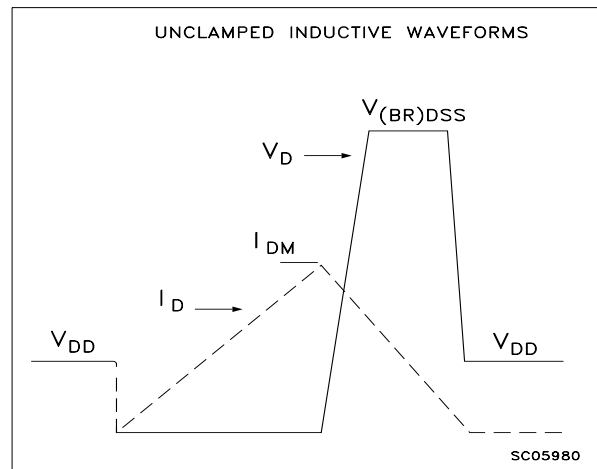
**Normalized BVDSS vs Temperature**



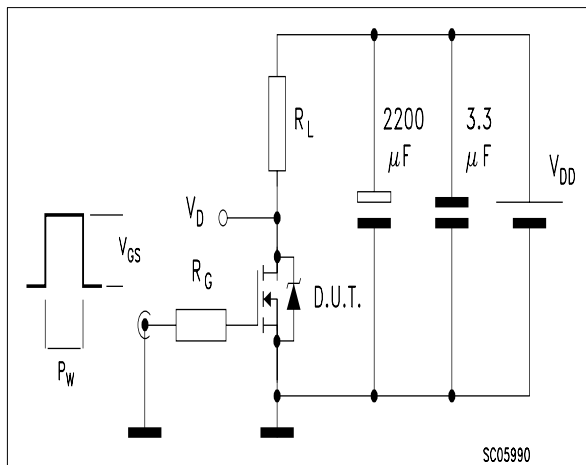
**Fig. 1: Unclamped Inductive Load Test Circuit**



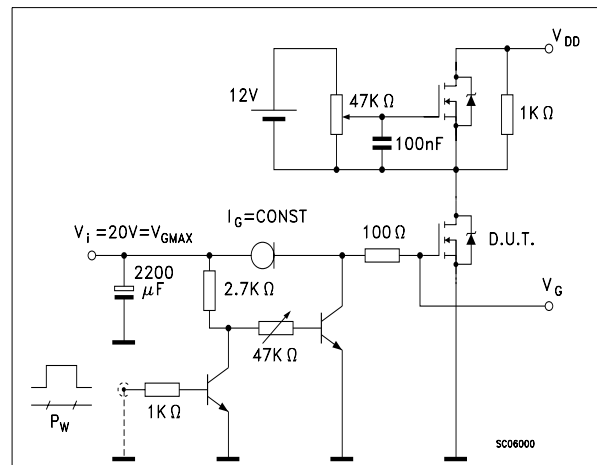
**Fig. 2: Unclamped Inductive Waveform**



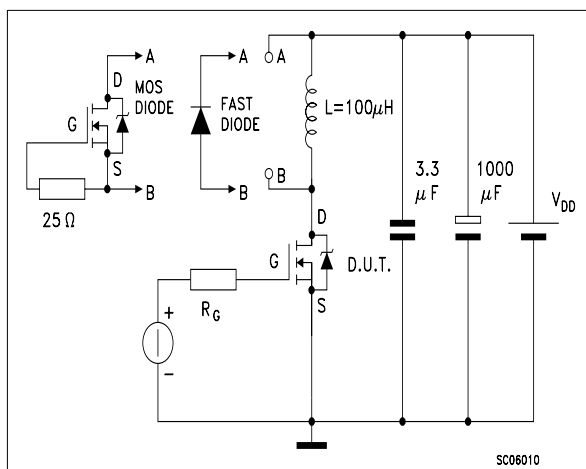
**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

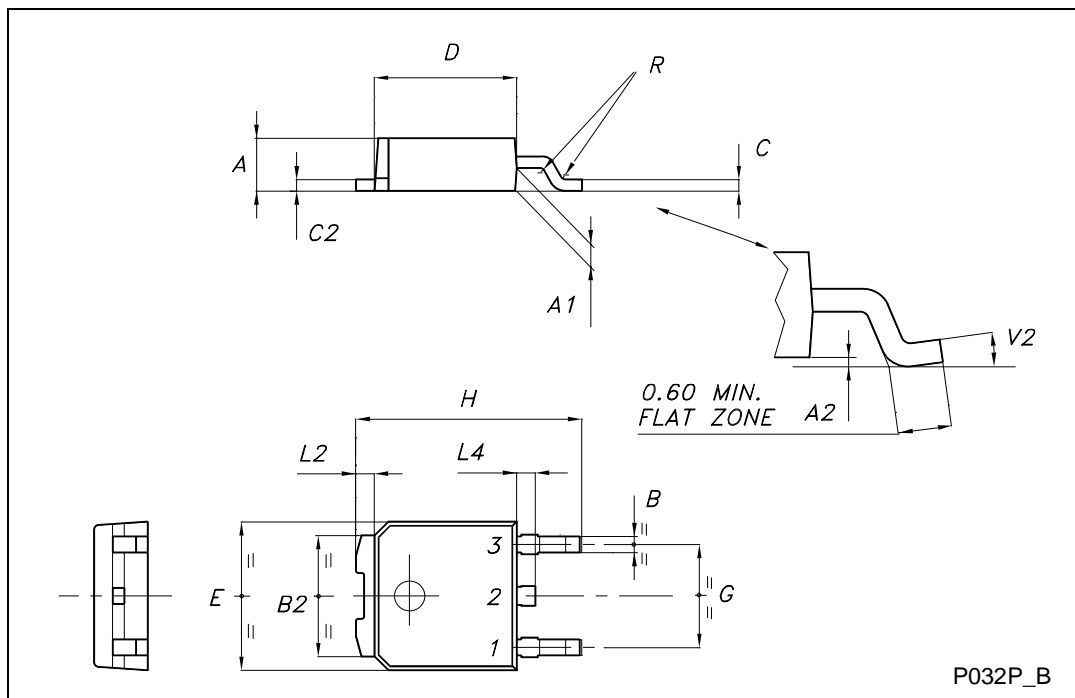


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



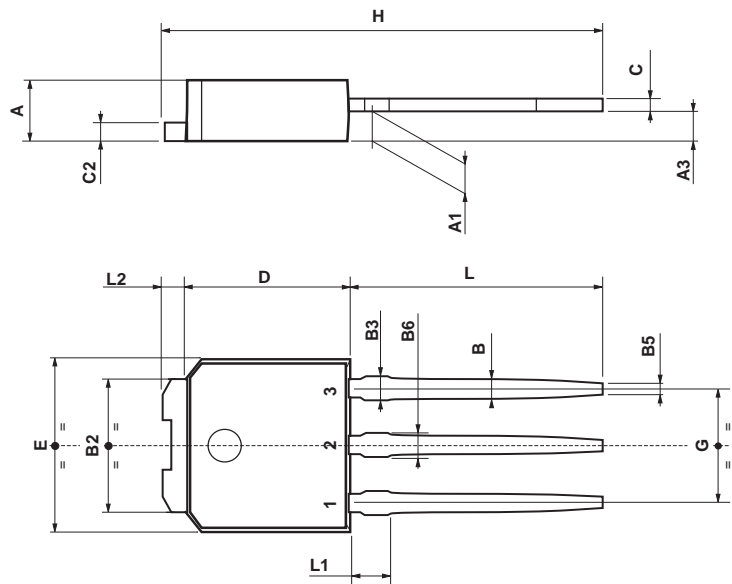
## TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



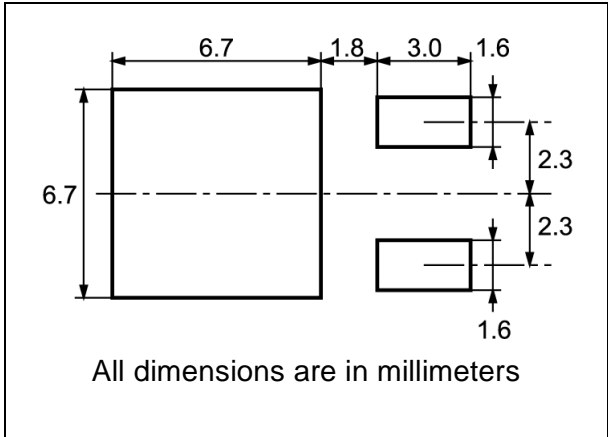
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

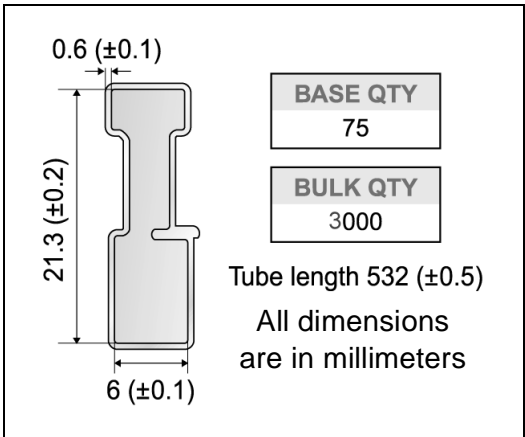




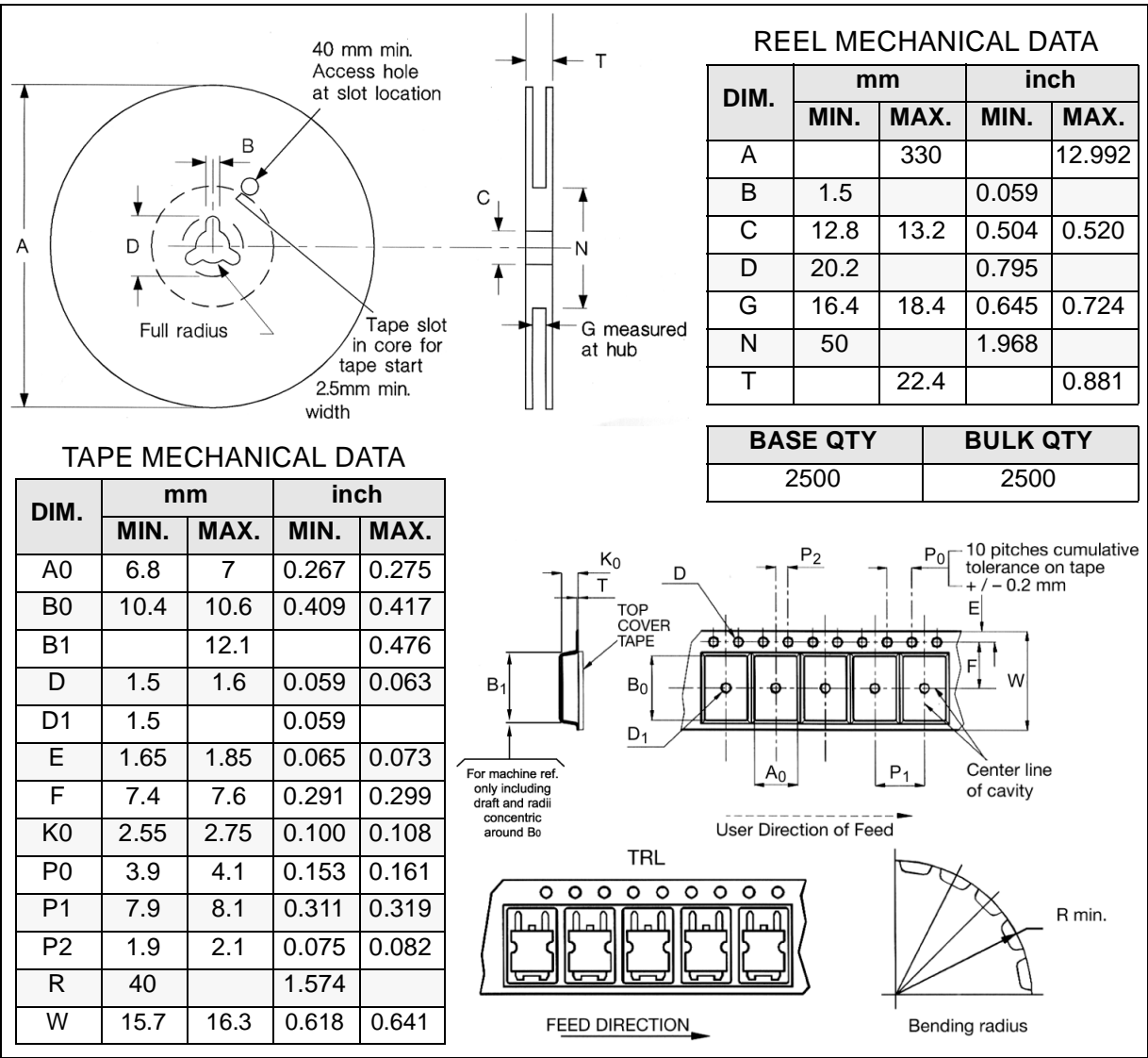
### DPAK FOOTPRINT



### TUBE SHIPMENT (no suffix)\*



### TAPE AND REEL SHIPMENT (suffix "T4")\*



\* on sales type

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>