



STP9NK80Z STF9NK80Z

N-CHANNEL 800V -0.9Ω - 7.5A TO-220/TO-220FP Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP9NK80Z	800 V	<1.2 Ω	7.5 A	150 W
STF9NK80Z	800 V	<1.2 Ω	7.5 A	35 W

- TYPICAL R_{DS(on)} = 0.9Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES
- SMPS

Figure 1: Package

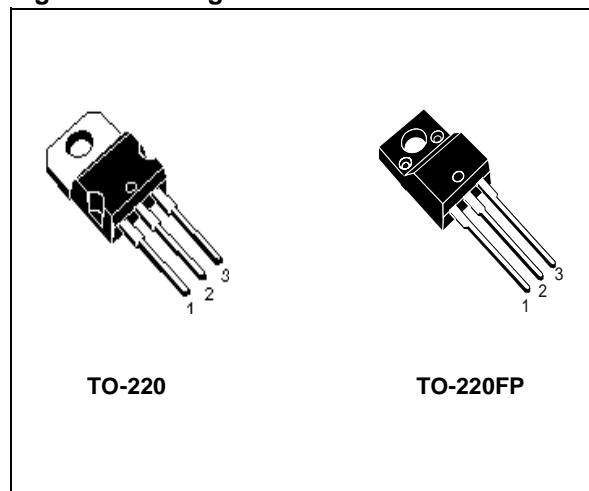


Figure 2: Internal Schematic Diagram

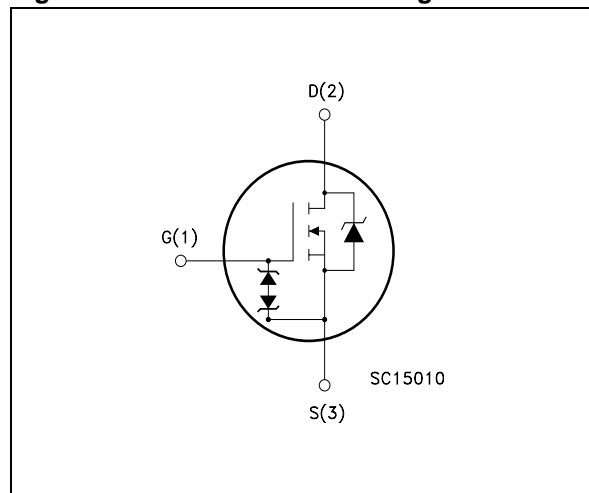


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP9NK80Z	P9NK80Z	TO-220	TUBE
STF9NK80Z	F9NK80Z	TO-220FP	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	800		V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	800		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	7.5	7.5 (*)	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	4.7	4.7 (*)	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	30	30 (*)	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	150	35	W
	Derating Factor	1.20	0.28	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	4000		V
$dv/dt(1)$	Peak Diode Recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		$^\circ\text{C}$ $^\circ\text{C}$

(●) Pulse width limited by safe operating area

(1) $I_{SD} \leq 7.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	0.83	3.6	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		$^\circ\text{C}/\text{W}$
T_I	Maximum Lead Temperature For Soldering Purpose	350		$^\circ\text{C}$

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	7.5	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	350	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{gs} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}\text{C}$ UNLESS OTHERWISE SPECIFIED)**Table 7: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	800			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 100\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 3.75\text{ A}$		0.9	1.2	Ω

Table 8: DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 3.75\text{ A}$		7.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1900 180 38		pF pF pF
$C_{oss\text{ eq. (3)}}$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 640\text{V}$		75		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 400\text{ V}$, $I_D = 3.75\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 19)		26 19 58 18		ns ns ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 640\text{ V}$, $I_D = 7.5\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 20)		12 10 24		ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 640\text{V}$, $I_D = 7.5\text{ A}$, $V_{GS} = 10\text{V}$ (see Figure 22)		60 12 35	84	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				7.5 30	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 7.5\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 7.5\text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 35\text{V}$, $T_j = 25^{\circ}\text{C}$ (see Figure 20)		530 4.5 17		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 7.5\text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 35\text{V}$, $T_j = 150^{\circ}\text{C}$ (see Figure 20)		690 6.4 17		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Safe Operating Area for TO-220

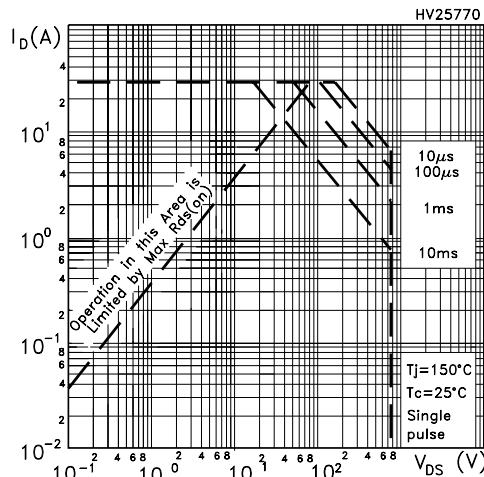


Figure 4: Safe Operating Area for TO-220FP

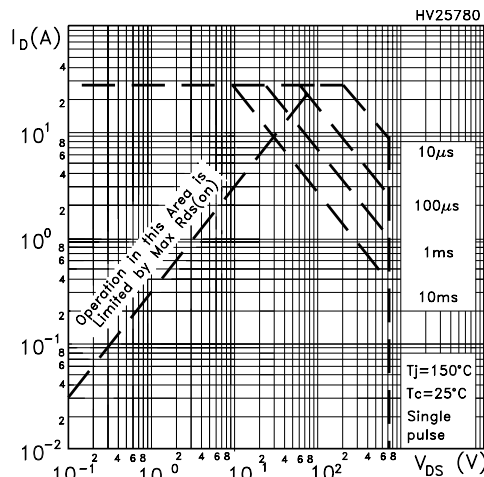


Figure 5: Output Characteristics

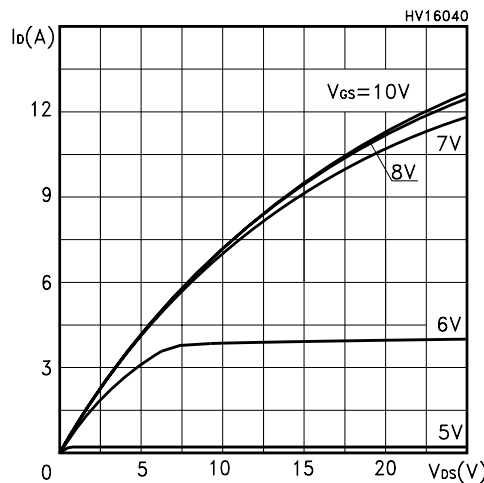


Figure 6: Thermal Impedance for TO-220

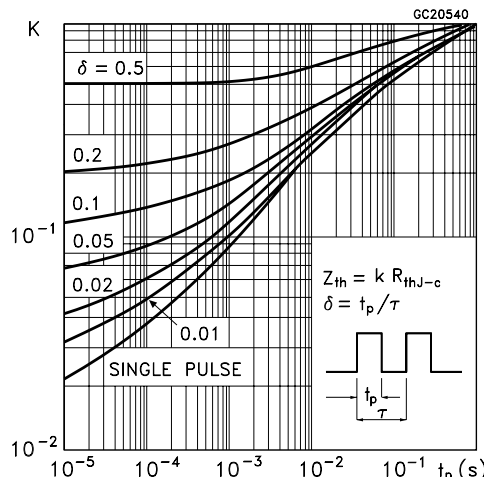


Figure 7: Thermal Impedance for TO-220FP

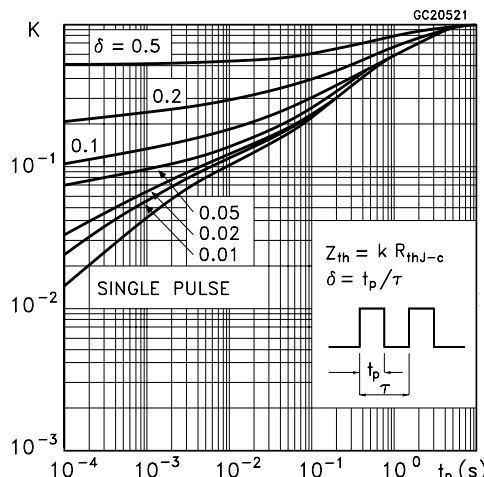


Figure 8: Transfer Characteristics

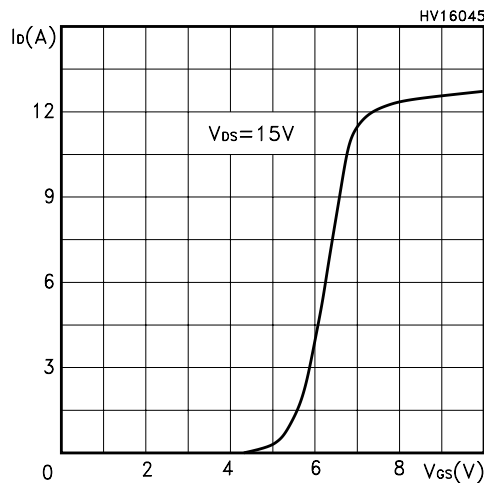


Figure 9: Transconductance

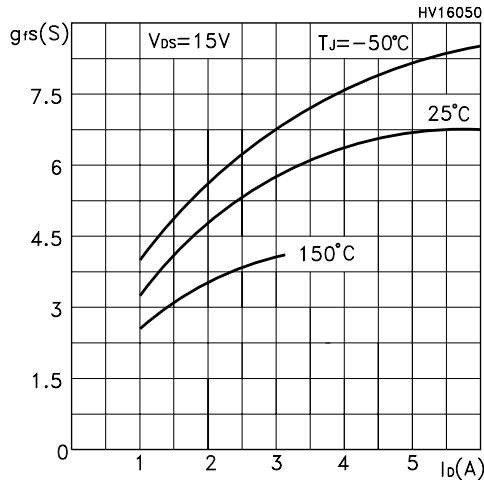


Figure 10: Gate Charge vs Gate-source Voltage

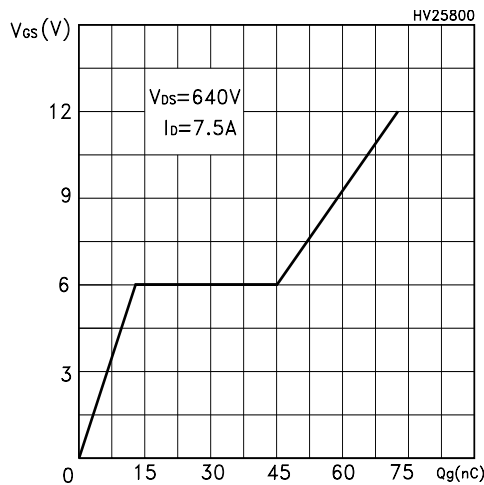


Figure 11: Normalized Gate Threshold Voltage vs Temperature

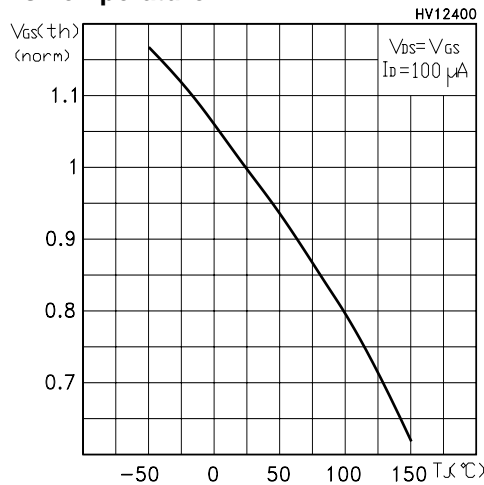


Figure 12: Static Drain-source On Resistance

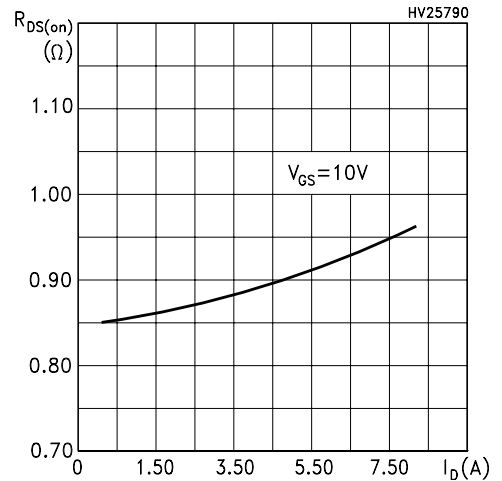


Figure 13: Capacitance Variations

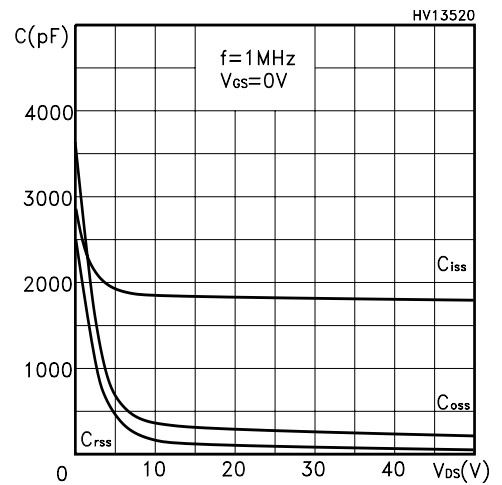


Figure 14: Normalized BVDSS vs Temperature

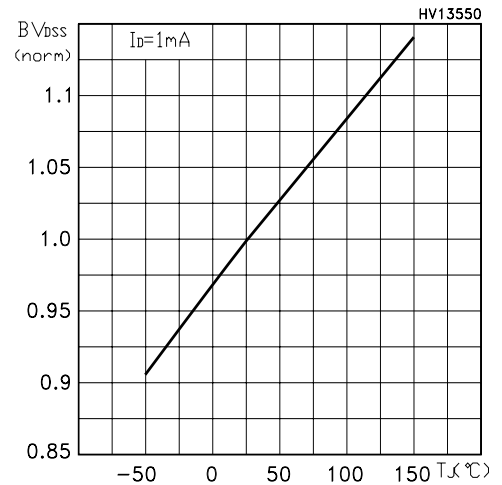


Figure 15: Normalized On Resistance vs TemperatureS

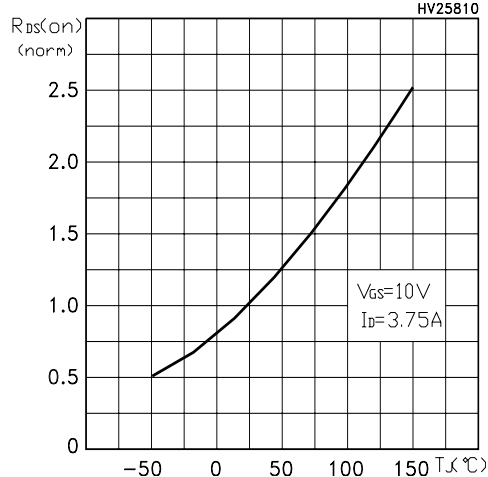


Figure 16: Avalanche Energy vs Temperature

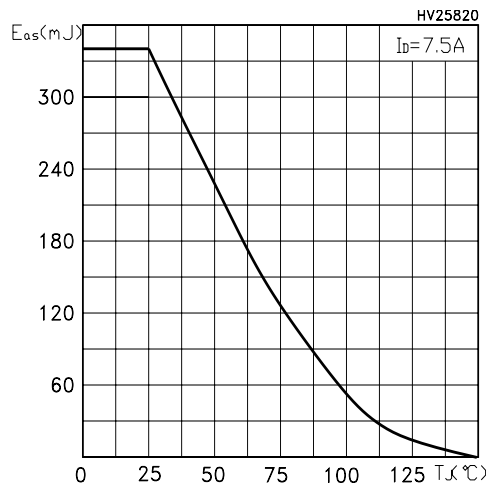


Figure 17: Source-Drain Diode Forward Characteristics

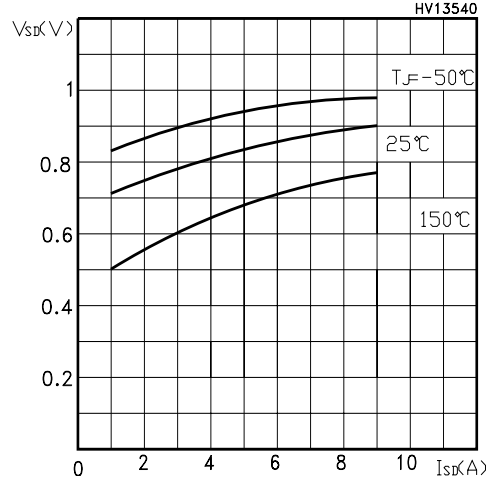


Figure 18: Unclamped Inductive Load Test Circuit

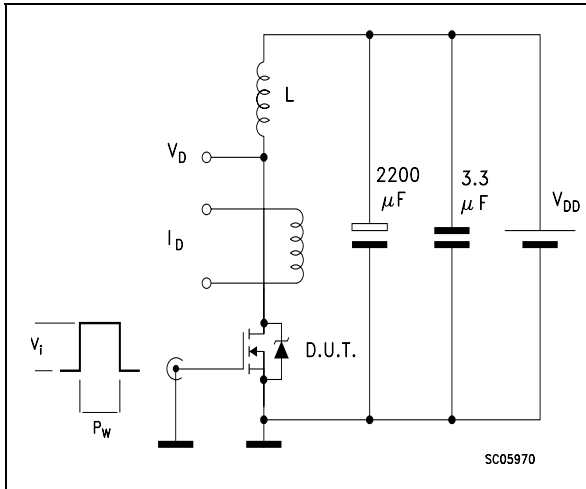


Figure 19: Switching Times Test Circuit For Resistive Load

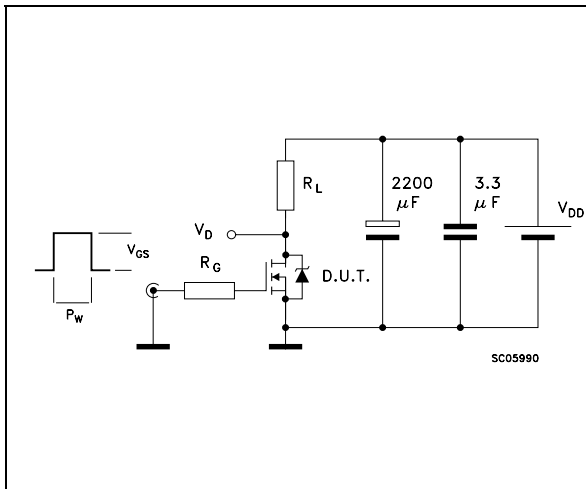


Figure 20: Test Circuit For Inductive Load Switching and Diode Recovery Times

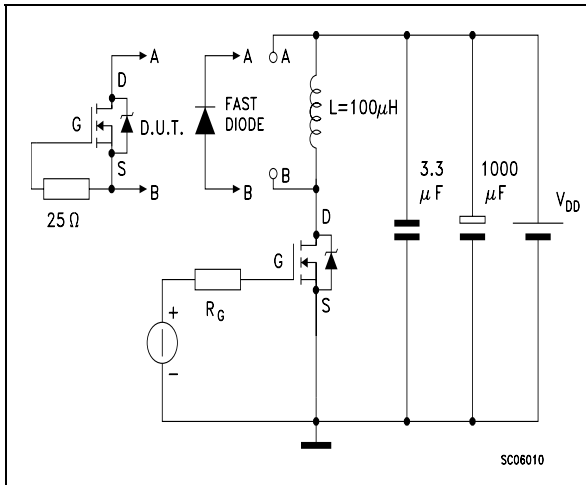


Figure 21: Unclamped Inductive Waform

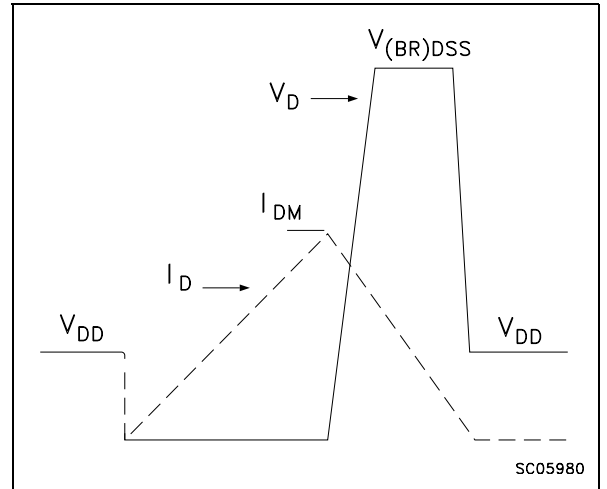
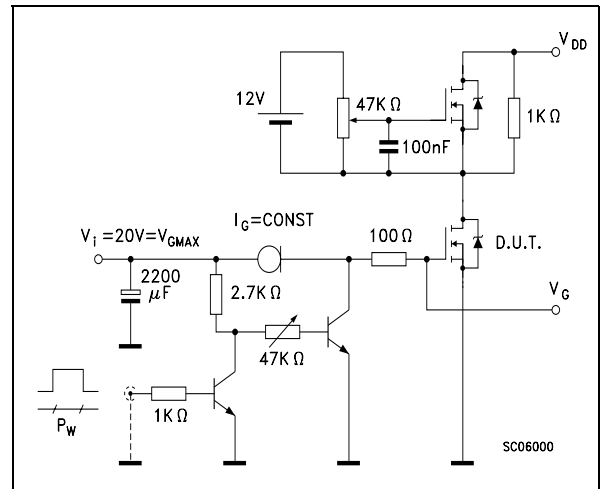
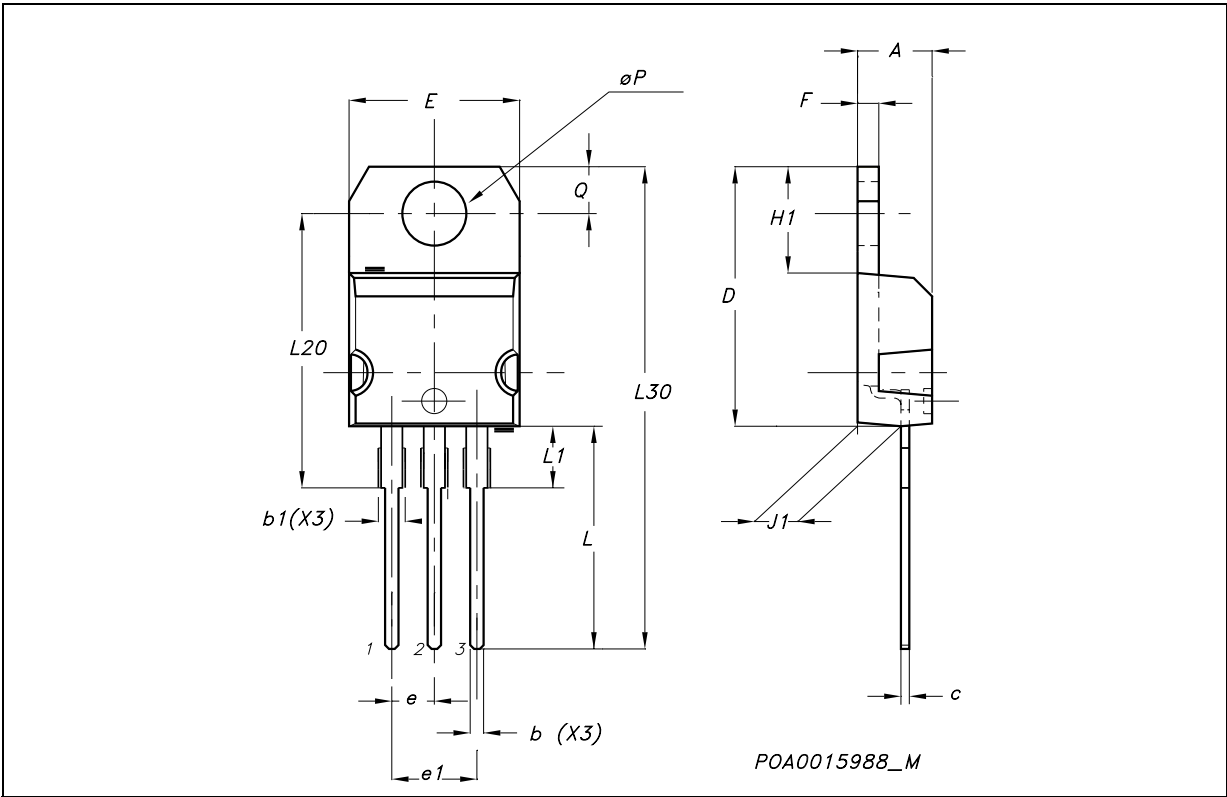


Figure 22: Gate Charge Test Circuit



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

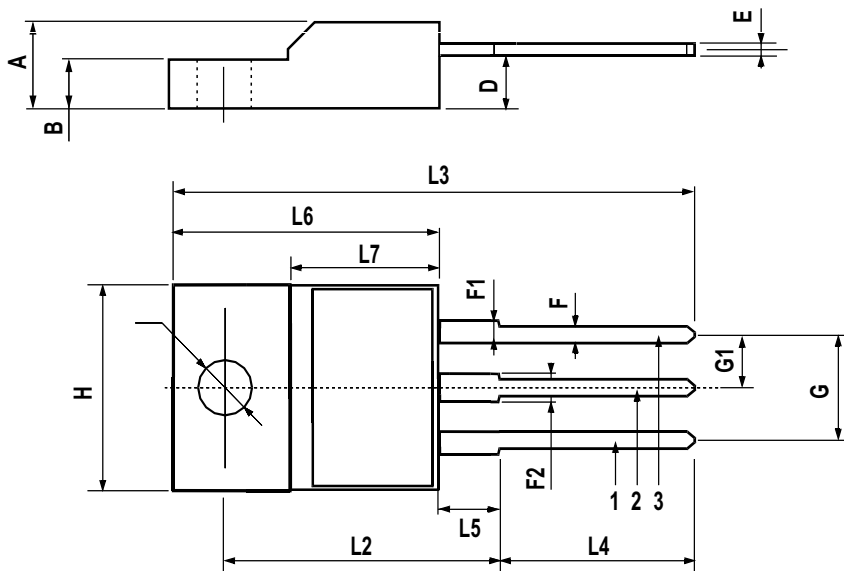


Table 10: Revision History

Date	Revision	Description of Changes
18-May-2005	1	First Release.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2005 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America