



Single chip 802.11b/g WLAN radio

DATA BRIEF

Features

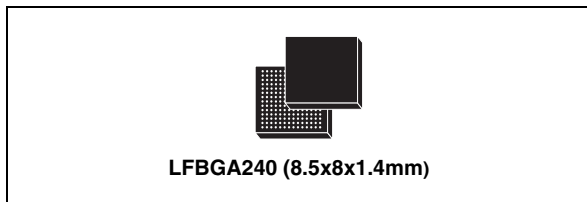
- Extremely small footprint
- Ultra Low Power consumption
- Fully compliant with the IEEE 802.11b and 802.11g WLAN standards
- Support for 54, 48, 36, 24, 18, 12, 9, and 6Mbps OFDM, 11 and 5.5Mbps CCK and legacy 2 and 1Mbps data rates
- Single Chip 802.11b/g WLAN solution with
- Fully integrated:
 - Zero IF (ZIF) transceiver,
 - Voltage Controlled Oscillator (VCO),
 - High-Speed A/ D and D/A Converters,
 - Radio Power Management Unit (PMU),
 - OFDM and CCK baseband processor,
 - ARM9 Media Access Controller (MAC),
 - SPI serial host interface
 - SDIO (4-bit) serial host interface
 - Passive components integration
 - PA bias control
 - Flexible integrated Power Management Unit
 - Glueless FEM interface
- Intelligent Power Control, Including 802.11 Power Save Mode
- Fully integrated Bluetooth coexistence

Applications

- Cellular Phones
- Personal Digital Assistants (PDA)
- Portable Computers
- Hand-held Data Transfer Devices
- Cameras
- Computer Peripherals
- Cable Replacement

Order codes

Part number	Temp range, °C	Package	Packing
STLC4550	-30 to 85°C	LFBGA240- (8.5x8x1.4mm)	Tray



Description

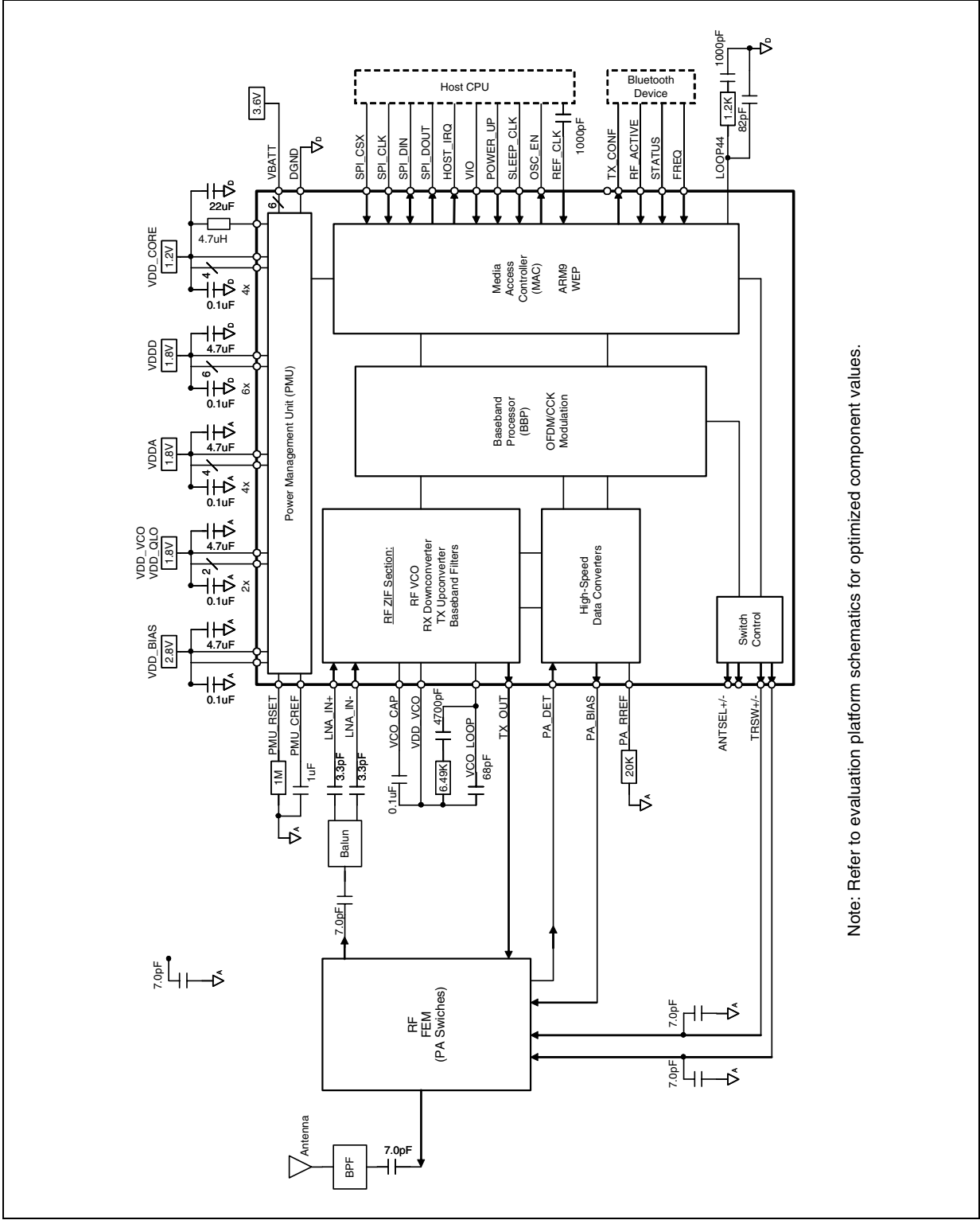
The STLC4550 is a single chip 802.11b/g WLAN radio for embedded, low-power and very small form factor mobile applications. The product conforms to the IEEE 802.11b and 802.11g protocols operating in the 2.45GHz ISM frequency band supporting OFDM data rates of 54, 48, 36, 24, 18, 12, 9, and 6Mbps as well as CCK data rates of 11 and 5.5Mbps and legacy data rates of 2 and 1Mbps.

The STLC4550 is a fully integrated wireless radio including a ZIF transceiver, RDocRev1F Synthesizer/VCO, high-speed data converters, an OFDM/CCK digital baseband processor, an ARM9-based MAC and a complete Power Management Unit with integrated PA bias control. In addition some passive components are integrated further reducing the overall reference design cost and size. An external FEM completes a highly integrated chip set solution.

Host control is provided by a flexible SPI or SDIO serial interface. The SPI interface supports a maximum clock rate of 48MHz whereas the SDIO supports a maximum clock rate of xxMHz. For maximum flexibility, the STLC4550 accepts system reference clock frequencies of 19.2, 26, 38.4 and 40MHz. A reference design evaluation platform of hardware and software is provided to system integrators to rapidly enable wireless connectivity to mobile platforms.

1 Block diagram & Application circuit

Figure 1. Block Diagram and Application Circuit (Standard Front End Module)

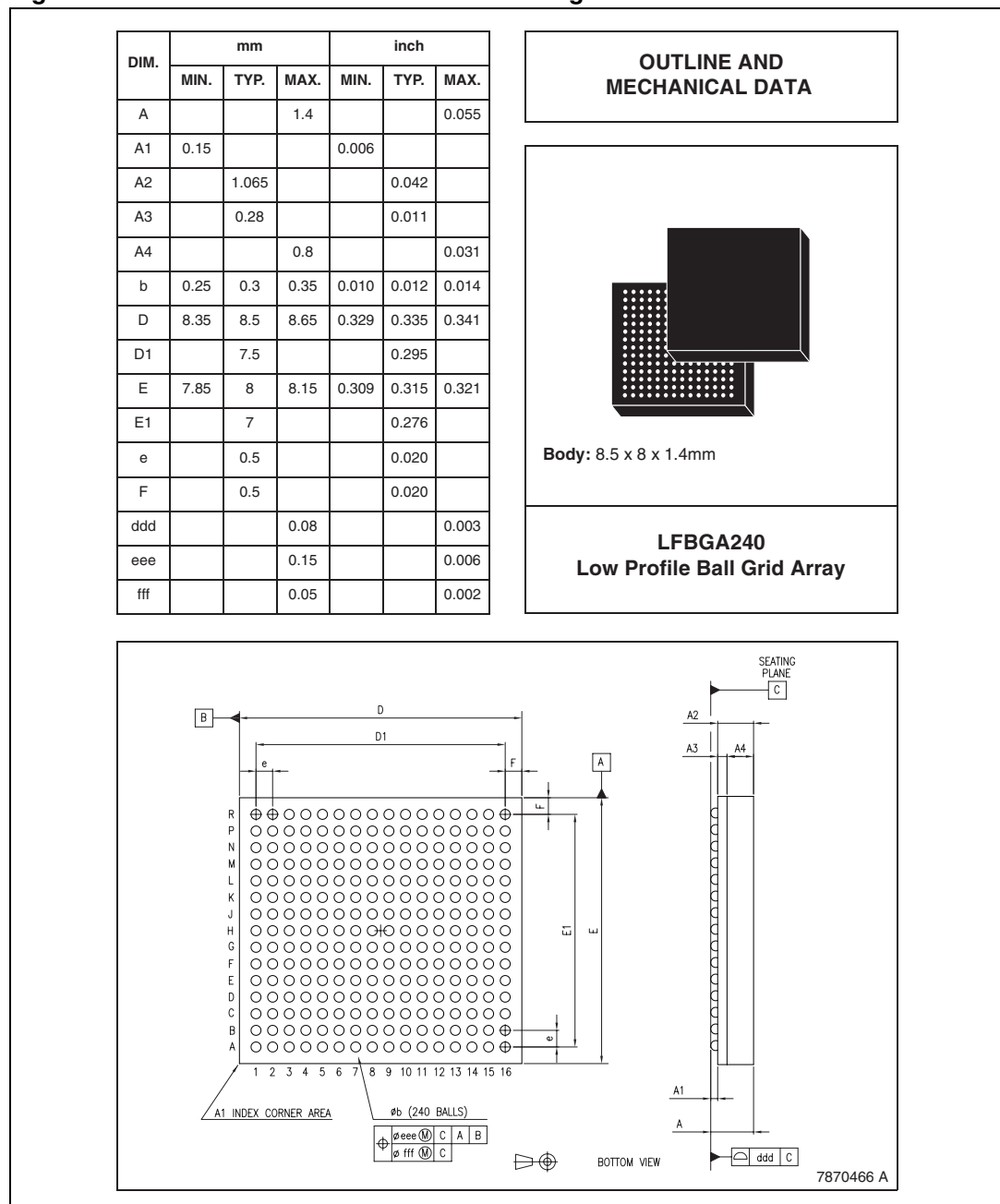


2 Package Information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. LFBGA240 Mechanical Data & Package Dimensions



3 Revision history

Table 1. Document revision history

Date	Revision	Changes
06-Feb-2006	1	Initial release.

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