

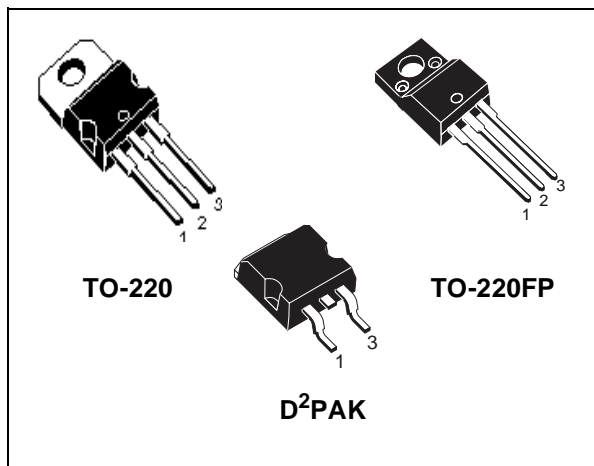


STP6NK90Z - STP6NK90ZFP STB6NK90Z

N-CHANNEL 900V - 1.56Ω - 5.8A TO-220/TO-220FP/D²PAK
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP6NK90Z	900 V	< 2 Ω	5.8 A	140 W
STP6NK90ZFP	900 V	< 2 Ω	5.8 A	30 W
STB6NK90Z	900 V	< 2 Ω	5.8 A	140 W

- TYPICAL R_{DS(on)} = 1.56 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



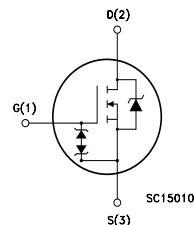
DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP6NK90Z	P6NK90Z	TO-220	TUBE
STP6NK90ZFP	P6NK90ZFP	TO-220FP	TUBE
STB6NK90ZT4	B6NK90Z	D ² PAK	TAPE & REEL

STP6NK90Z - STP6NK90ZFP - STB6NK90Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP6NK90Z / STB6NK90Z	STP6NK90ZFP	
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	900		V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	900		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	5.8	5.8 (*)	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	3.65	3.65 (*)	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	23.2	23.2 (*)	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	140	30	W
	Derating Factor	1.12	0.24	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	4000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V_{iso}	Insulation Withstand Voltage (DC)	--	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		$^\circ\text{C}$

(\bullet) Pulse width limited by safe operating area

(1) $I_{SD} \leq 5.8\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220	D ² PAK	TO-220FP	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.89		4.2	$^\circ\text{C}/\text{W}$
Rthj-pcb	Thermal Resistance Junction-pcb Max (When mounted on minimum Footprint)		60		$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5			$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300			$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5.8	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	300	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}\text{C}$ UNLESS OTHERWISE SPECIFIED)
ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	900			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 100\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 2.9\text{A}$		1.56	2	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15\text{V}$, $I_D = 2.9\text{A}$		5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		1350 130 26		pF pF pF
$C_{oss \text{ eq. (3)}}$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 720V		70		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 450\text{V}$, $I_D = 3\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Resistive Load see, Figure 3)		17 20		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 720\text{V}$, $I_D = 5.8\text{A}$, $V_{GS} = 10\text{V}$		46.5 8.5 25		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 450\text{V}$, $I_D = 3\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Resistive Load see, Figure 3)		45 20		ns ns
$t_r(V_{off})$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 720\text{V}$, $I_D = 5.8\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Inductive Load see, Figure 5)		11 12 20		ns ns ns

SOURCE DRAIN DIODE

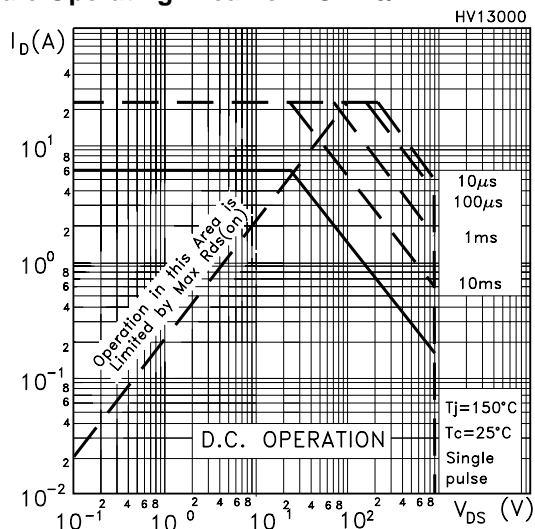
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				5.8 23.2	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 5.8\text{A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5.8\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 36\text{V}$, $T_J = 150^{\circ}\text{C}$ (see test circuit, Figure 5)		840 5880 14		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

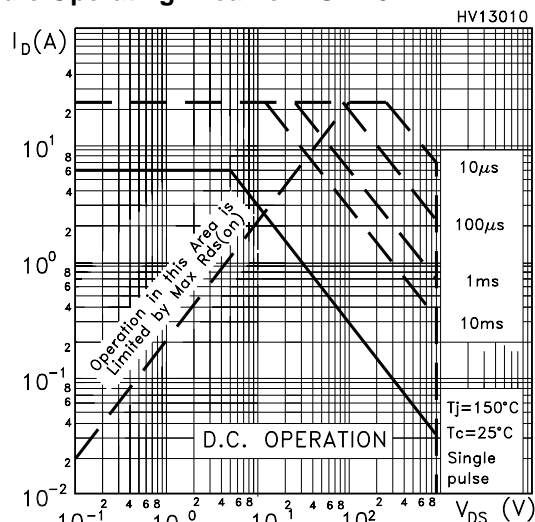
2. Pulse width limited by safe operating area.

3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

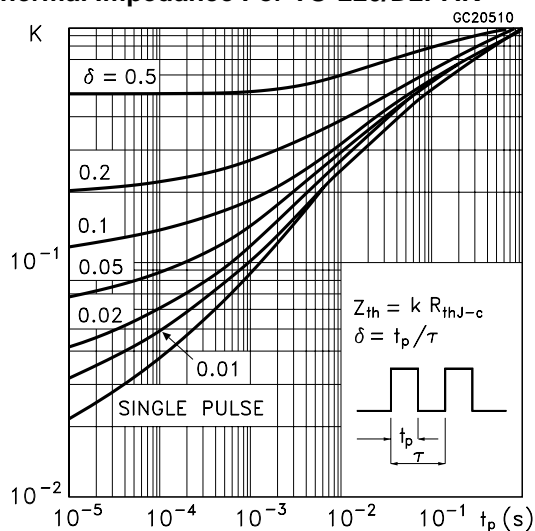
Safe Operating Area For TO-220/D2PAK



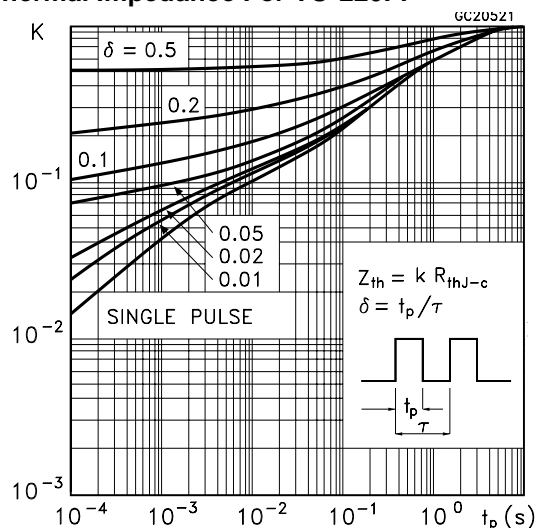
Safe Operating Area For TO-220FP



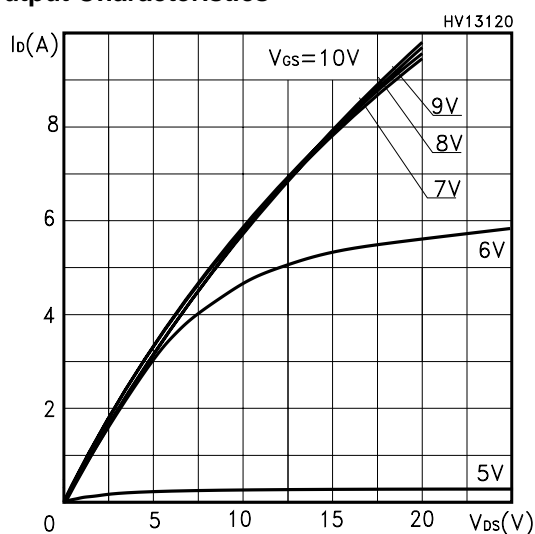
Thermal Impedance For TO-220/D2PAK



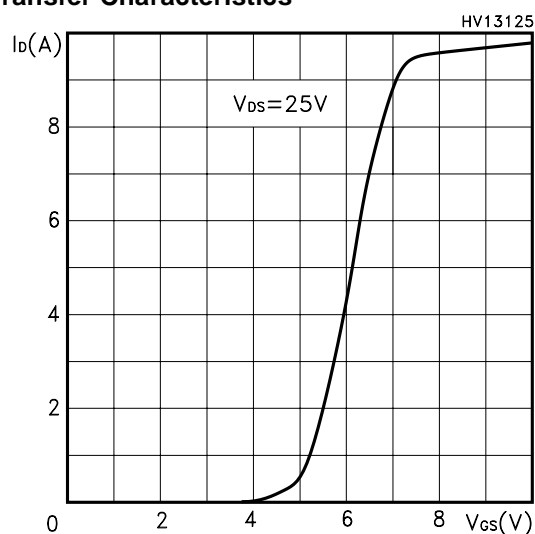
Thermal Impedance For TO-220FP



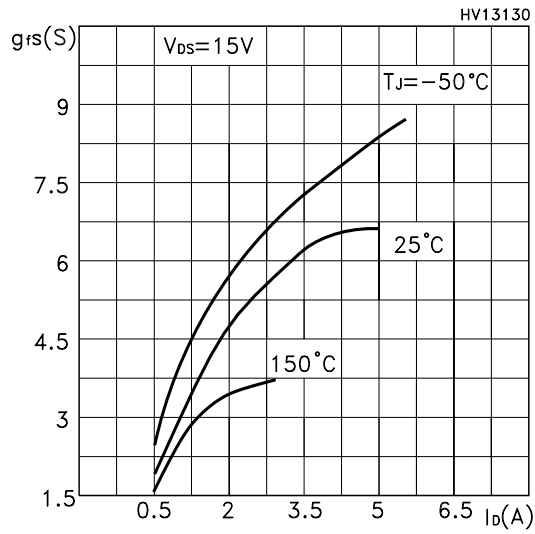
Output Characteristics



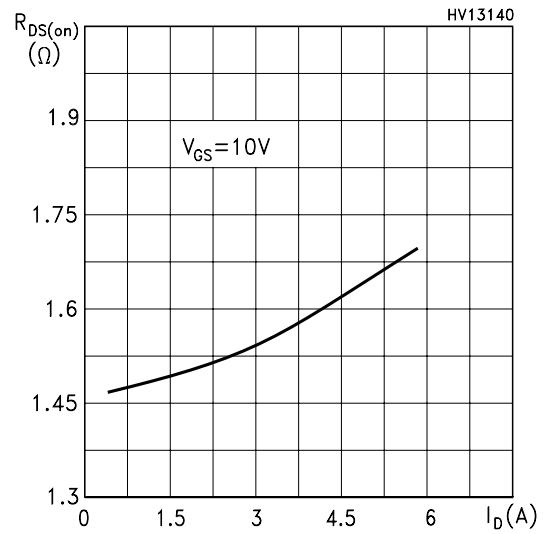
Transfer Characteristics



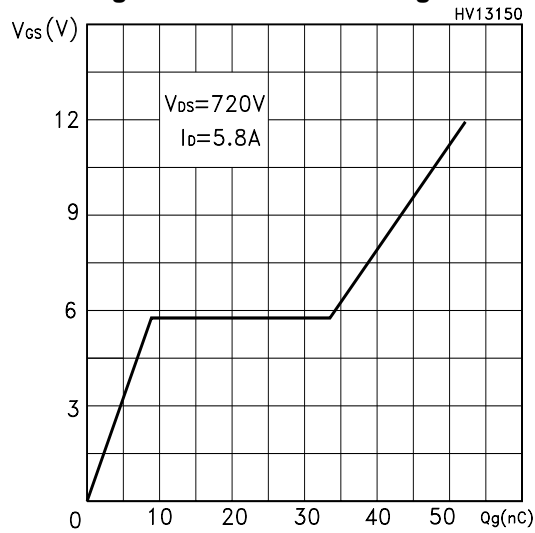
Transconductance



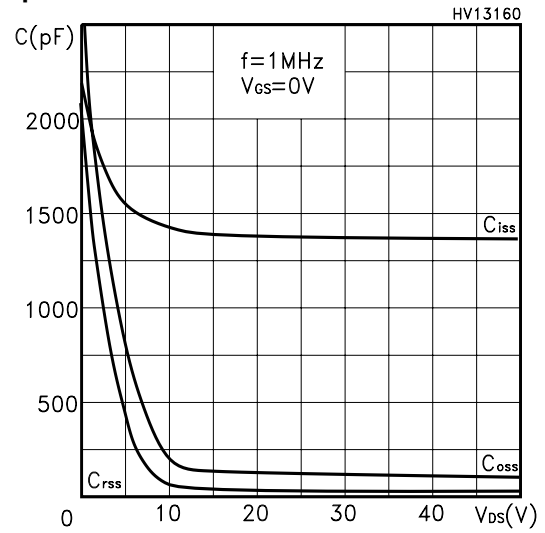
Static Drain-source On Resistance



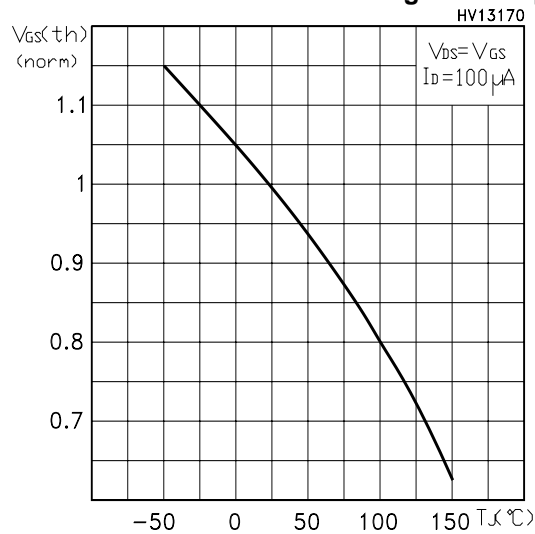
Gate Charge vs Gate-source Voltage



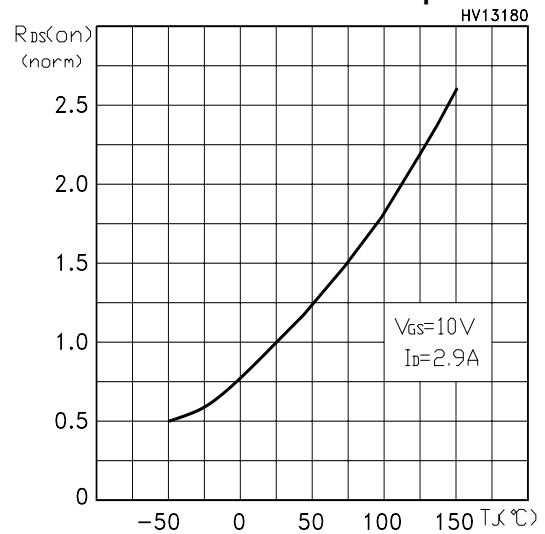
Capacitance Variations



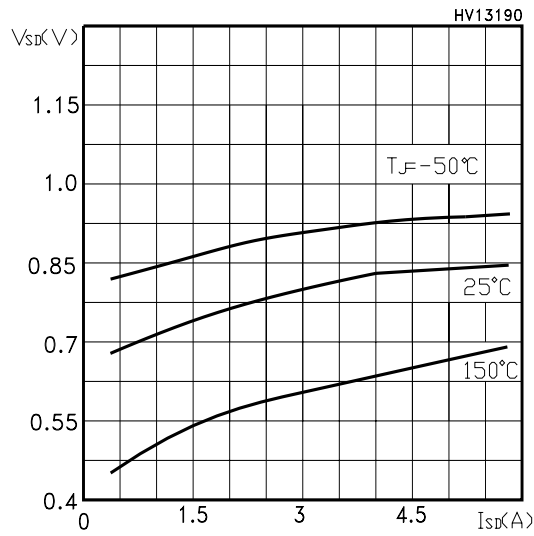
Normalized Gate Threshold Voltage vs Temp.



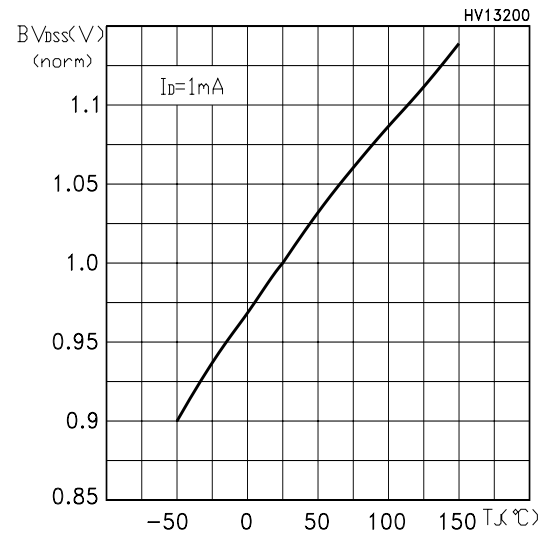
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

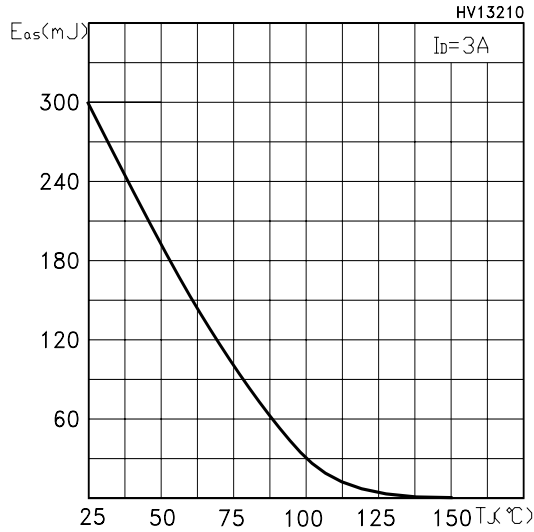


Fig. 1: Unclamped Inductive Load Test Circuit

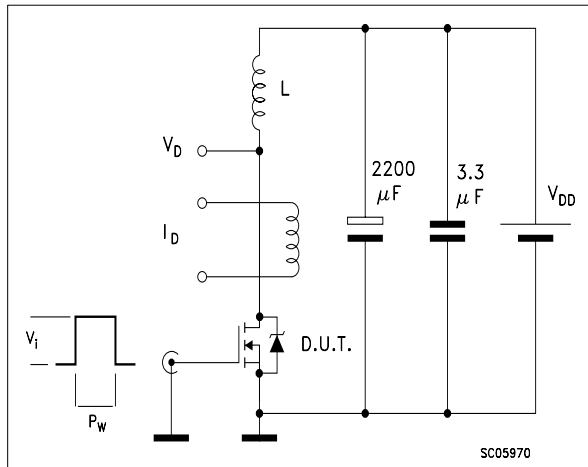


Fig. 2: Unclamped Inductive Waveform

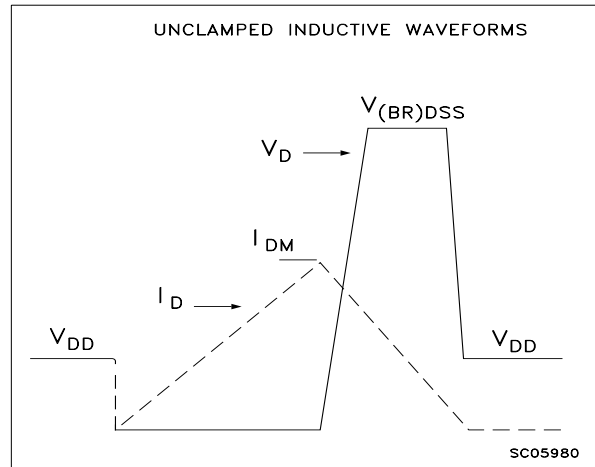


Fig. 3: Switching Times Test Circuit For Resistive Load

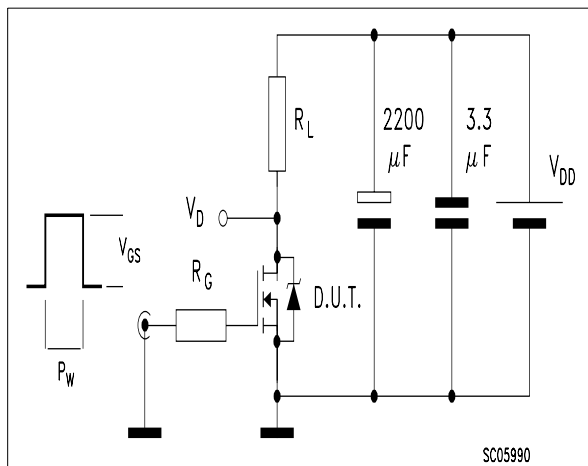


Fig. 4: Gate Charge test Circuit

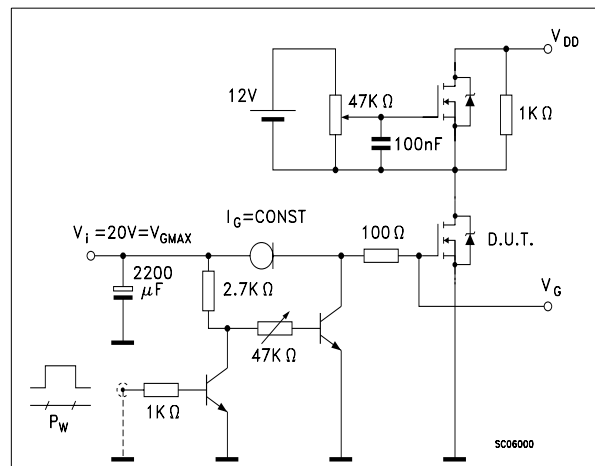
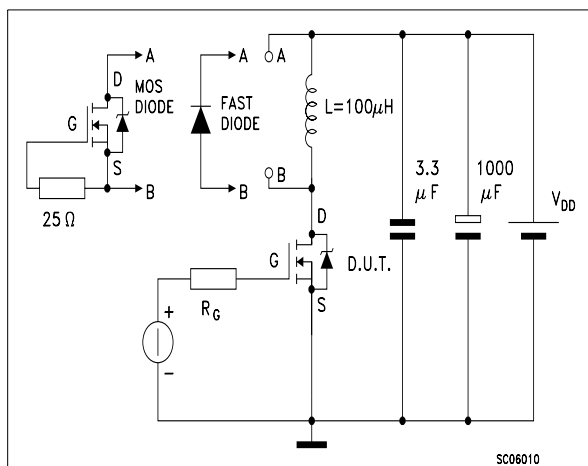
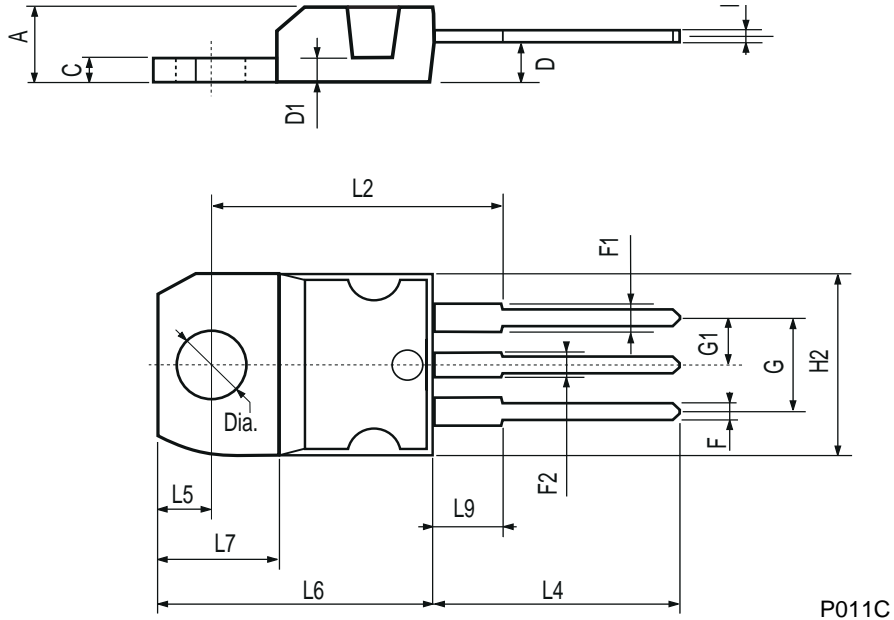


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



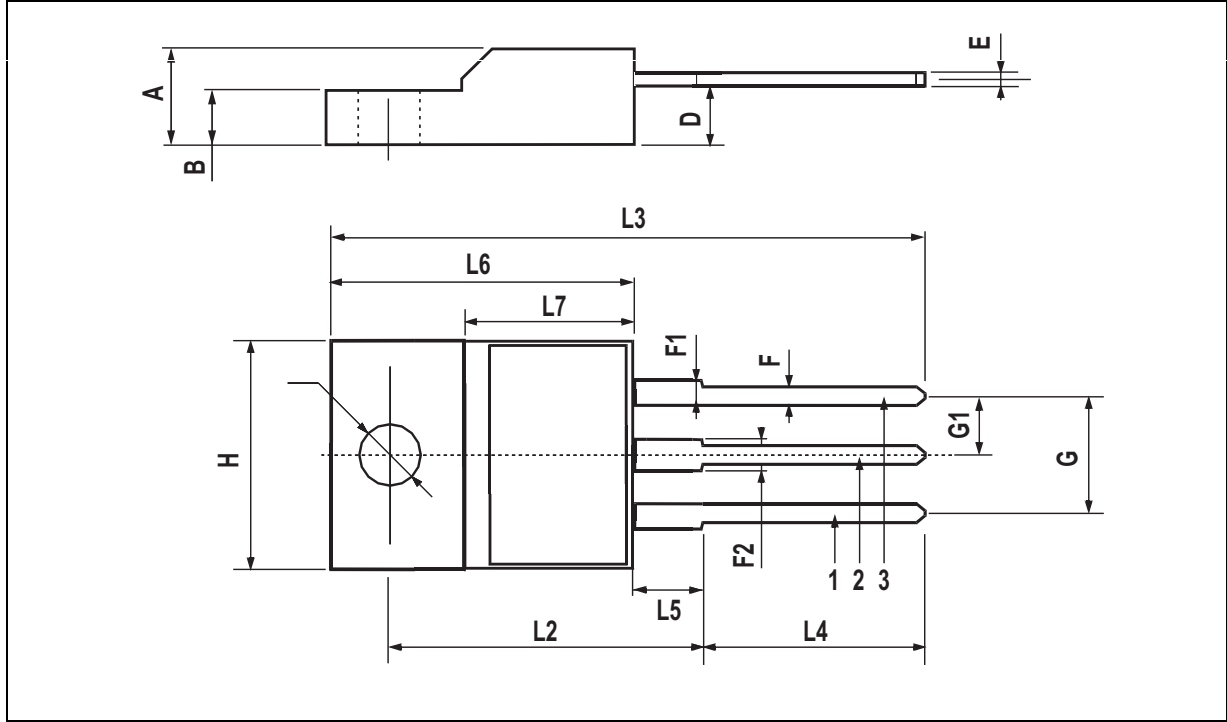
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



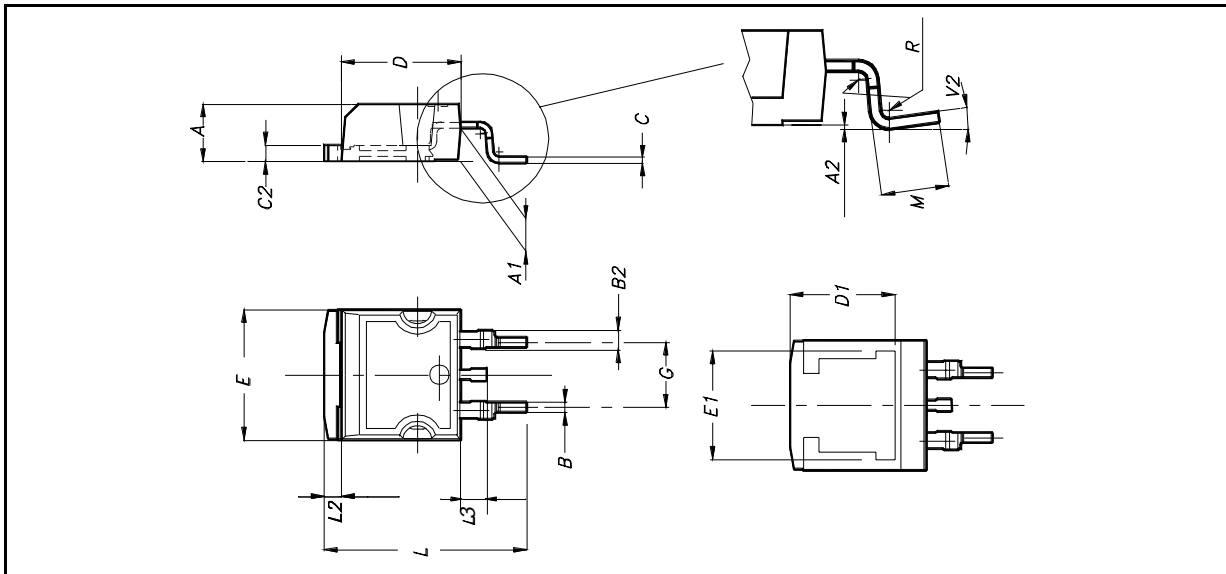
TO-220FP MECHANICAL DATA

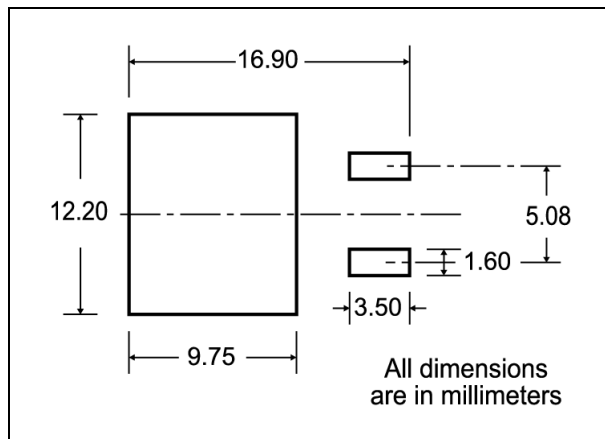
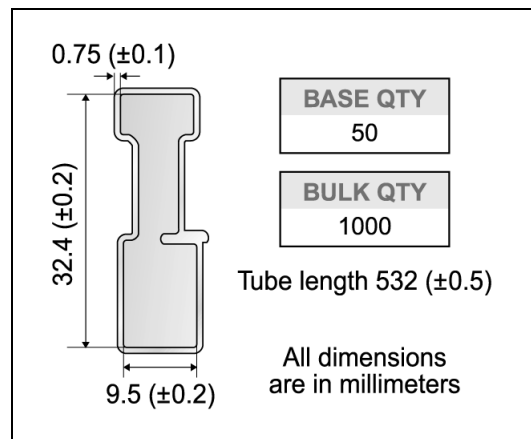
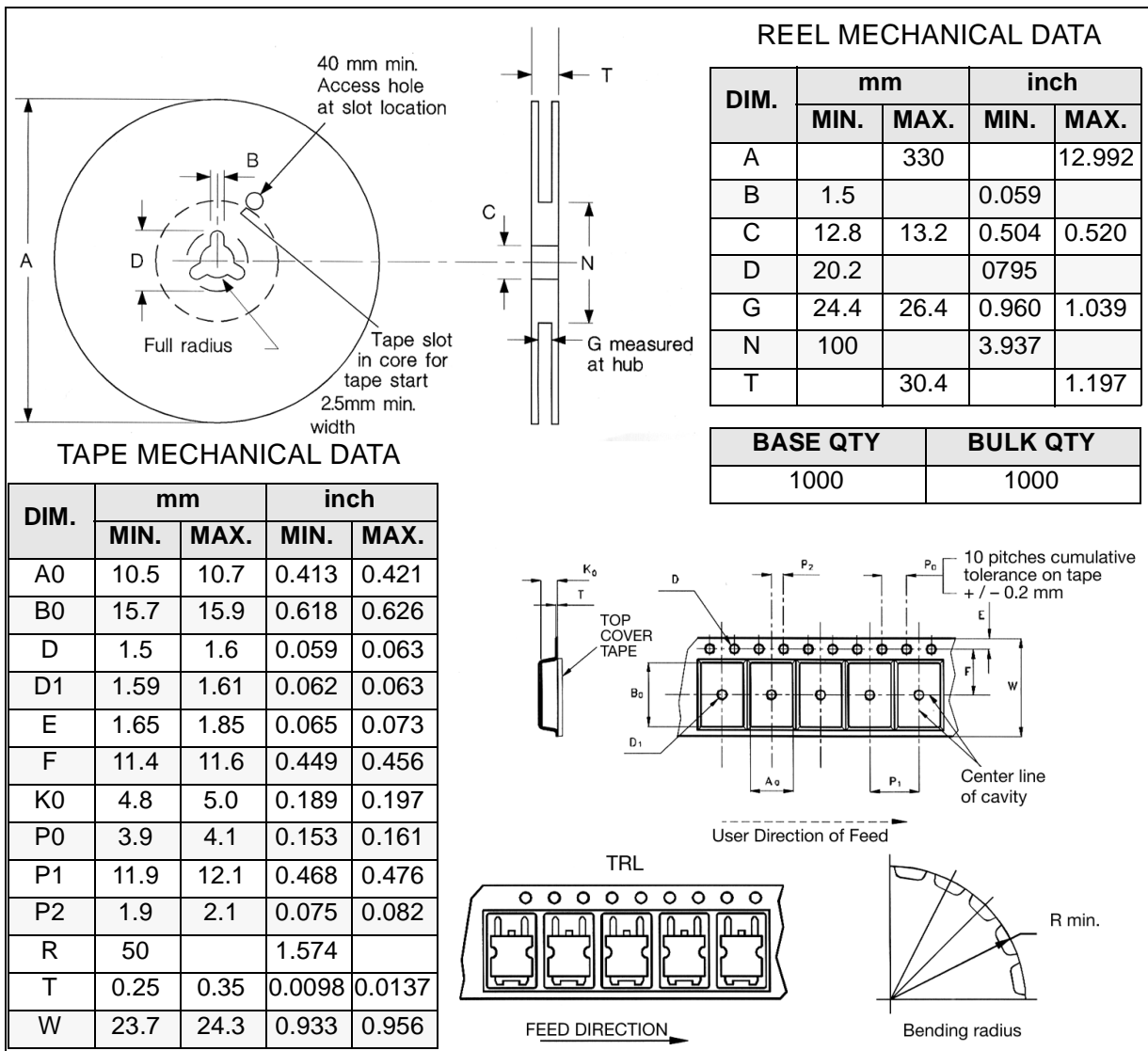
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



D²PAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>