



STP80NS04Z

N - CHANNEL CLAMPED 7.5mΩ - 80A - TO-220 FULLY PROTECTED MESH OVERLAY™ MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP80NS04Z	CLAMPED	<0.008 Ω	80 A

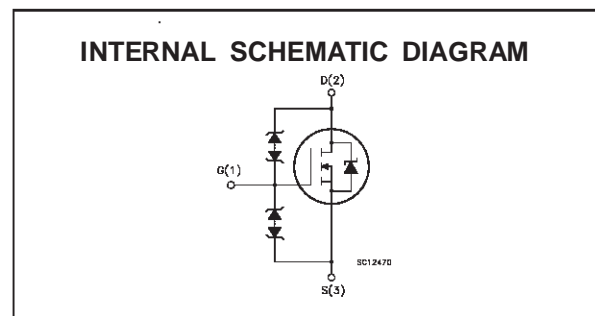
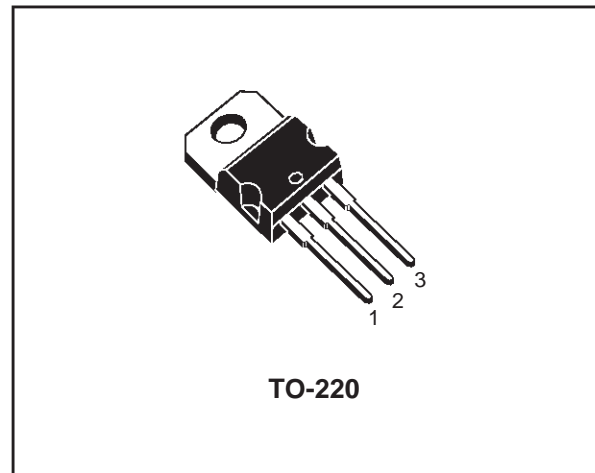
- TYPICAL R_{DS(on)} = 0.0075 Ω
- 100% AVALANCHE TESTED
- LOW CAPACITANCE AND GATE CHARGE
- 175 °C MAXIMUM JUNCTION TEMPERATURE

DESCRIPTION

This fully clamped Mosfet is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

APPLICATIONS

- ABS, SOLENOID DRIVERS
- MOTOR CONTROL
- DC-DC CONVERTERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	CLAMPED	V
V _{DG}	Drain- gate Voltage	CLAMPED	V
V _{GS}	Gate-source Voltage	CLAMPED	V
I _D	Drain Current (continuous) at T _c = 25 °C	80	A
I _D	Drain Current (continuous) at T _c = 100 °C	60	A
I _{DG}	Drain Gate Current (continuous)	± 50	mA
I _{GS}	Gate Source Current (continuous)	± 50	mA
I _{DM} (•)	Drain Current (pulsed)	320	A
P _{tot}	Total Dissipation at T _c = 25 °C	160	W
	Derating Factor	1.06	W/°C
V _{ESD} (G-S)	Gate-Source ESD (HBM - C= 100pF, R=1.5 kΩ)	2	kV
V _{ESD} (G-D)	Gate-Drain ESD (HBM - C= 100pF, R=1.5 kΩ)	4	kV
V _{ESD} (D-S)	Drain-Source ESD (HBM - C= 100pF, R=1.5 kΩ)	4	kV
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	-40 to 175	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 80 A, di/dt ≤ 300 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.94	$^{\circ}C/W$
$R_{thj-case}$	Thermal Resistance Junction-case	Typ	0.65	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}C/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.5	$^{\circ}C/W$
T_I	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	80	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}C$, $I_D = I_{AR}$, $V_{DD} = 30 V$)	500	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-Gate Breakdown Voltage	$I_D = 1 mA$ $V_{GS} = 0$ $-40 < T_j < 175^{\circ}C$	33			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = 16 V$ $T_j = 175^{\circ}C$			50	μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 10 V$ $T_j = 175^{\circ}C$ $V_{GS} = \pm 16 V$ $T_j = 175^{\circ}C$			50 150	μA μA
V_{GSS}	Gate-Source Breakdown Voltage	$I_G = 100 \mu A$	18			V

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_D = 1 mA$ $-40 < T_j < 150^{\circ}C$	1.7	3	4.2	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 40 A$ $V_{GS} = 16V$ $I_D = 40 A$		8 7.5	9 8	$m\Omega$ $m\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	80			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 40 A$	30	50		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		4000 1250 230	5400 1700 320	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Q_g	Total Gate Charge	$V_{DD} = 16\text{ V}$ $I_D = 80\text{ A}$ $V_{GS} = 10\text{ V}$		105	142	nC
Q_{gs}	Gate-Source Charge			24		nC
Q_{gd}	Gate-Drain Charge			41		nC

SWITCHING OFF

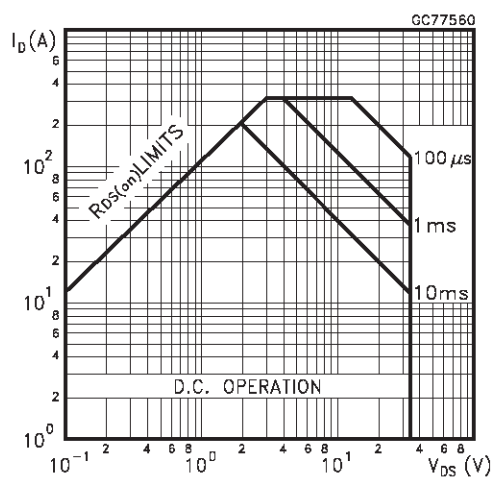
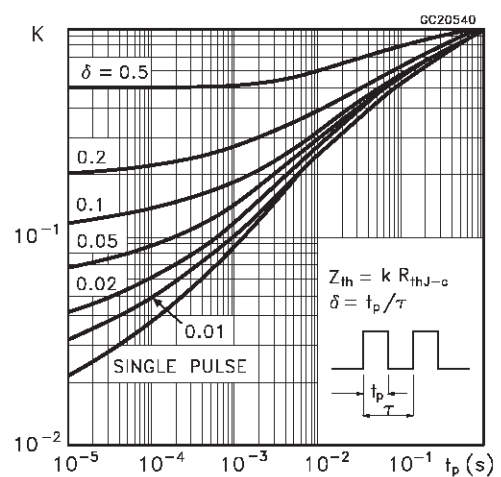
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(V_{off})}$	Off-voltage Rise Time	$V_{CLAMP} = 30\text{ V}$ $I_D = 80\text{ A}$		60	80	ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		140	190	ns
t_c	Cross-over Time	(see test circuit, figure 5)		220	300	ns

SOURCE DRAIN DIODE

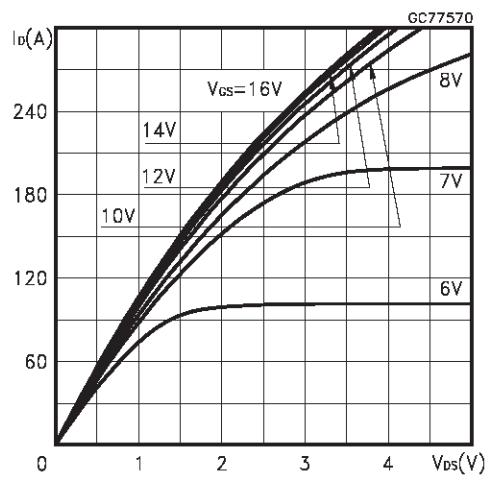
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				80	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				320	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 80\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 80\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_r = 25\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		75		ns
Q_{rr}	Reverse Recovery Charge			0.21		μC
I_{RRM}	Reverse Recovery Current			6		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

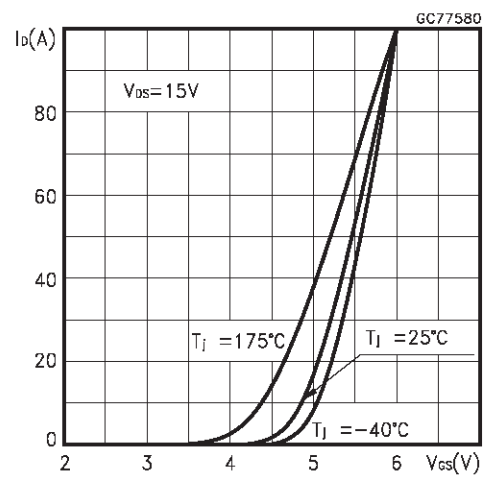
(•) Pulse width limited by safe operating area

Safe Operating Area**Thermal Impedance**

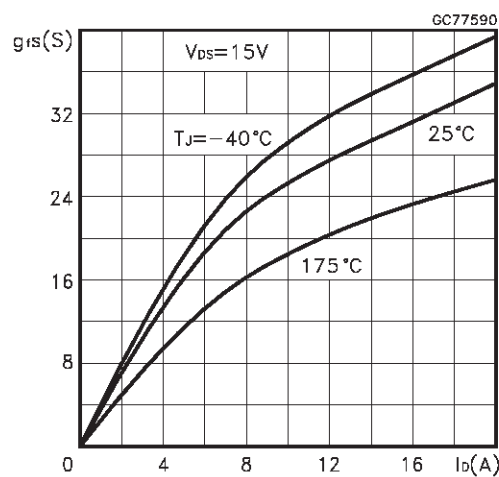
Output Characteristics



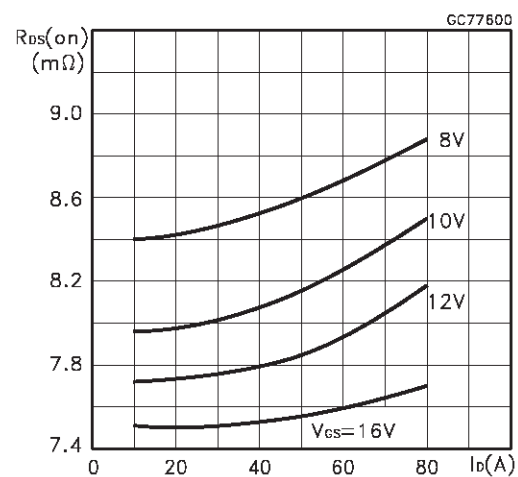
Transfer Characteristics



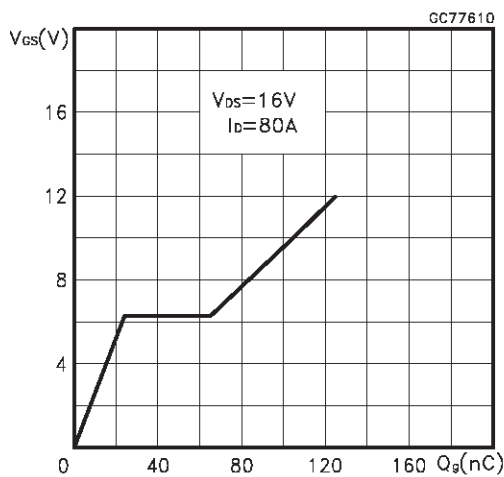
Transconductance



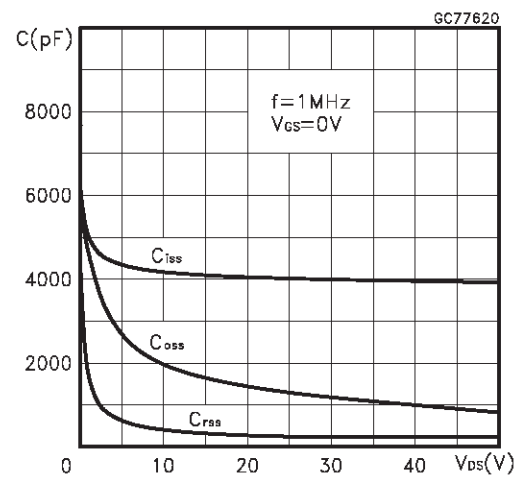
Static Drain-source On Resistance



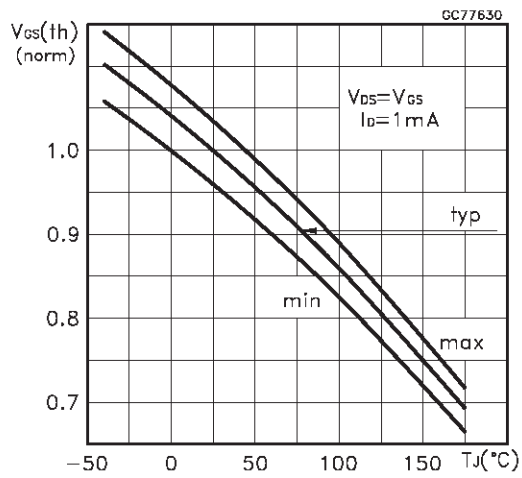
Gate Charge vs Gate-source Voltage



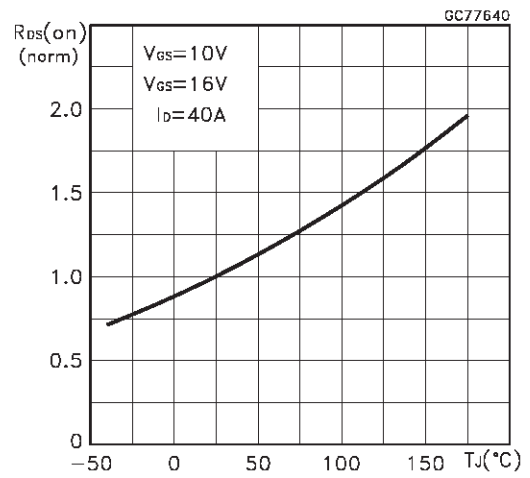
Capacitance Variations



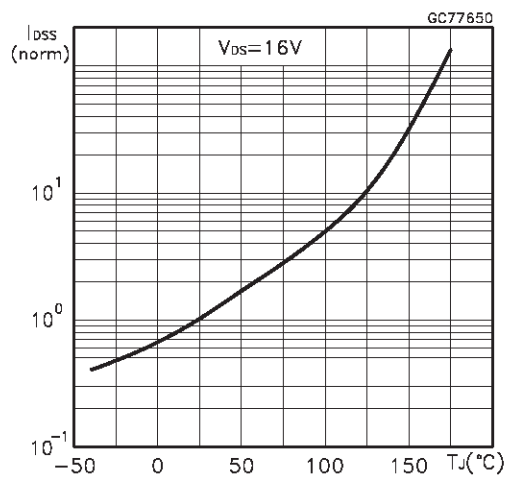
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Zero Gate Voltage Drain Current vs Temperature



Source-drain Diode Forward Characteristics

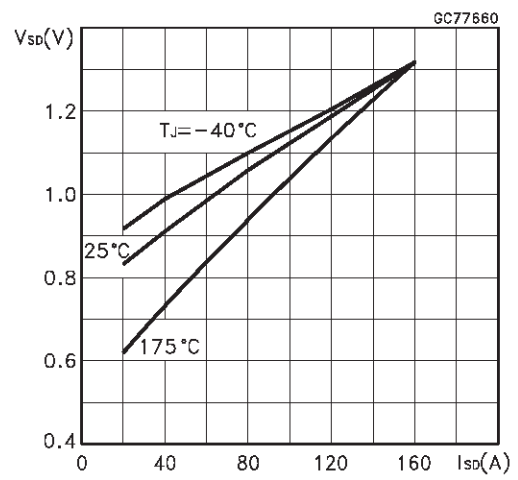


Fig. 1: Unclamped Inductive Load Test Circuit

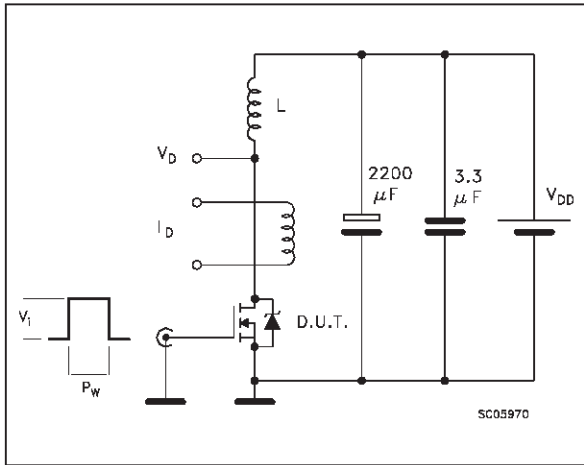


Fig. 2: Unclamped Inductive Waveform

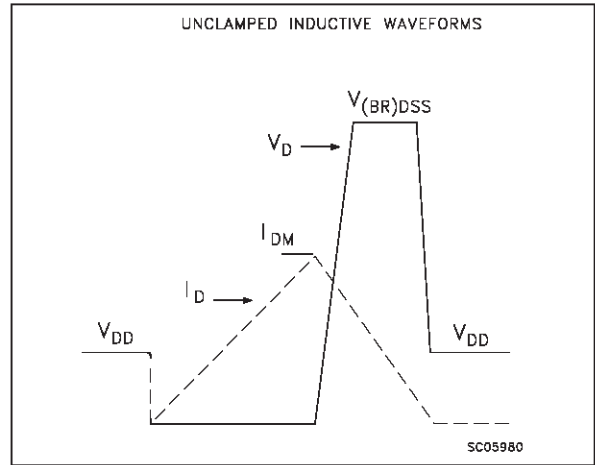


Fig. 3: Switching Times Test Circuits For Resistive Load

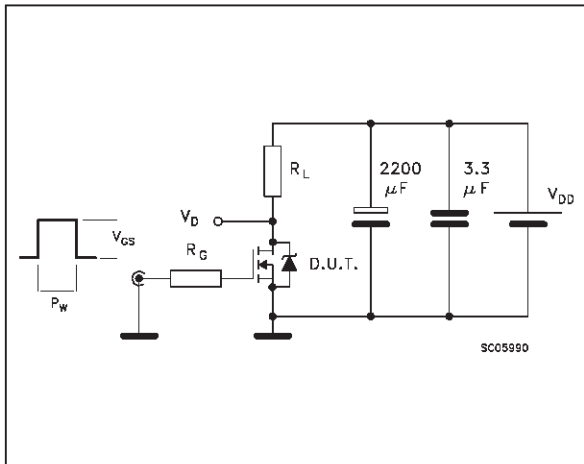


Fig. 4: Gate Charge test Circuit

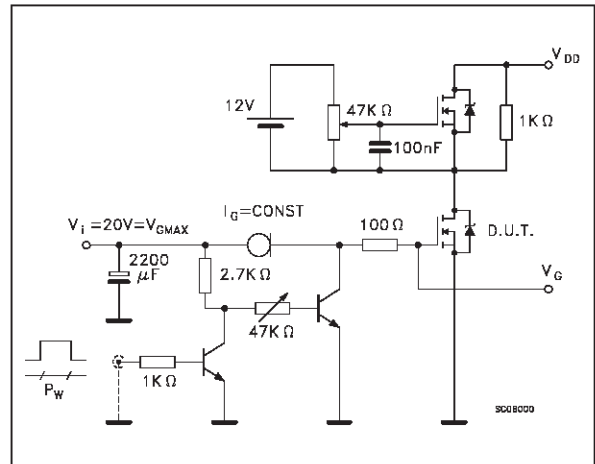
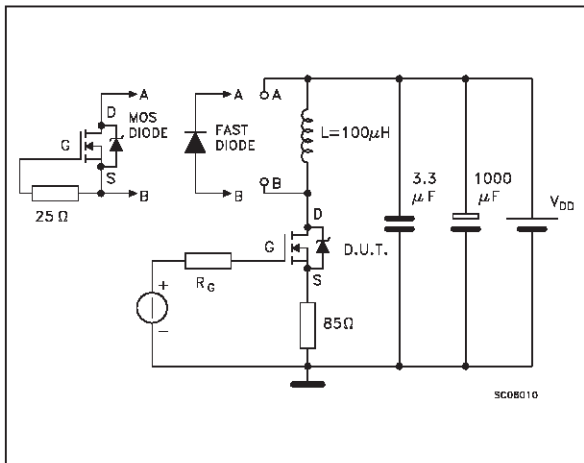
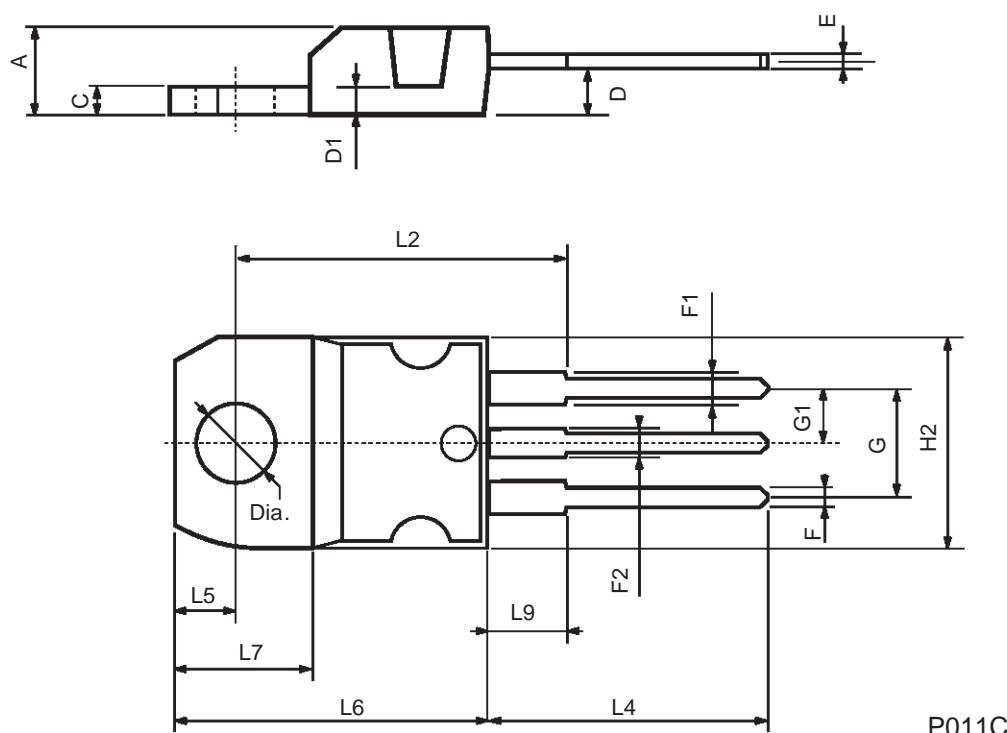


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.