



# STPAC02F2

## IPAD™

RF Detector for power amplifier control with internal temperature compensation

### Main product characteristics

- 0.8 to 2.5 GHz frequency range
- Detection diode voltage drop compensation
- Temperature compensation
- Fast response time
- Low Power consumption
- Chip Scale device
- Low parasitic impedance
- Lead free package

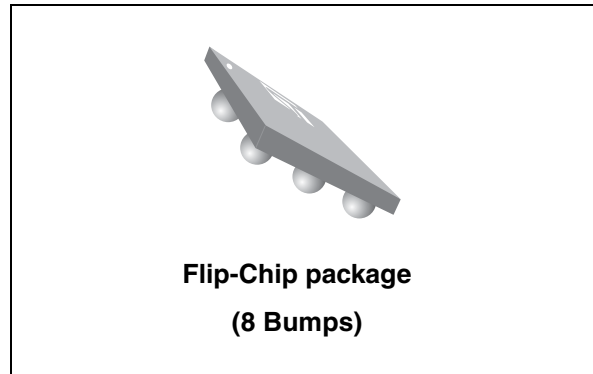
### Description

The STPAC02F2 is an integrated RF detector for power control chain. It has been developed to convert the RF signal coming from the external coupler into a DC signal usable by the mobile digital stage. It is based on the use of two similar diodes, one assuming the signal detection while the second one is used to compensate the ambient temperature effect. A biasing stage suppresses the detection diode drop voltage effect. The use of the IPAD technology allows the RF front-end designer to save PCB area and to drastically suppress the parasitic inductances of the package.

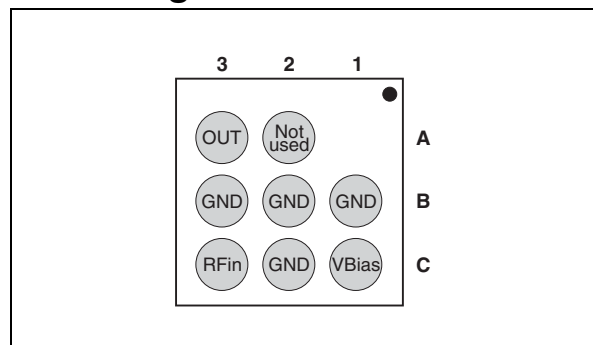
Target applications are cellular phones and PDA using GSM, DCS, PCS, AMPS, TDMA, CDMA and 800 MHz to 2100 MHz frequency ranges.

### Benefits

- The use of IPAD technology allows the RF front-end designer to save PCB area and to drastically suppress the parasitic inductances.



### Pin configuration



### Order code

Part number	Marking
STPAC02F2	RB

# 1 Characteristics

Figure 1. Functional diagram

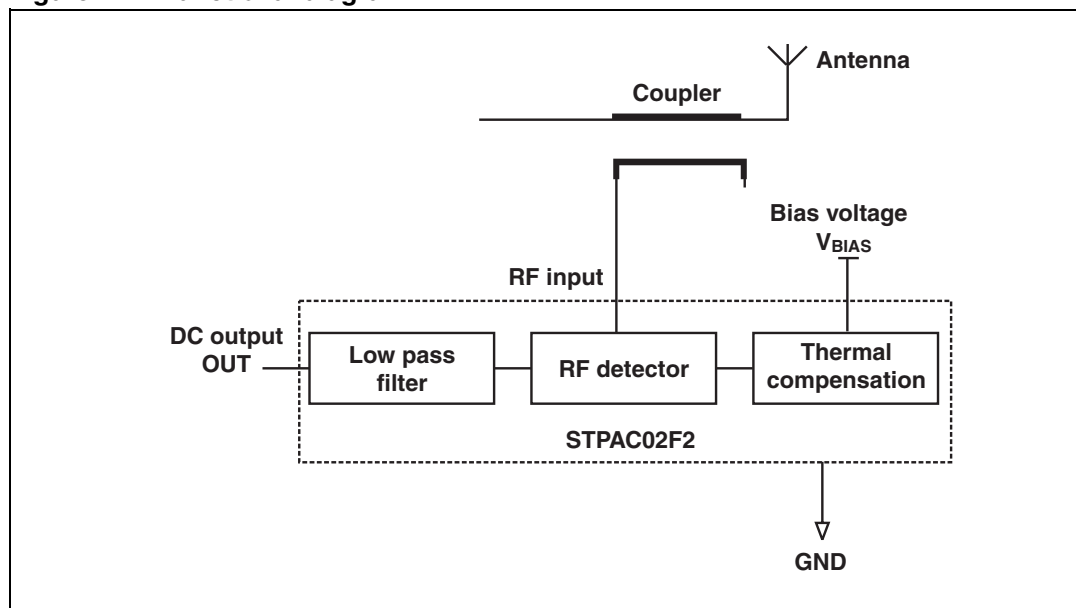


Table 1. Absolute ratings ( $T_{amb} = 25^{\circ}C$ )

Symbol	Parameter and test conditions	Value	Unit
$V_{BIAS}$	Bias voltage	5	V
$P_{RF}$	RF power at the RF input	20	dbm
$F_{OP}$	Operating frequency range	0.8 to 2.5	GHz
$V_{PP}$	ESD level as per MIL-STD 883E method 3015.7 notice 8 (HBM)	250	V
$T_{OP}$	Operating temperature range	- 30 to + 85	$^{\circ}C$
$T_{STG}$	Storage temperature range	- 55 to 150	$^{\circ}C$

## 1.1 Electrical characteristics ( $T_{amb} = 25^{\circ}C$ )

Table 2. Parameters related to bias voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BIAS}$	Operating bias voltage		2.3	2.8	3.3	V
$I_{BIAS}$	Bias current	$V_{BIAS} = 3.3 V$		1.1	1.6	mA

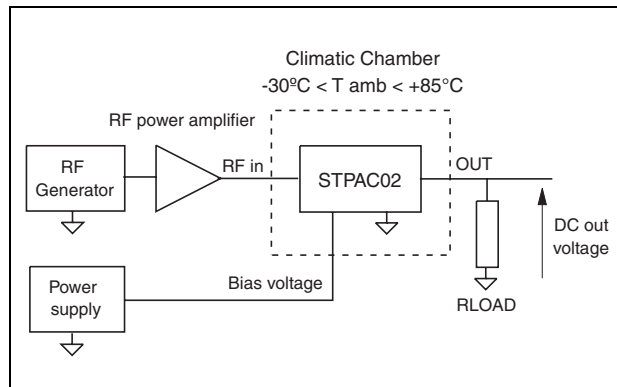
**Table 3. Parameters related to detection function** ( $V_{BIAS} = 2.8\text{ V}$ , DC output load = 200 k $\Omega$ )

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{DCout}$	DC output voltage (see <a href="#">Figure 2.</a> )	F = 1.75 GHz, $P_{RF} = 10\text{ dbm}$	0.63	0.69	0.75	V
		F = 1.75 GHz, $P_{RF} = -20\text{ dbm}$	0.20	0.22	0.24	
		F = 0.9 GHz, $P_{RF} = 10\text{ dbm}$	0.69	0.75	0.83	
		F = 0.9 GHz, $P_{RF} = -20\text{ dbm}$	0.20	0.22	0.24	
$\Delta V_{DCout}$	DC output voltage variation (see <a href="#">Figure 2.</a> )	$2.3\text{ V} < V_{BIAS} < 3.3\text{ V}$ , F = 1.85 GHz, $P_{RF} = 10\text{ dbm}$		100		mV

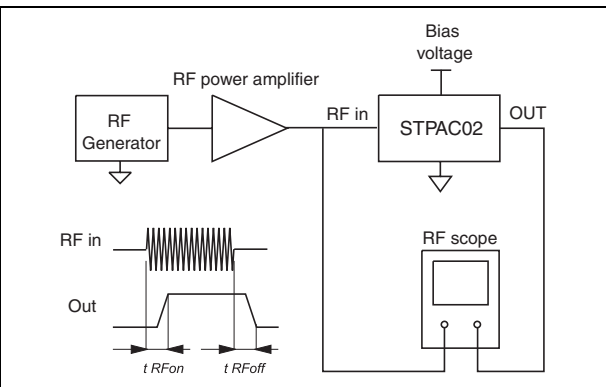
**Table 4. Parameters related to response time** ( $V_{BIAS} = 2.8\text{ V}$ , DC output load = 200 k $\Omega$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{VBIAS}$	Delay at $V_{BIAS}$ ON (see <a href="#">Figure 4.</a> )	$V_{BIAS}$ from 0 to 3 V		1		V
$t_{RFon}$	Delay at RF ON (see <a href="#">Figure 3.</a> )	$P_{RF}$ from 0 to 20 dbm		0.2		
$t_{RFOff}$	Delay at RF OFF (see <a href="#">Figure 3.</a> )	$P_{RF}$ from 20 to 0 dbm		0.2		

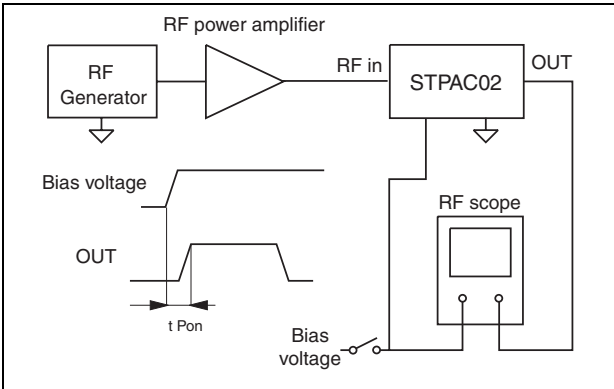
**Figure 2.  $V_{DC}$  output measurement circuit and temperature compensation measurement**



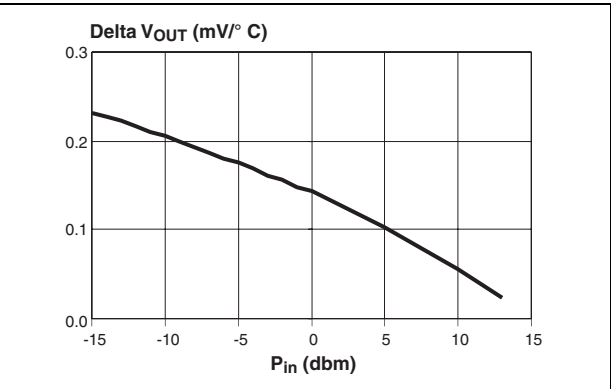
**Figure 3. RF Power ON/OFF response time set-up**



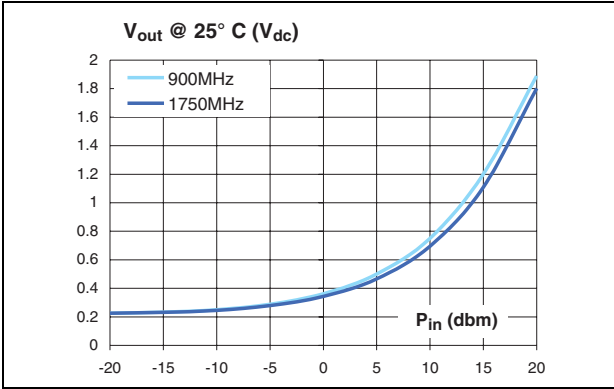
**Figure 4. Power supply turn ON response time**



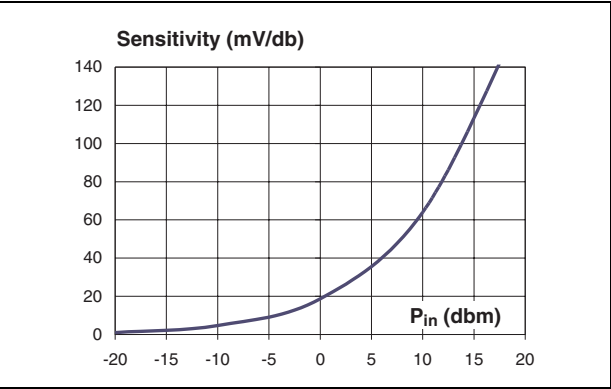
**Figure 5. Temperature sensitivity versus RF Power in ( $V_{BIAS} = 2.8\text{ V}$ , Freq. = 900 MHz)**



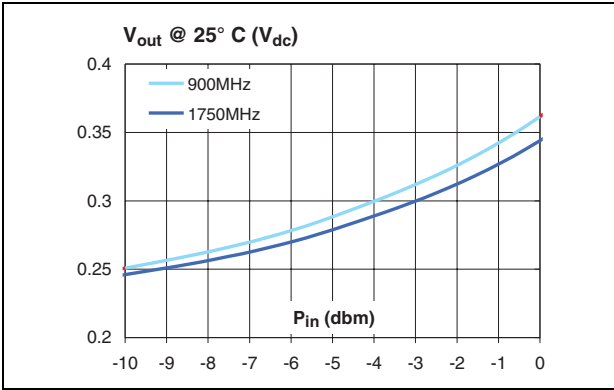
**Figure 6. STPAC02 Output voltage at wide RF power range**



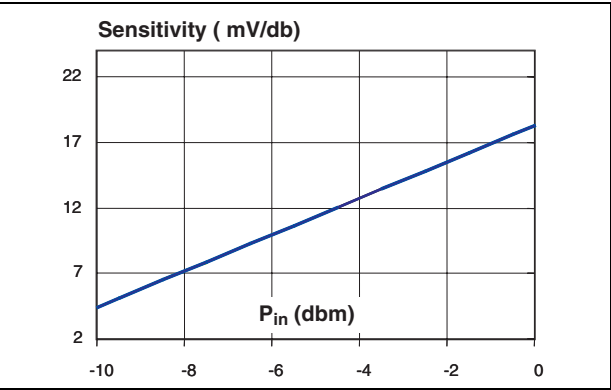
**Figure 7. Power detector sensitivity at wide RF power range**



**Figure 8. STPAC02 Output voltage at low RF power**



**Figure 9. Power detector sensitivity at low RF power**



## 2 Packaging information

Figure 10. Flip-Chip dimensions

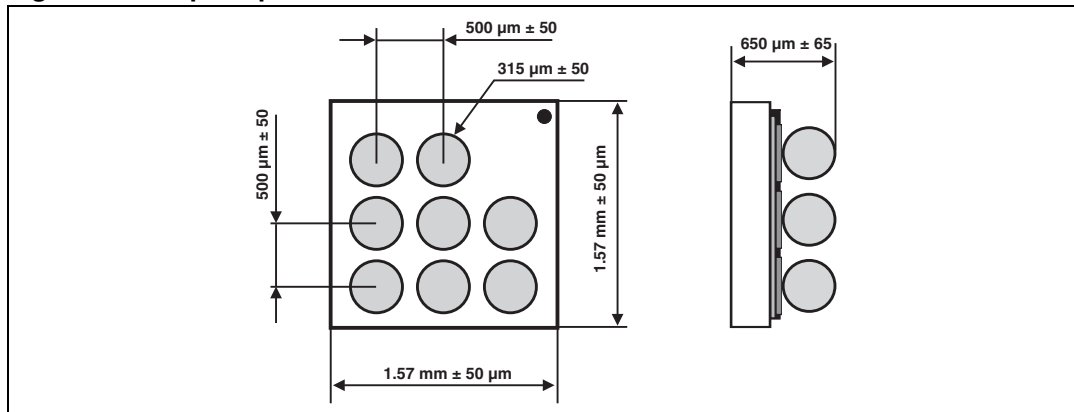


Figure 11. Foot print recommendations      Figure 12. Marking

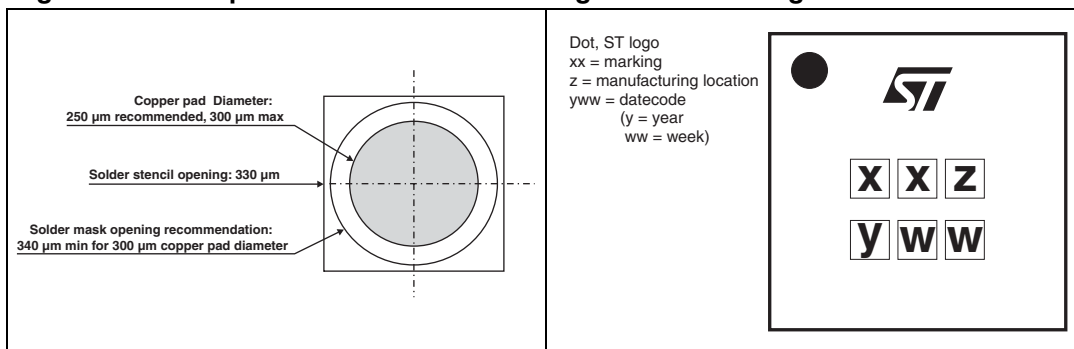
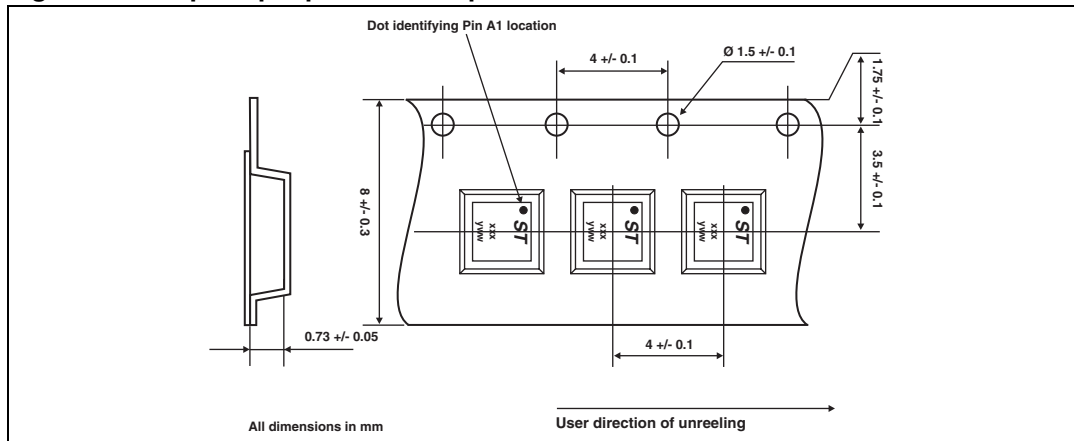


Figure 13. Flip-Chip tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 3 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
STPAC02F1	RB	Flip-Chip	3.3 mg	5000	Tape and reel

*Note:* More packing informations are available in the application notes:  
AN1235: "Flip-Chip: Package description and recommendations for use"  
AN1751: "EMI Filters: Recommendations and measurements"

### 4 Revision history

Date	Revision	Changes
16-May-2006	1	Initial release.

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