



STS1DNC45

DUAL N-CHANNEL 450V - 4.1Ω - 0.4A SO-8

SuperMESH™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS1DNC45	450 V	< 4.5 Ω	0.4 A

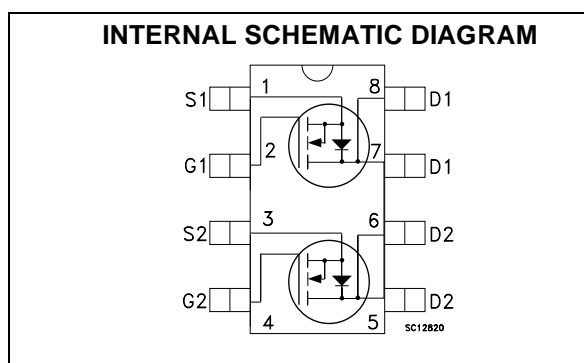
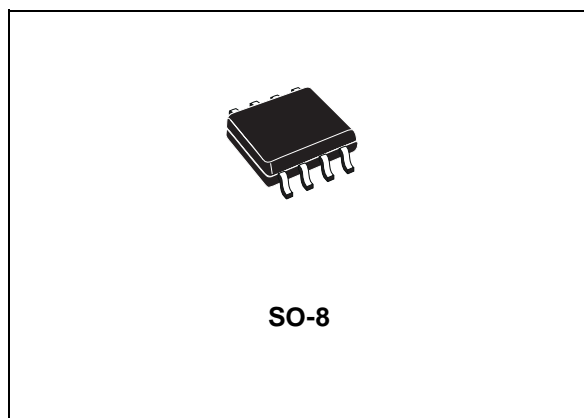
- TYPICAL R_{DS(on)} = 4.1Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- GATE CHARGE MINIMIZED

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- SWITCH MODE LOW POWER SUPPLIES (SMPS)
- DC-DC CONVERTERS
- LOW POWER, LOW COST CFL (COMPACT FLUORESCENT LAMPS)
- LOW POWER BATTERY CHARGERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	450	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	450	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C Drain Current (continuous) at T _C = 100°C	0.40 0.25	A A
I _{DM} (●)	Drain Current (pulsed)	1.6	A
P _{TOT}	Total Dissipation at T _C = 25°C Dual Operation Total Dissipation at T _C = 25°C Single Operation	1.6 2	W W
dv/dt(1)	Peak Diode Recovery voltage slope	3	V/ns

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 0.4 A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}.

STS1DNC45

THERMAL DATA

Rthj-amb(#)	Thermal Resistance Junction-ambient Max Single Operation Thermal Resistance Junction-ambient Max Dual Operation	62.5 78	°C/W °C/W
T _j	Max. Operating Junction Temperature	150	°C
T _{stg}	Storage Temperature	−65 to 150	°C

(#) When Mounted on FR4 board (Steady State)

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	0.4	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	30	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	450			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	2.3	3	3.7	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 0.5 A		4.1	4.5	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 25 V, I _D = 0.5 A		1.1		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		160		pF
C _{oss}	Output Capacitance			27.5		pF
C _{rss}	Reverse Transfer Capacitance			4.7		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 225\text{ V}$, $I_D = 0.5\text{ A}$		6.7		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		4		ns
Q_g	Total Gate Charge	$V_{DD} = 360\text{ V}$, $I_D = 1.5\text{ A}$,		7	10	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{ V}$		1.3		nC
Q_{gd}	Gate-Drain Charge			3.2		nC

SWITCHING OFF

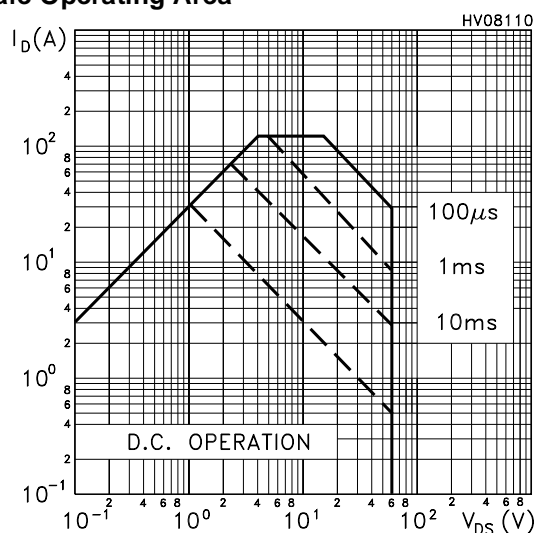
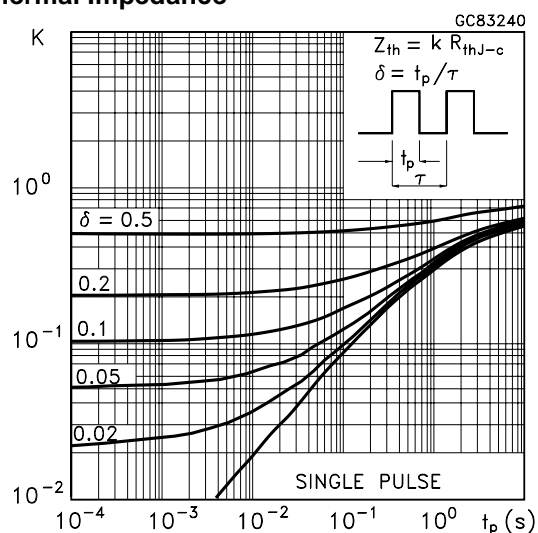
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(off)}$	Off-voltage Rise Time	$V_{DD} = 360\text{ V}$, $I_D = 1.5\text{ A}$		8.5		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$		12		ns
t_c	Cross-over Time	(see test circuit, Figure 5)		18		ns

SOURCE DRAIN DIODE

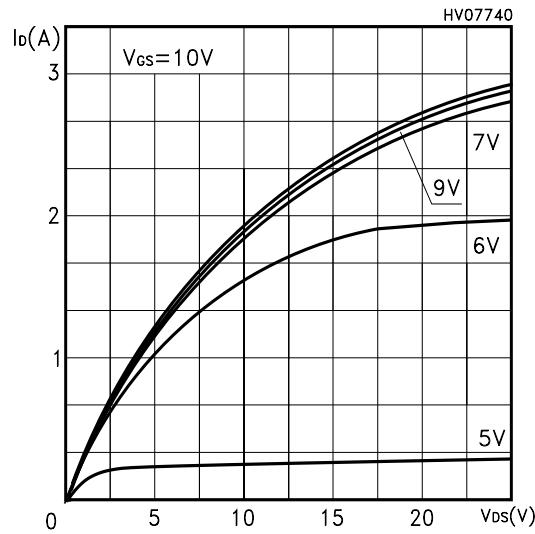
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				0.4	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				1.6	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 0.4\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 0.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,		225		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 100\text{ V}$, $T_j = 150^\circ\text{C}$		530		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		4.7		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

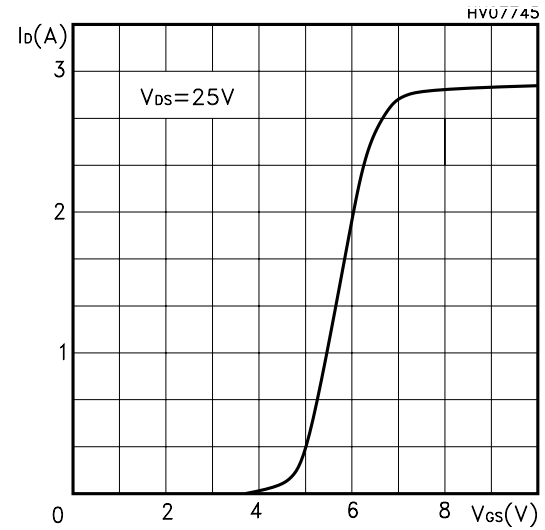
2. Pulse width limited by safe operating area.

Safe Operating Area**Thermal Impedance**

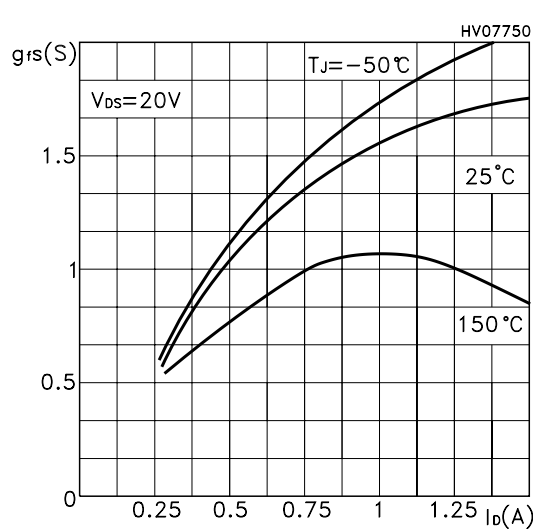
Output Characteristics



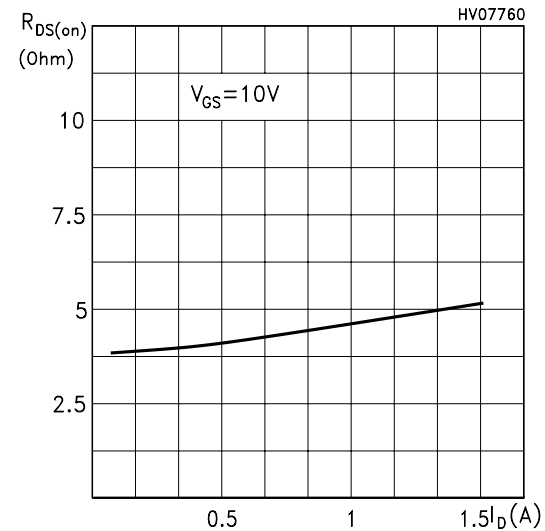
Transfer Characteristics



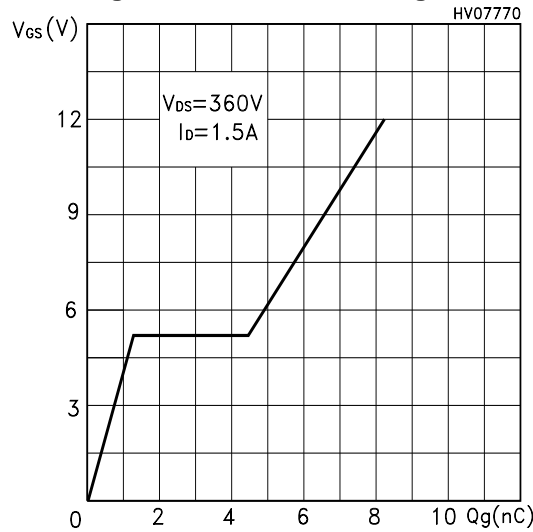
Transconductance



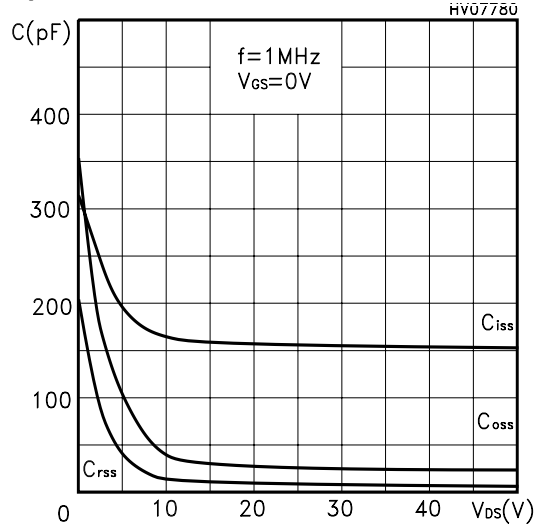
Static Drain-source On Resistance



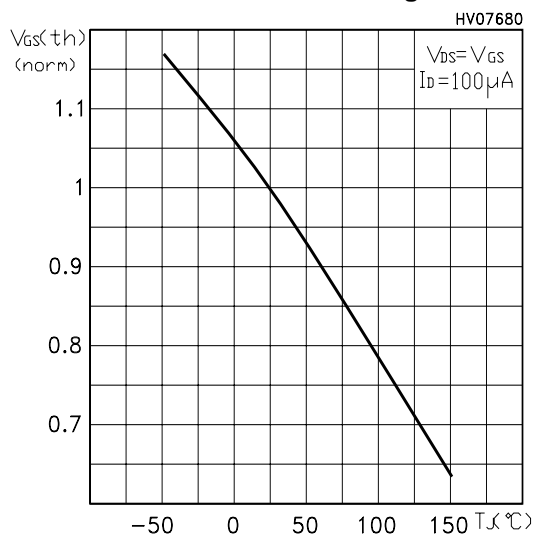
Gate Charge vs Gate-source Voltage



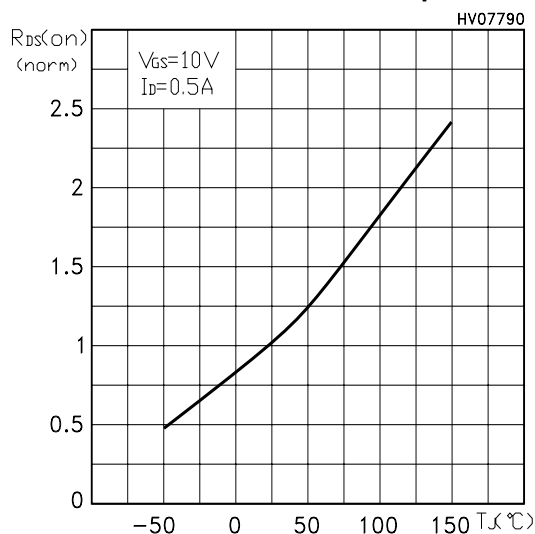
Capacitance Variations



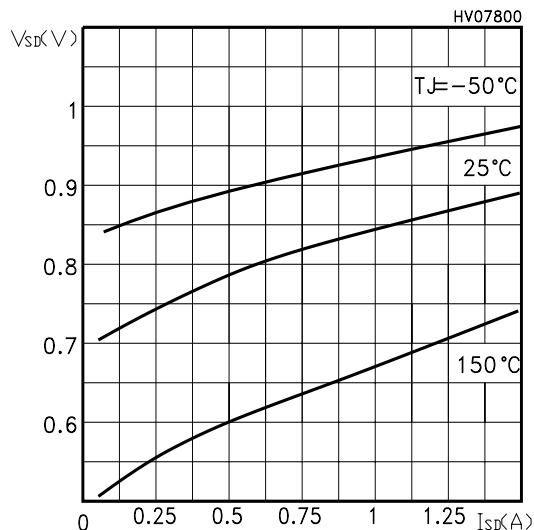
Normalized Gate Threshold Voltage vs Temp.



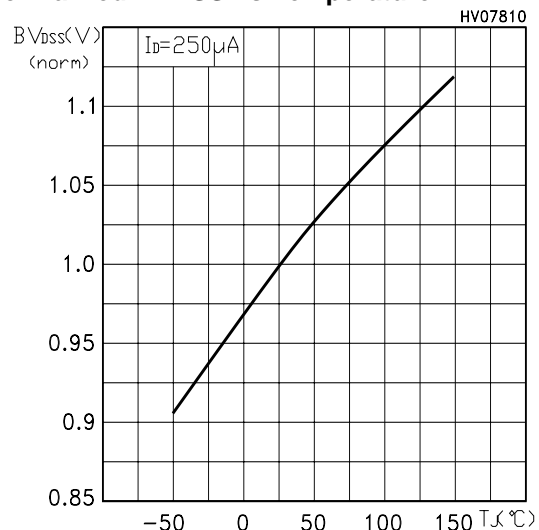
Normalized On Resistance vs Temperature



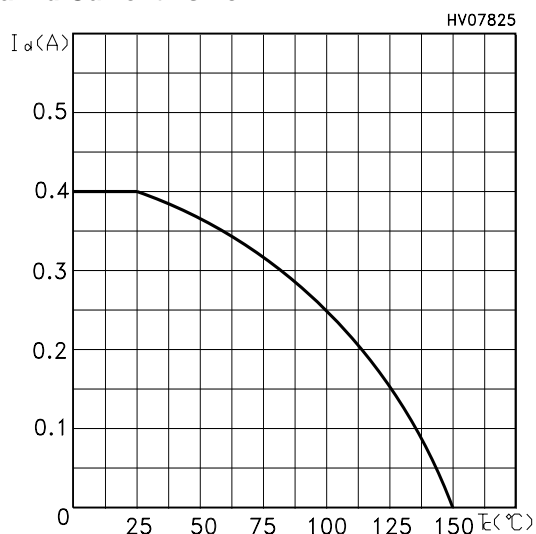
Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Max Id Current vs Tc



Maximum Avalanche Energy vs Temperature

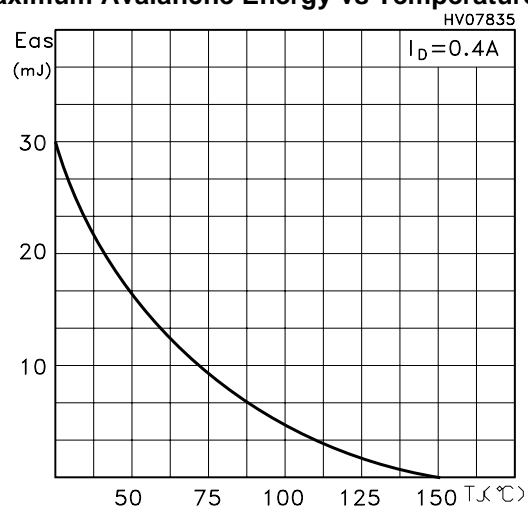


Fig. 1: Unclamped Inductive Load Test Circuit

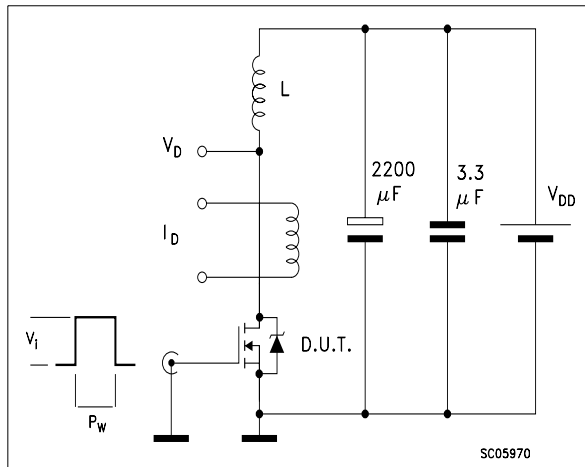


Fig. 2: Unclamped Inductive Waveform

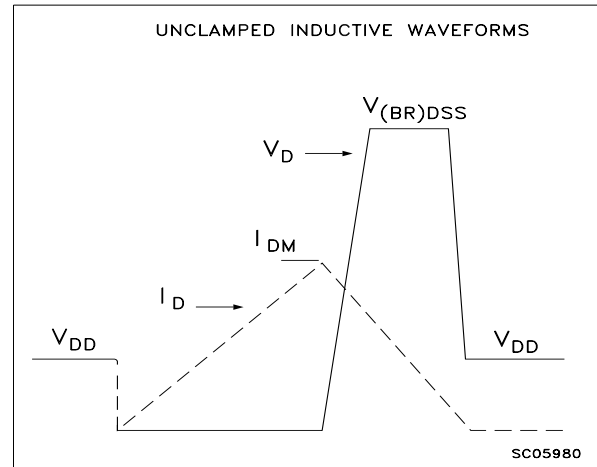


Fig. 3: Switching Times Test Circuit For Resistive Load

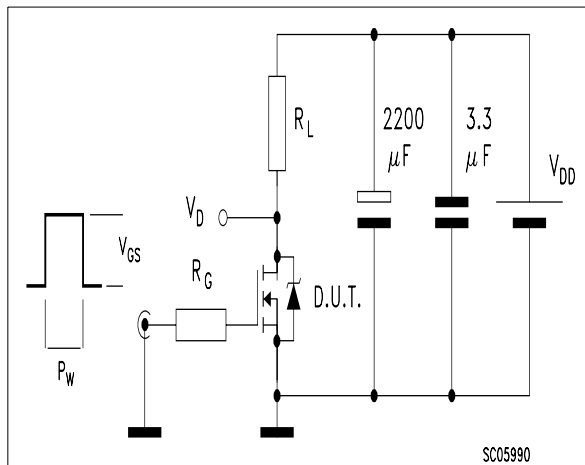


Fig. 4: Gate Charge test Circuit

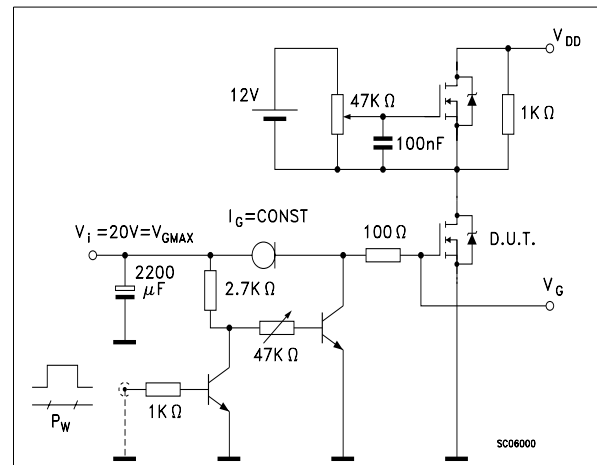
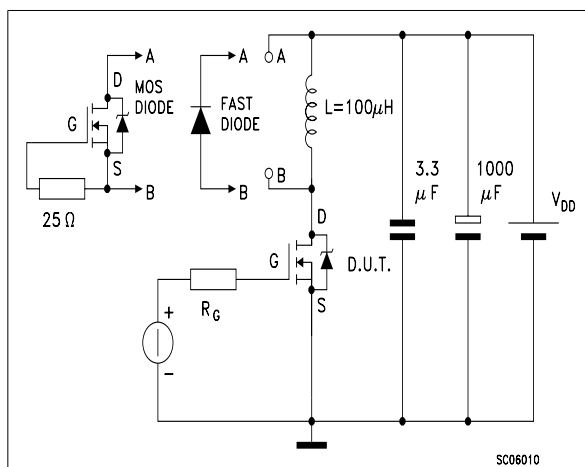
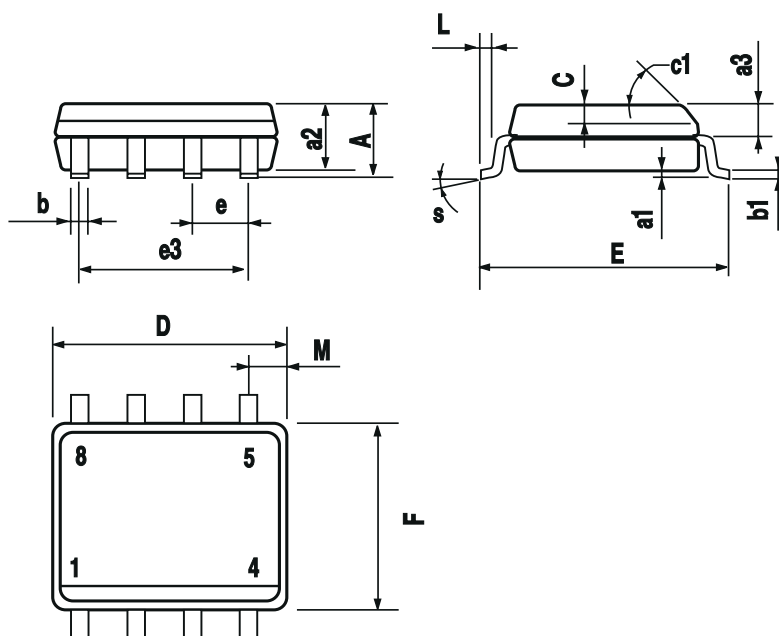


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>