



STS3DPF30L

DUAL P - CHANNEL 30V - 0.145Ω - 3A SO-8 STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS3DPF30L	30 V	< 0.16 Ω	3 A

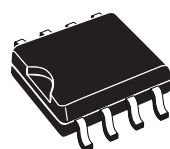
- TYPICAL R_{DS(on)} = 0.145 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

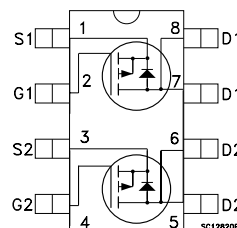
APPLICATIONS

- BATTERY MANAGMENT IN NOMADIC EQUIPMENT
- POWER MANAGMENT IN CELLULAR PHONES
- DC-DC CONVERTER



SO-8

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C Single Operation	3	A
	Drain Current (continuous) at T _c = 100 °C Single Operation	1.9	A
I _{DM} (•)	Drain Current (pulsed)	12	A
P _{tot}	Total Dissipation at T _c = 25 °C Dual Operation	2	W
	Total Dissipation at T _c = 25 °C Single Operation	1.6	W

(•) Pulse width limited by safe operating area

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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THERMAL DATA

$R_{thj-amb}$	*Thermal Resistance Junction-ambient	Single Operation	78	$^{\circ}\text{C/W}$
T_j	Maximum Operating Junction Temperature	Dual Operation	62.5	$^{\circ}\text{C/W}$
T_{stg}	Storage Temperature		150	$^{\circ}\text{C}$
			-55 to 150	$^{\circ}\text{C}$

(*) Mounted on FR-4 board ($t \leq 10\text{sec}$)

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\ \text{V}$ $I_D = 1.5\ \text{A}$ $V_{GS} = 4.5\ \text{V}$ $I_D = 1.5\ \text{A}$		0.145 0.18	0.16 0.19	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\ \text{V}$	3			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 3\ \text{A}$		3		S
C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$ $f = 1\ \text{MHz}$ $V_{GS} = 0\ \text{V}$		510		pF
C_{oss}	Output Capacitance			170		pF
C_{rss}	Reverse Transfer Capacitance			55		pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 1.5\text{ A}$		14.5		ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		37		ns
Q_g	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 3\text{ A}$ $V_{GS} = 4.5\text{ V}$		5.5		nC
Q_{gs}	Gate-Source Charge			1.7		nC
Q_{gd}	Gate-Drain Charge			1.8		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 1.5\text{ A}$		88		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		23		ns

SOURCE DRAIN DIODE

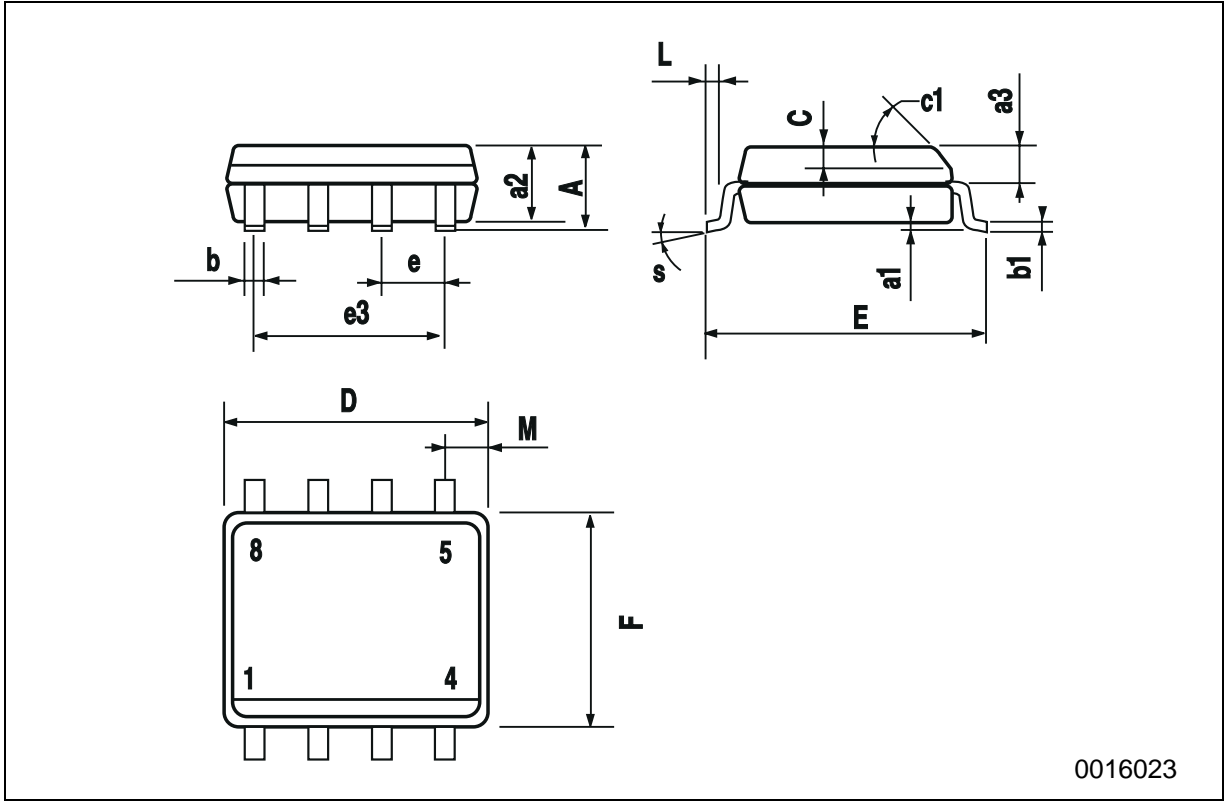
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				12	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 3\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 3\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		T.B.D		ns
Q_{rr}	Reverse Recovery Charge					μC
I_{RRM}	Reverse Recovery Current					A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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