



STS4DNF30L

DUAL N-CHANNEL 30V - 0.039Ω - 4A SO-8

STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS4DNF30L	30 V	< 0.050 Ω	4 A

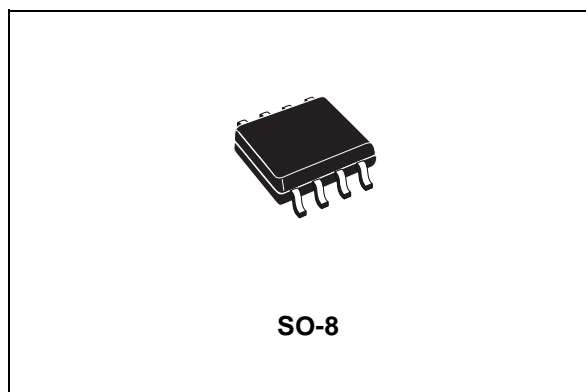
- TYPICAL R_{DS(on)} = 0.039 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

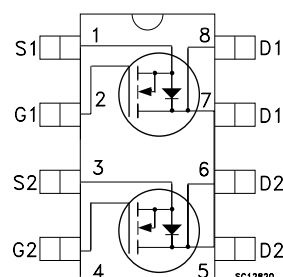
This Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- BATTERY MANAGMENT IN NOMADIC EQUIPMENT
- POWER MANAGMENT IN CELLULAR PHONES
- DC MOTOR DRIVE



INTERNAL SCHEMATIC DIAGRAM



MOSFET ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 16	V
I _D	Drain Current (continuous) at T _C = 25°C	4	A
I _D	Drain Current (continuous) at T _C = 100°C	2.5	A
I _{DM} (●)	Drain Current (pulsed)	16	A
P _{TOT}	Total Dissipation at T _C = 25°C Dual Operation	2	W

(●) Pulse width limited by safe operating area.

STS4DNF30L

THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient Max	62.5	°C/W
T _{stg}	Storage Temperature Range	-55 to 150	°C
T _J	Junction Temperature	150	°C
(*) Mounted on FR-4 board (t ≤ 10sec)			

MOSFET ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 2 A V _{GS} = 4.5V, I _D = 2 A		0.039 0.046	0.050 0.060	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 2 A	1	3		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		330		pF
C _{oss}	Output Capacitance			90		pF
C _{rss}	Reverse Transfer Capacitance			40		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\Omega$		11		ns
t_r	Rise Time	$V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		100		ns
Q_g	Total Gate Charge	$V_{DD} = 24\text{ V}$, $I_D = 4\text{ A}$, $V_{GS} = 10\text{ V}$		6.5	9	nC
Q_{gs}	Gate-Source Charge			3.6		nC
Q_{gd}	Gate-Drain Charge			2		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$		25		ns
t_f	Fall Time	(see test circuit, Figure 3)		22		ns
$t_{r(Voff)}$	Off-Voltage Rise Time	$V_{DD} = 24\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$		22		ns
t_f	Fall Time	(see test circuit, Figure 5)		55		ns
t_c	Cross-over Time			75		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				4	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				16	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 4\text{ A}$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$, $T_j = 150^\circ\text{C}$		30		ns
Q_{rr}	Reverse Recovery Charge	(see test circuit, Figure 5)		18		nC
I_{RRM}	Reverse Recovery Current			1.2		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

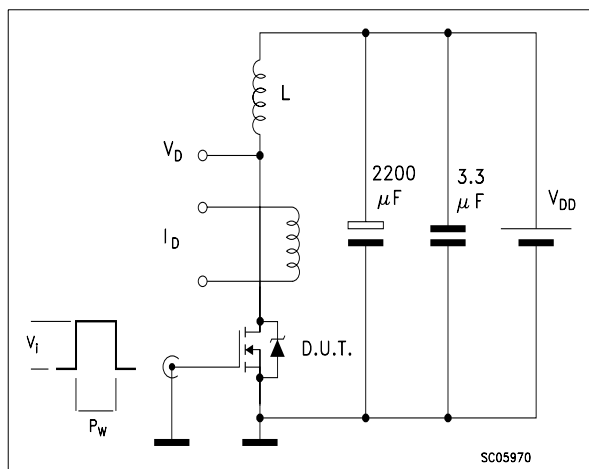


Fig. 2: Unclamped Inductive Waveform

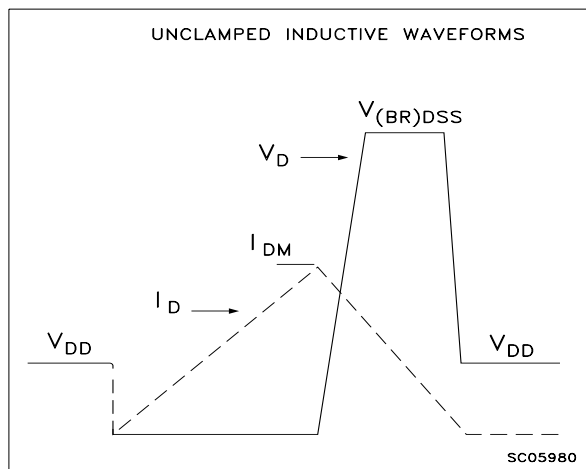


Fig. 3: Switching Times Test Circuits For Resistive Load

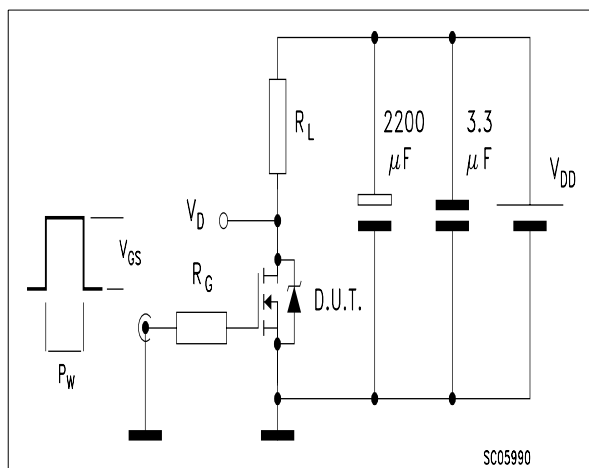


Fig. 4: Gate Charge test Circuit

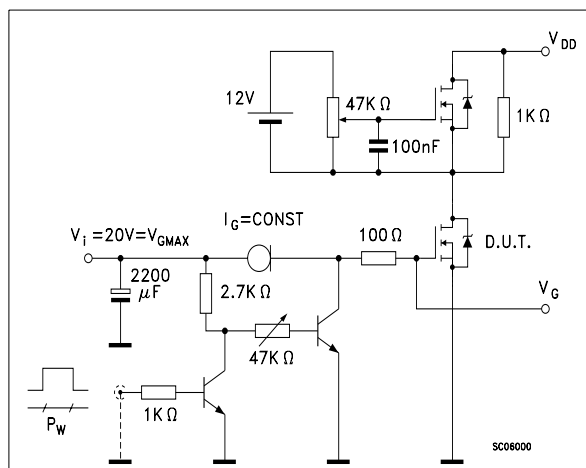
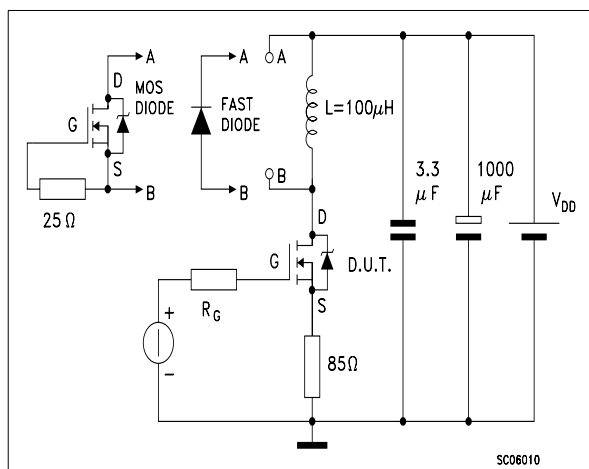
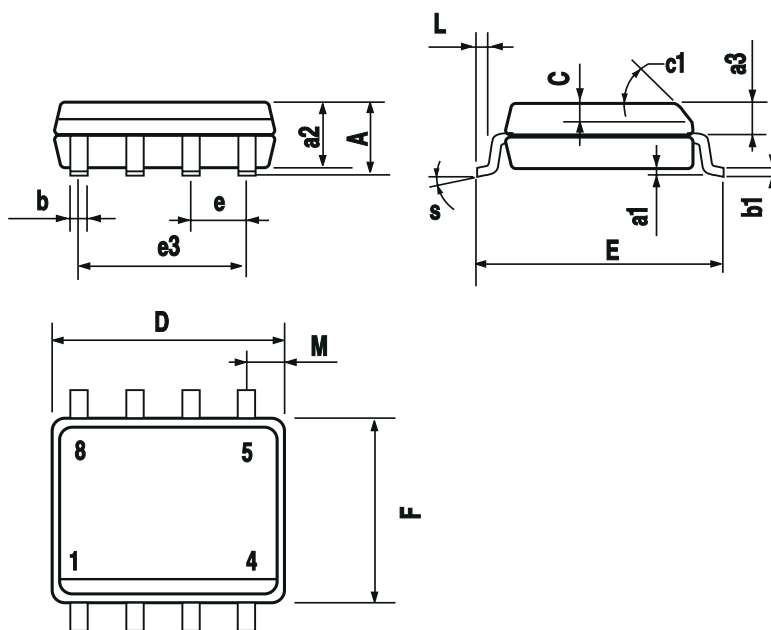


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>