



# STS9NF30L

## N-CHANNEL 30V - 0.015 $\Omega$ - 9A SO-8 LOW GATE CHARGE STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS9NF30L	30 V	< 0.020 $\Omega$	9 A

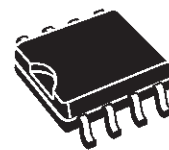
- TYPICAL R<sub>DS(on)</sub> = 0.018  $\Omega$  @ 4.5V
- TYPICAL Q<sub>g</sub> = 9 nC @ 4.5V
- OPTIMAL R<sub>DS(on)</sub> x Q<sub>g</sub> TRADE-OFF
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

### DESCRIPTION

This application specific Power Mosfet is the third generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

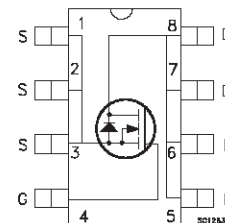
### APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCs



SO-8

### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	30	V
V <sub>GS</sub>	Gate-source Voltage	$\pm 20$	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	9	A
	Drain Current (continuous) at T <sub>c</sub> = 100 °C	5.6	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	36	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	2.5	W

(•) Pulse width limited by safe operating area

## STS9NF30L

### THERMAL DATA

$R_{thj-amb}$	(*)Thermal Resistance Junction-ambient	50	$^{\circ}\text{C}/\text{W}$
$T_j$	Maximum Operating Junction Temperature	150	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature	-65 to 150	$^{\circ}\text{C}$

(\*) Mounted on FR-4 board ( $t \leq 10\text{sec}$ )

### ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA

#### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\ \text{V}$ $I_D = 4\ \text{A}$ $V_{GS} = 4.5\ \text{V}$ $I_D = 4\ \text{A}$		0.015 0.018	0.020 0.024	$\Omega$ $\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\ \text{V}$	9			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 5.5\ \text{A}$		10		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\ \text{V}$ $f = 1\ \text{MHz}$ $V_{GS} = 0\ \text{V}$		750 270 60		pF pF pF

**ELECTRICAL CHARACTERISTICS** (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 4.5\text{ A}$		15		ns
$t_r$	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig.3)		78		ns
$Q_g$	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 9\text{ A}$ $V_{GS} = 4.5\text{ V}$		9	12	nC
$Q_{gs}$	Gate-Source Charge			3		nC
$Q_{gd}$	Gate-Drain Charge			5		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 4.5\text{ A}$		38		ns
$t_f$	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig.3)		23		ns

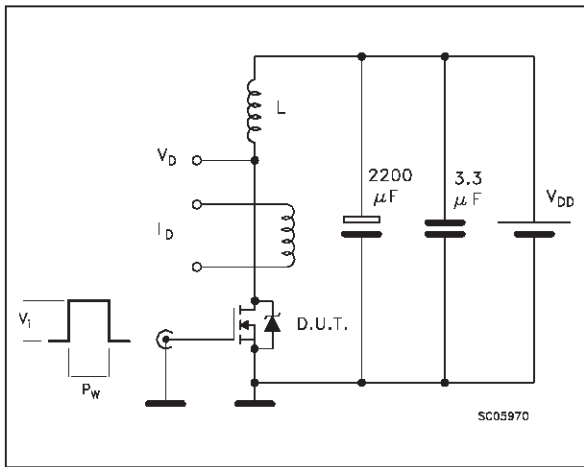
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				9	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				36	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 9\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 9\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_r = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig.5)		50		ns
$Q_{rr}$	Reverse Recovery Charge			80		nC
$I_{RRM}$	Reverse Recovery Current			2		A

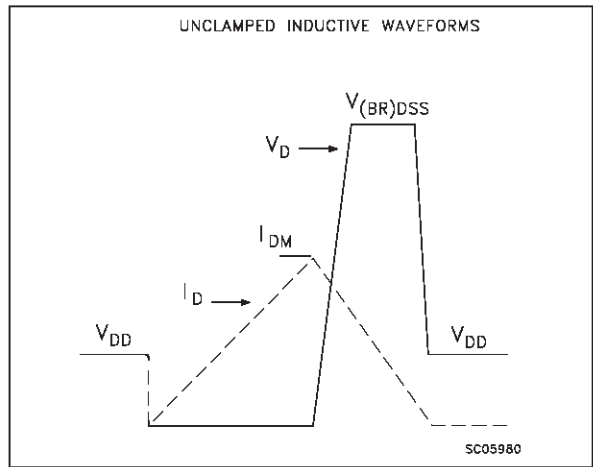
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

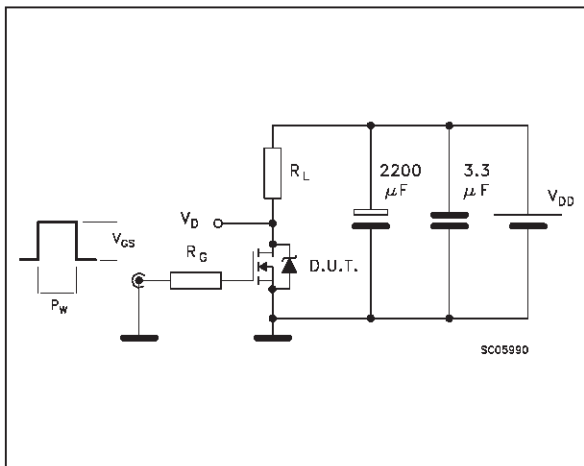
**Fig. 1: Unclamped Inductive Load Test Circuit**



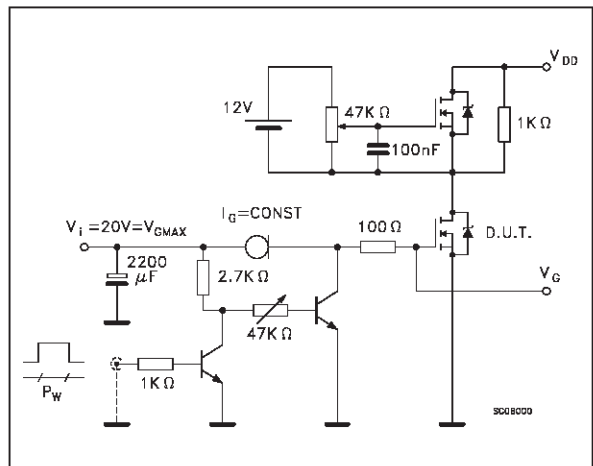
**Fig. 2: Unclamped Inductive Waveform**



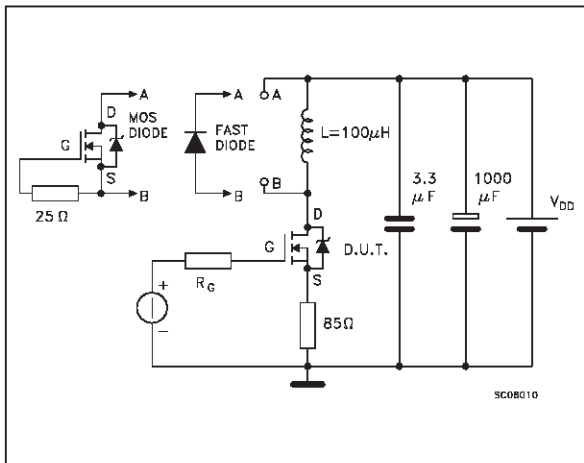
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

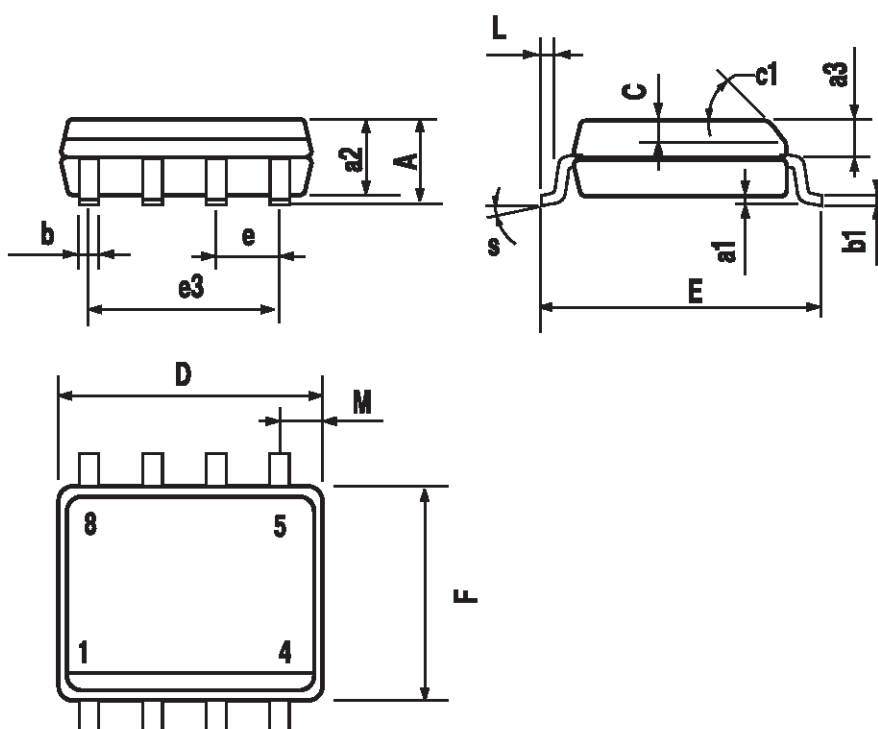


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



## SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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