



STU11NB60

N-CHANNEL 600V - 0.5Ω - 11A Max220

PowerMesh™II MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STU11NB60	600V	< 0.6Ω	11 A

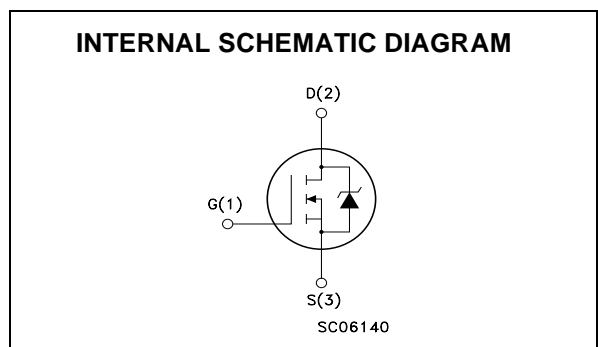
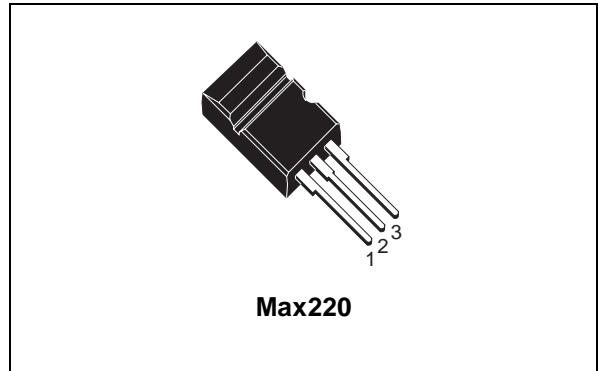
- TYPICAL R_{DS(on)} = 0.5Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's propriety edge termination structure, gives the lowest R_{DS(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600	V
V _{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	11	A
I _D	Drain Current (continuous) at T _C = 100°C	7	A
I _{DM} (●)	Drain Current (pulsed)	44	A
P _{TOT}	Total Dissipation at T _C = 25°C	160	W
	Derating Factor	1.28	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(1) I_{SD} ≤ 11A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.78	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	11	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	500	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)**OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 µA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 5.5A		0.5	0.60	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs}	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 5.5A		9		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2200		pF
C _{oss}	Output Capacitance			285		pF
C _{rss}	Reverse Transfer Capacitance			30		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300V$, $I_D = 5.5 A$ $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 3)		27		ns
t_r	Rise Time			12		ns
Q_g	Total Gate Charge	$V_{DD} = 480V$, $I_D = 11 A$, $V_{GS} = 10V$, $R_G = 4.7\Omega$		54	70	nC
Q_{gs}	Gate-Source Charge			17		nC
Q_{gd}	Gate-Drain Charge			23		nC

SWITCHING OFF

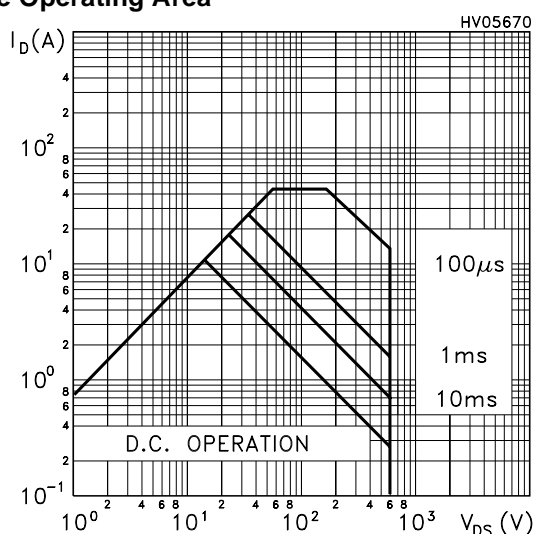
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 480V$, $I_D = 11 A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 5)		20		ns
t_f	Fall Time			15		ns
t_c	Cross-over Time			32		ns

SOURCE DRAIN DIODE

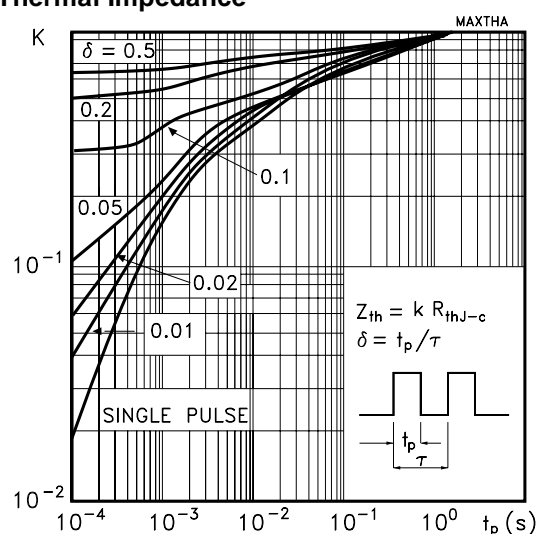
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				12	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				48	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 12 A$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 11 A$, $di/dt = 100 A/\mu s$, $V_{DD} = 100V$, $T_j = 150^\circ C$ (see test circuit, Figure 5)		600		ns
Q_{rr}	Reverse Recovery Charge			6.5		μC
I_{RRM}	Reverse Recovery Current			20.5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

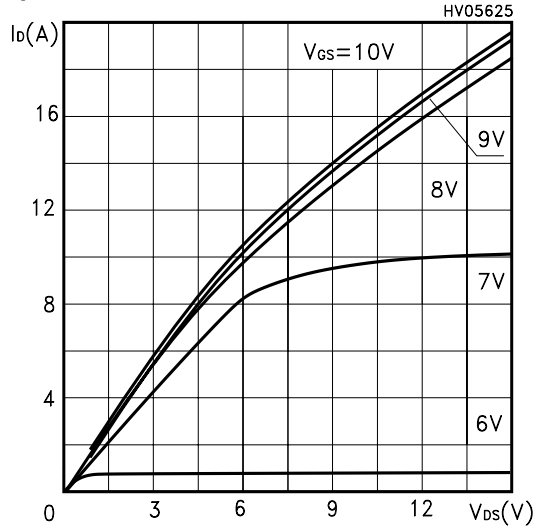
Safe Operating Area



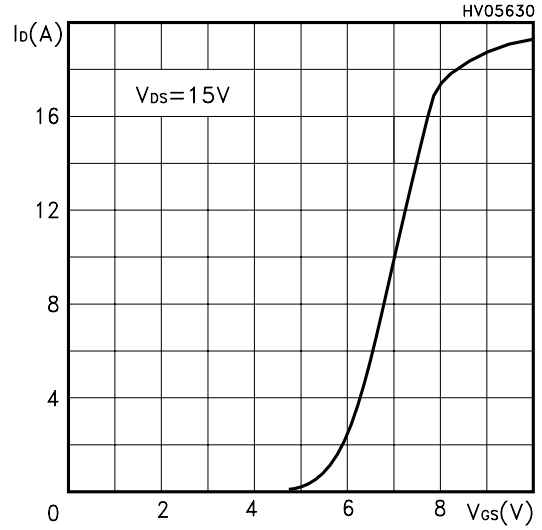
Thermal Impedance



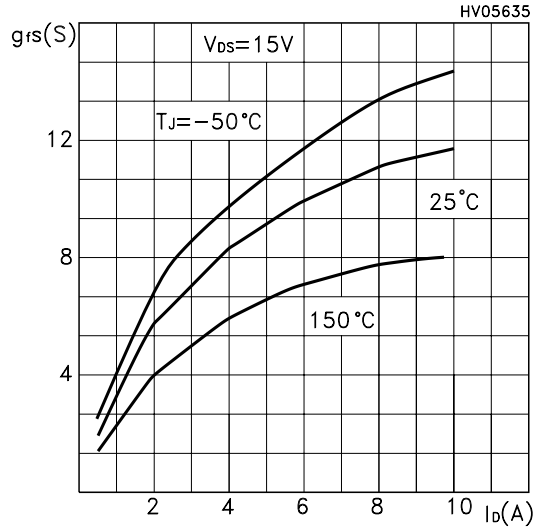
Output Characteristics



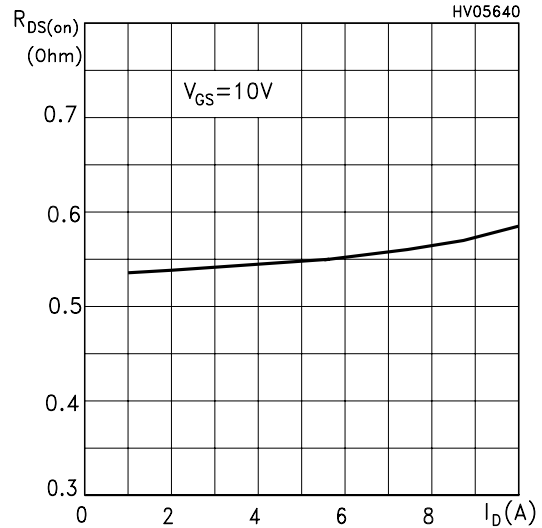
Transfer Characteristics



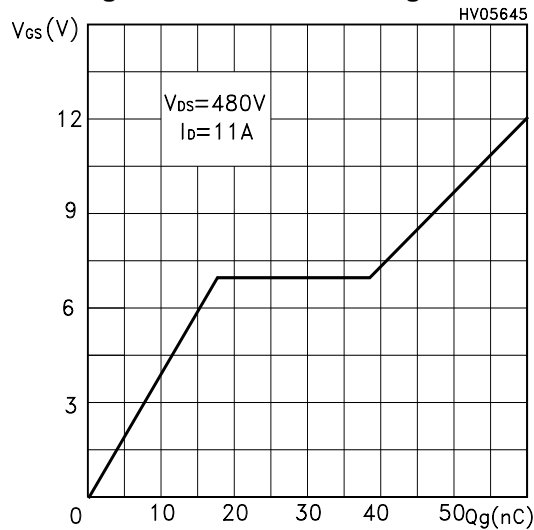
Transconductance



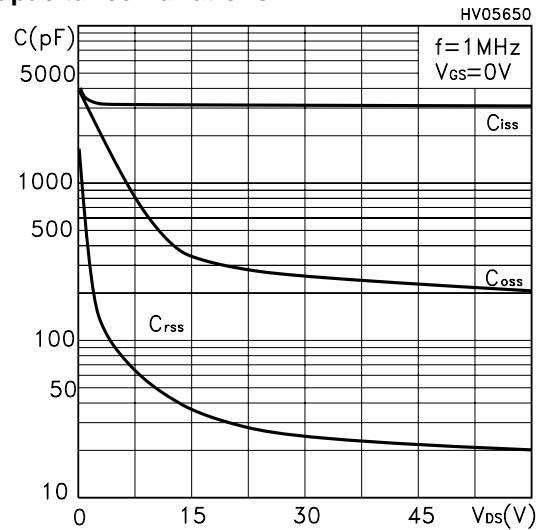
Static Drain-source On Resistance



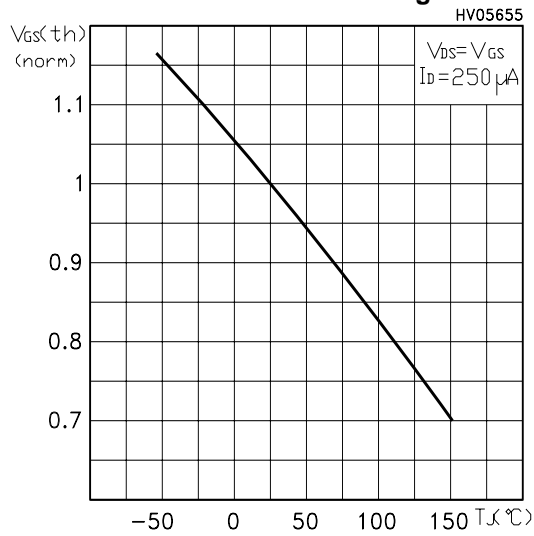
Gate Charge vs Gate-source Voltage



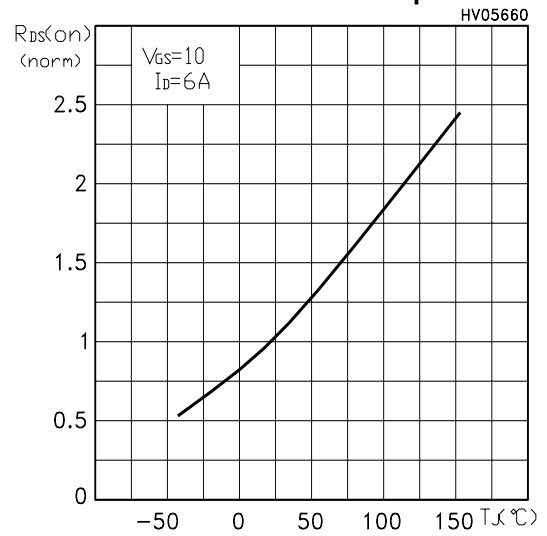
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

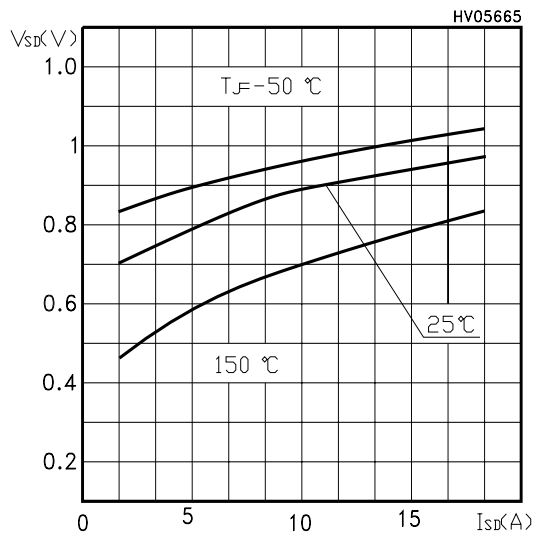


Fig. 1: Unclamped Inductive Load Test Circuit

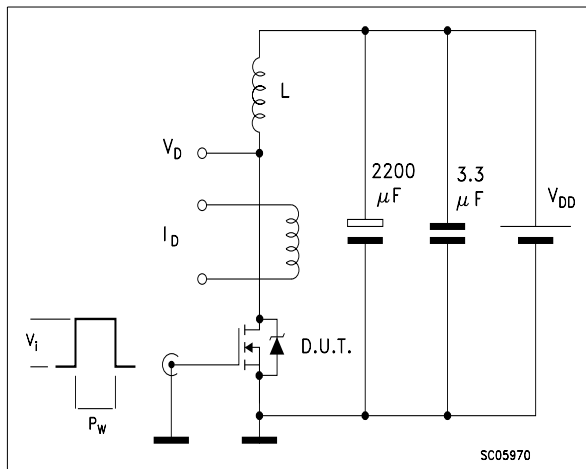


Fig. 2: Unclamped Inductive Waveform

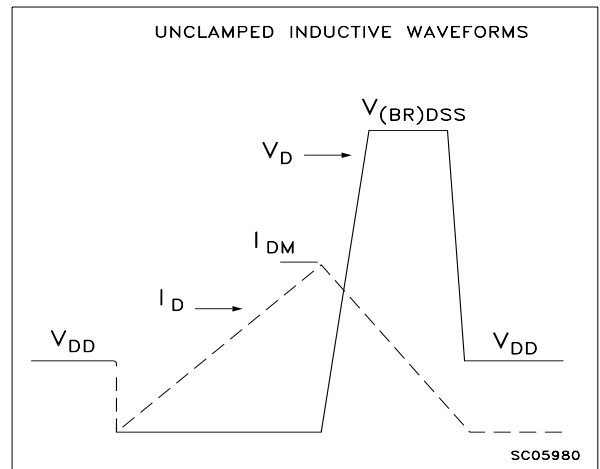


Fig. 3: Switching Times Test Circuit For Resistive Load

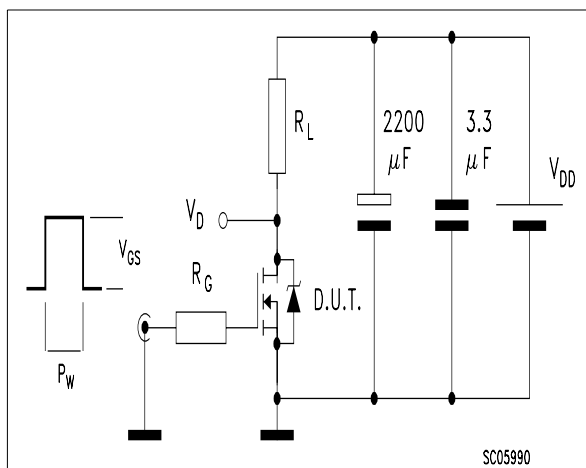


Fig. 4: Gate Charge test Circuit

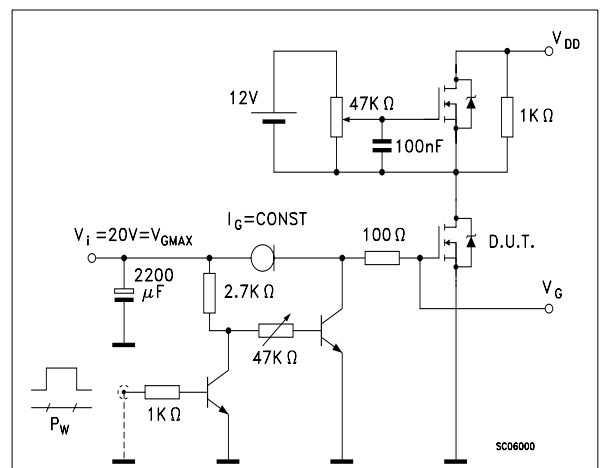
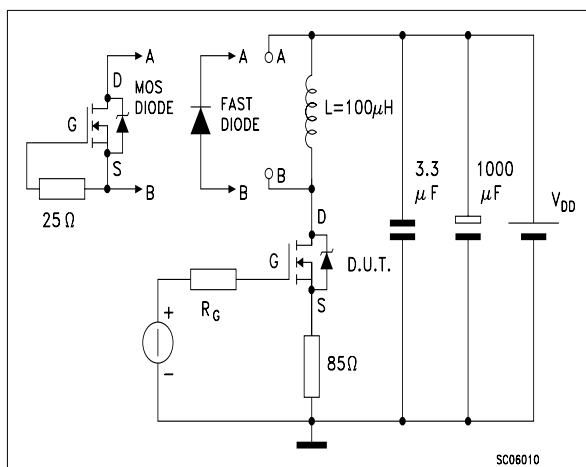
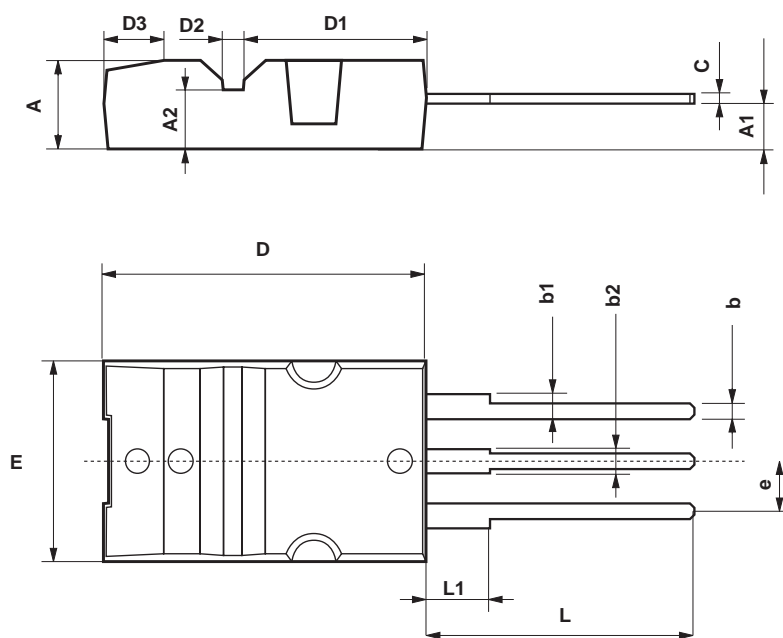


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



Max220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.3		4.6	0.169		0.181
A1	2.2		2.4	0.087		0.094
A2	2.9		3.1	0.114		0.122
b	0.7		0.93	0.027		0.036
b1	1.25		1.4	0.049		0.055
b2	1.2		1.38	0.047		0.054
c	0.45		0.6		0.18	0.023
D	15.9		16.3		0.626	0.641
D1	9		9.35	0.354		0.368
D2	0.8		1.2	0.031		0.047
D3	2.8		3.2	0.110		0.126
e	2.44		2.64	0.096		0.104
E	10.05		10.35	0.396		0.407
L	13.2		13.6	0.520		0.535
L1	3		3.4	0.118		0.133



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