

PAL LUMA-CHROMA & DEFLECTION PROCESSOR

PRELIMINARY DATA

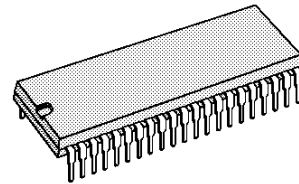
- RGB AND FAST BLANKING INPUTS
- AUTOMATIC CUT-OFF CONTROL
- DC-CONTROLLED BRIGHTNESS, CONTRAST AND SATURATION
- CERAMIC 500kHz VCO FOR LINE DEFLECTION
- PHASE-LOCKED REFERENCE OSCILLATOR USING A STANDARD 4.43MHz
- OSD CAPABILITY ON OUTPUTS
- VIDEO IDENTIFICATION GENERATOR

DESCRIPTION

The STV2102 is a PAL chroma decoder, video and H/V deflection processor for CTV.

Used with the TDA8222, this IC permits a complete low cost solution with external output stages.

It is pin compatible with STV2110 PAL/SECAM processor.



SHRINK 42
(Plastic Package)

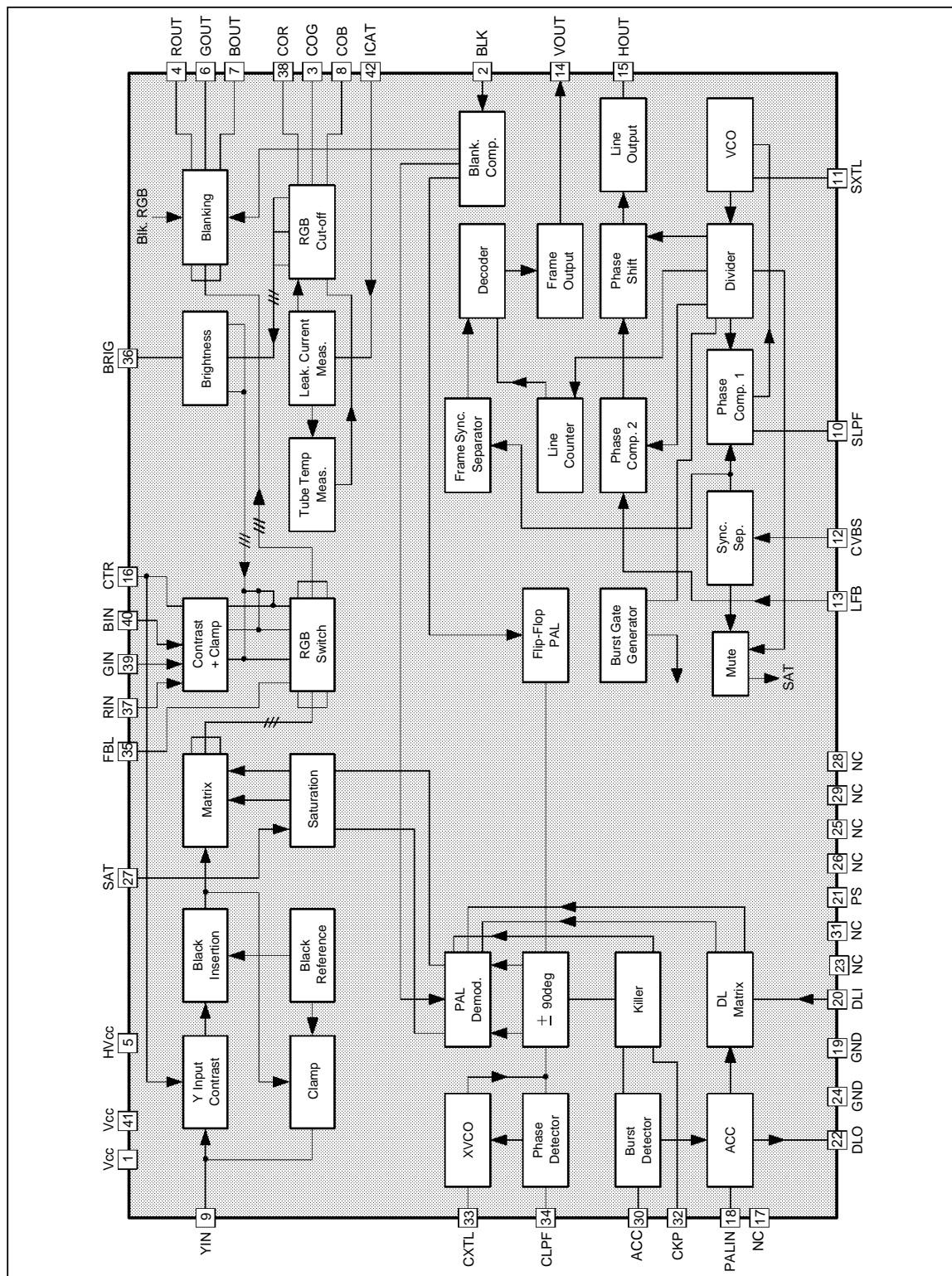
ORDER CODE : STV2102

PIN CONNECTIONS

SUPPLY VOLTAGE	Vcc	1	42	ICAT	CATHODE CURRENT
BLANKING INPUT	BLK	2	41	Vcc	SUPPLY VOLTAGE INPUT
GREEN CUT-OFF CAPACITOR	COG	3	40	BIN	BLUE INPUT
RED OUTPUT	ROUT	4	39	GIN	GREEN INPUT
HORIZONTAL Vcc	HVcc	5	38	COR	RED CUT-OFF CAPACITOR
GREEN OUTPUT	GOUT	6	37	RIN	RED INPUT
BLUE OUTPUT	BOUT	7	36	BRIG	BRIGHTNESS CONTROL
BLUE CUT-OFF CAPACITOR	COB	8	35	FBL	FAST BLANKING INPUT
LUMINANCE SIGNAL INPUT	YIN	9	34	CLPF	CHROMA LOOP FILTER
SCANNING LOOP FILTER	SLPF	10	33	CXTL	CHROMA XTAL
SCANNING XTAL	SXTL	11	32	CKP	PAL KILLER CAPACITOR
COMPOSITE VIDEO SIGNAL	CVBS	12	31	NC	NOT CONNECTED
LINE FLYBACK INPUT	LFB	13	30	ACC	ACC CONTROL CAPACITOR
VERTICAL OUTPUT	VOUT	14	29	NC	NOT CONNECTED
HORIZONTAL OUTPUT	HOUT	15	28	NC	NOT CONNECTED
CONTRAST CONTROL	CTR	16	27	SAT	SATURATION CONTROL
NOT CONNECTED	NC	17	26	NC	NOT CONNECTED
PAL CHROMA INPUT	PALIN	18	25	NC	NOT CONNECTED
GROUND	GND	19	24	GND	GROUND
DELAY CHROMA INPUT	DLI	20	23	NC	NOT CONNECTED
CHROMA STANDARD	PS	21	22	DLO	CHROMA OUTPUT

2102-01.EPS

2102-02.EPS



FUNCTIONAL DESCRIPTION

DEFLECTION

Synchronization Separator

The synchronization separator is based on the bottom of synchronization pulses alignment to an internal reference voltage. An external capacitor permits to align synchro. pulses, two external resistors determines the detection threshold of synchro pulses. The frame synchronization pulses are locked to a 32 μ s reference signal to perfect interlacing.

Horizontal Scanning

The horizontal scanning frequency is obtained from a 500kHz VCO. The circuit uses two phase-locked loops (PLL). The first one controls the frequency; the second one, fully integrated, controls the relative phase of the synchronization and the line fly-back signals.

The first PLL has two time constants : a long time constant during the picture to have a good noise immunity, a short time constant at the beginning of the frame to recapture faster the phase in case of VCR video signal. Moreover, the PLL is in short time constant three lines before frame pulses occurred, it permits to ensure good interlacing when the video signal comes from a VCR tape with high phase error.

The horizontal output signal is 28 μ s width. On starting up, horizontal pulses are enabled at $V_{CC} = 6.8V$. On shutting down, horizontal pulses are inhibited for $V_{CC} = 6.2V$.

The vertical output signal is 10.5 lines width. It permits to drive a sawtooth generator such as TDA1771.

A video recognition function permits to send the information of no video identification to SAT pin : it forces a low level when no video detection occurs.

CHROMA

ACC Amplifier, DL Matrix and Demodulator

The correct chroma subcarrier input, issued from bandpass, is internally selected with the standard. The ACC amplifier involves three stages : the first one selects the correct input, the second one the -6dB in picture (PAL mode), the third one is controlled by the ACC voltage.

The dynamic range is over than 30dB.

The chrominance output signal is fed to the delay line.

The adding and subtracting direct and delayed signals are performed by the DL matrix function.

Two synchronous demodulators multiply the (B-Y) signal with the 0 degree phase 4.43MHz reference signal and the (R-Y) signal with the alternate ± 90 deg. 4.43MHz phase reference signal.

4.43MHz Phase Locked Loop

The oscillating frequency of the 4.43MHz crystal oscillator is controlled by the output voltage of the loop filter. The phase detector will lock the 90 degree reference signal to the direct burst signal. A 90 degree phase shifter permits to recover the 0 degree reference signal. A flip-flop driven by line pulses permits to generate the alternate ± 90 degree signal.

ACC Control and Color Killer

The direct burst signal is demodulated with the ± 90 degree reference signal. The demodulation result is used by ACC control and killer function.

If the demodulation result is always positive, the killer capacitor is charged and the standard is identified (color ON). When demodulation result is always negative, the killer capacitor voltage reaches the flip-flop inhibition level, so the alternate sequence is reversed and the capacitor is charged again.

In case of no video signal, the killer capacitor voltage is maintained about $V_{CC}/2$, below the color off threshold.

VIDEO

The luminance input is controlled by the contrast control stage which range is 20dB.

The luminance and color difference signals are added in the video matrix circuit to obtain the color signals.

The color signals are sent to an RGB switch which will drive to the outputs either internal RGB signals or external RGB signals.

Automatic Cut-off Control

The black levels of the RGB outputs are controlled with the cut-off loops during three line periods after the frame retrace. The cut-off measurements are sequentially achieved during these three lines. The leakage current measurement is achieved during the frame retrace and memorized on an internal capacitor, thus the circuit is able to extract the cut-off current from the total current measurement.

Warm-up Detector

At the start-up, the cut-off loops are switched off, a white level is inserted on the luminance signal until a cathode current is detected. Then the cut-off loops are released.

RGB Inputs

To avoid the black level of the inserted signal differing from the black level of the normal video signal, the external RGB are clamped to the black

level of the luminance signal. Therefore, an AC coupling is required for the RGB inputs.

The RGB inputs are controlled by a 12dB range contrast control stage.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12	V
T_{stg}	Storage Temperature	-55, +150	°C
T_{oper}	Operating Temperature	0, +70	°C

2102-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	Max. 70	°C/W

2102-02.TBL

DC AND AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 9V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HV_{CC}	Scanning Supply Voltage (Pin 5)		8.1	9	9.9	V
V_{CC}	Video & Chroma Supply Voltage (Pins 41-42)		8.1	9	9.9	V
I_{och}	Scanning Supply Current (pin 5)	No load		20	30	mA
$I_{ccv\&c}$	Video & Chroma Supply Current (Pins 41-42)	No load		45	55	mA
P_D	Total Power Dissipation	No load		580	850	mW

LUMINANCE INPUT (Pin 9)

V_{BW9}	Input Level before Clipping (black to white)			350		mV _{PP}
V_{DC9}	DC Operating Voltage	No input signal		2.5		V
I_g	Input Current	<ul style="list-style-type: none"> During burst period Out of burst period 		±100	5	μA μA
G_9	Luma Gain			5.5		

CONTRAST CONTROL (Pin 16)

V_{16}	Contrast Control Voltage			2 to 4		V
$V_{16(Max.)}$	Maximum Allowed Control Voltage		5			V
G_{16}	Contrast Control Range			20		dB
I_{16}	Input Current				10	μA

BRIGHTNESS CONTROL (Pin 36)

V_{36}	Brightness Control Voltage			1.5 to 4.5		V
$V_{36(Max.)}$	Maximum Allowed Control Voltage		5			V
I_{36}	Input Current				10	μA

SATURATION CONTROL INPUT (Pin 27)

I_{29}	Input Current				10	μA
V_{29}	Saturation Control Voltage			2 to 4		V
$V_{29(Max.)}$	Maximum Allowed Control Voltage		5			V
G_{29}	Saturation Control Range			-50		dB

RGB CLAMP CAPACITORS (Pins 4-7-39)

I_{4-7-39}	Control Current			±150		μA
$I_{i4-7-39}$	Leakage Current			1		μA

RGB OUTPUTS (Pins 4-6-7)

$V_{BW 4-6-7}$	Output Signal Amplitude (black to white)	<ul style="list-style-type: none"> 0.35V B to W @ Pin 9 Contrast @ max Sat. & Brig. @ 3V 		2		V
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2102-03.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)(V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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RGB OUTPUTS (Pins 4-6-7) (continued)

I ₄₋₆₋₇	Individual Output Sinking Current			2		mA
VM ₄₋₆₋₇	Maximum Peak White Level			7.8		V
V _{blank 4-6-7}	Blanking Level			0.7		V
	Relative Variation in Black Level with Various CONT. SAT. BRIG between the 3 channels				20	mV
ΔV _{temp}	Black Level Thermal Drift			0.5		mV/°C
BW ₄₋₆₋₇	Bandwith	- 3dB		5		MHz
	Tracking between Luminance and Chrominance Signals over 10dB Contrast Control				2	dB

RGB INPUTS (Pins 37-39-40)

V _{BW37-39-40}	Maximum Input Level (B to W)				2	V
V _{clamp 37-39-40}	Clamp Level	Contrast max		1.5		V
BW ₃₇₋₃₉₋₄₀	Bandwidth	-3dB		8		MHz
G _{CTR}	RGB Contrast Control Range			12		dB
G ₃₇₋₃₉₋₄₀	RGB Gain			4		

FAST BLANKING INPUT (Pin 35)

V _{TH1-35}	First Threshold (switching)			0.7		V
V _{TH2-35}	Second Threshold (switching)			2.1		V
I ₃₅	Input Current	0V @ Pin 35			50	μA
T _{switch}	Switching Delay			50		ns
T _{blank}	Blanking Delay			50		ns

CATHODE CURRENT INPUT (Pin 42)

	Leakage Current Reference Voltage			1.75		V
	CO Reference referred to Leakage Current Reference			250		mV
	Low Voltage Output Current				200	μA

AUTOMATIC CUT-OFF (Pin 3-8-38)

	Capacitor Cut-off Positive Negative Clamping			100		μA
	Start-beam Current Detection Reference Voltage			2		V
V ₄₋₆₋₇	Cut-off Output Range			3		V

CHROMINANCE INPUT (Pin 18)

V ₁₈	Input Level Before Clipping			900		mV _{pp}
V _{burst-18}	Minimum Burst Signal Amplitude within the ACC Control Range			30		mV _{pp}
G _{ACC}	ACC Control Range	Change of burst over whole ACC Control Range < 1dB		30		dB
R ₁₈	Input Impedance			8		kΩ
V _{DC-18}	DC Operating Voltage	No input signal		3.5		V

ACC CAPACITOR (Pin 30)

I ₃₀	Charging Current	During burst gate period		250		μA
I ₃₀	Leakage Current	Out of burst gate period			1	μA

PLL LOOP FILTER (Pin 34)

I ₃₄	Control Current			400		μA
I ₃₄	Leakage Current				5	μA

CHROMAXTAL (Pin 33)

CR ₃₃	Catching Range			700		Hz
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2102-04.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)(V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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SUBCARRIER OUTPUT (Pin 22)

V _{burst-22}	Output Burst Amplitude (PAL mode)	Within ACC Control Range		2.2		V _{pp}
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KILLER CAPACITOR (Pin 32)

V _{OFF-32}	Collor off Voltage	No chroma signal		4.9		V
V _{ON-32}	Color on Voltage			5.4		V
V _{INH-32}	PAL Flip-flop Inhibition Level			3.2		V
I ₃₂	Control Current			250		μA
I ₃₂	Leakage Current				5	μA
V _{nom-32}	Voltage with Nominal Input Signal			6.0		V

DELAYED CHANNEL INPUT (Pin 20)

V _{DC-20}	DC Operating Voltage	No input Signal		2.2		V
R ₂₀	Input Impedance	PAL standard		8		kΩ

COMPOSITE VIDEO BASE BAND SIGNAL (Pin 12)

V _{REF-12}	Voltage Reference	I ₁₂ = -1μA	0.6	0.8	1.0	V
V ₁₂	Video Input Signal				2.5	V _{PP}

SCANNING XTAL (Pin 11)

F ₁₁	Frequency after Divider			15.625		kHz
CR ₁₁	Frequency Control Range after Divider			±700		Hz

PLL LOOP FILTER (Pin 10)

I _{low-10}	Low Loop Gain Output Current			0.15		mA
I _{high-10}	High Loop Gain Output Current			0.40		mA
	Window Pulse Width			4		μs

DELAYED LINE FLYBACK INPUT (Pin 13)

V _{TH-13}	Threshold			0.6		V
V ₁₃	Line Flyback Amplitude		1.5			V _{PP}
V _{DC-13}	Minimum Negative Voltage		-0.4			V
I ₁₃	Input Current				5	μA

DIRECT BLANKING INPUT (Pin2)

V _{TH-2}	Threshold			0.6		V
V ₂	Line Flyback Amplitude		1.5			V _{pp}
V _{DC-2}	Minimum Negative Voltage		-0.4			V
I ₂	Input Current				5	μA
Ph ₂	External Adjustment	Appli. Adjust.	2	4	6	μs

HORIZONTAL OUTPUT (Pin 15)

T ₁₅	Output Pulse Width		26	28	29	μs
V _{low-15}	Output Voltage (open collector)	I ₁₅ = 10mA		1		V
V _{start-15}	V _{CC} Start Level			6.8		V
V _{stop-15}	V _{CC} Stop Level			6.2		V
Δt ₁₅	φ2 Phase Range			10		μs

VERTICAL OUTPUT (Pin 14)

T ₁₄	Output Pulse Width			10.5		lines
T _{sync}	Frame Synchro. Window			248 to 352		line
V _{low-14}	Output Voltage (Open collector)			1		V

2102-05.TEL

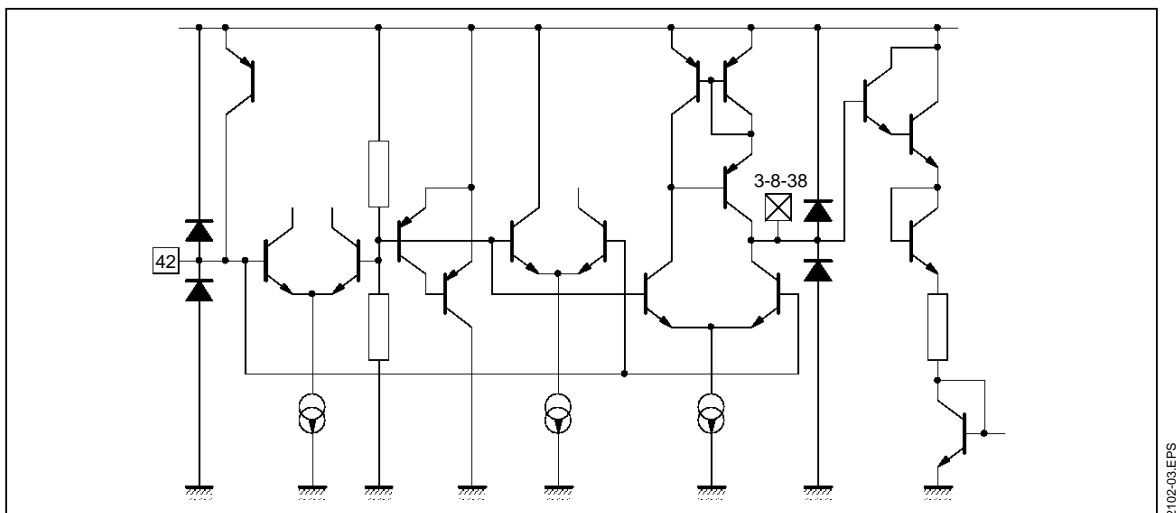
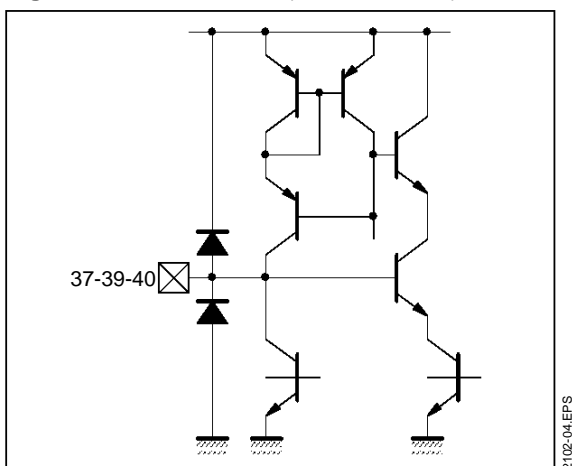
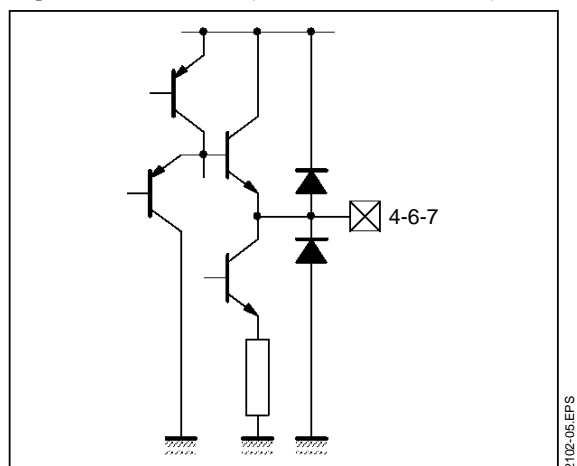
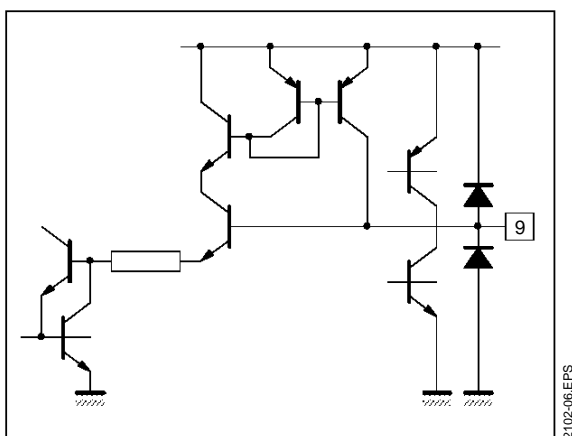
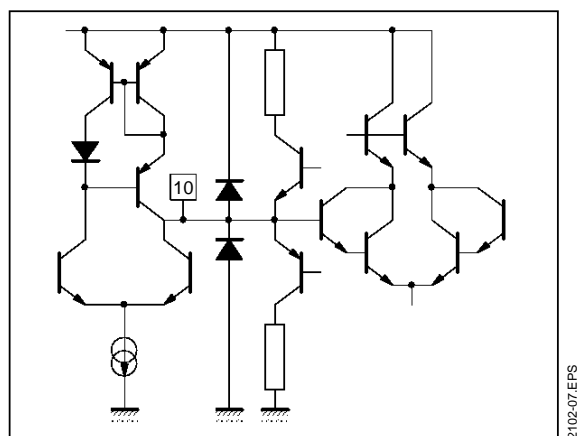
Figure 1 : Pins 3-8-38-42 (COG, COB, COR, ICAT)**Figure 2 :** Pins 37-39-40 (RIN, GIN, BIN)**Figure 3 :** Pins 4-6-7 (ROUT, GOUT, BOUT)**Figure 4 :** Pin 9 (YIN)**Figure 5 :** Pin 10 (SLPF)

Figure 6 : Pin 11 (SXTL)

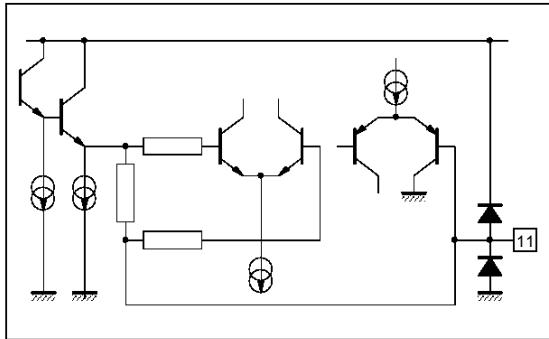


Figure 7 : Pin 12 (CVBS)

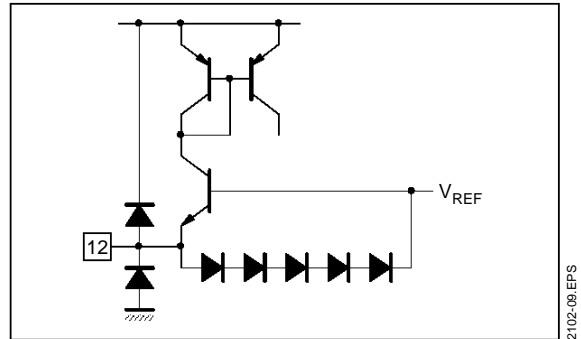


Figure 8 : Pins 2-13 (BLK, LFB)

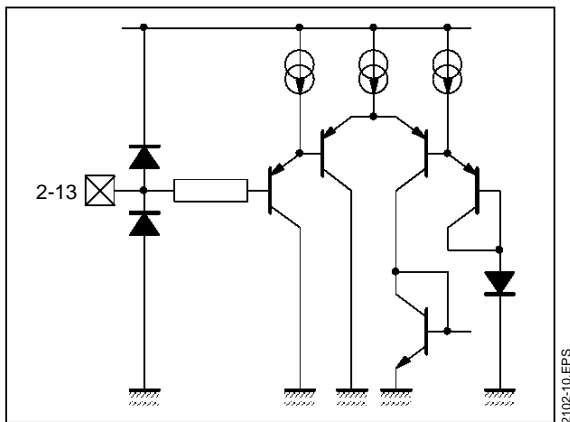


Figure 9 : Pins 14-15 (VOUT, HOUT)

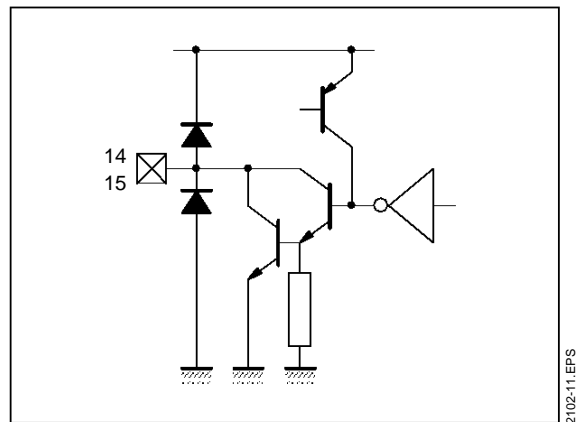


Figure 10 : Pins 16-27 (CTR, SAT)

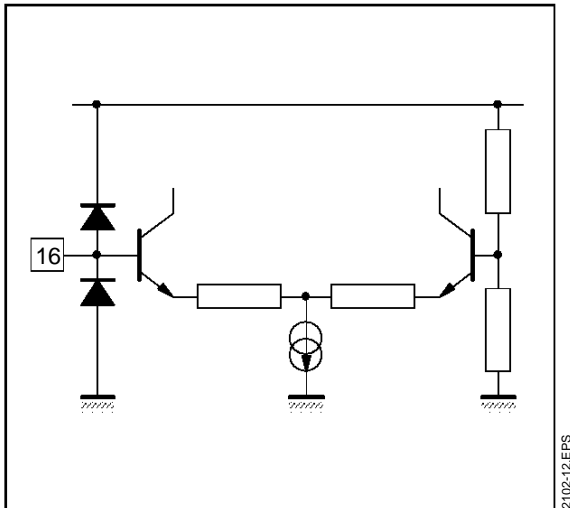


Figure 13 : Pin 18 (PALIN)

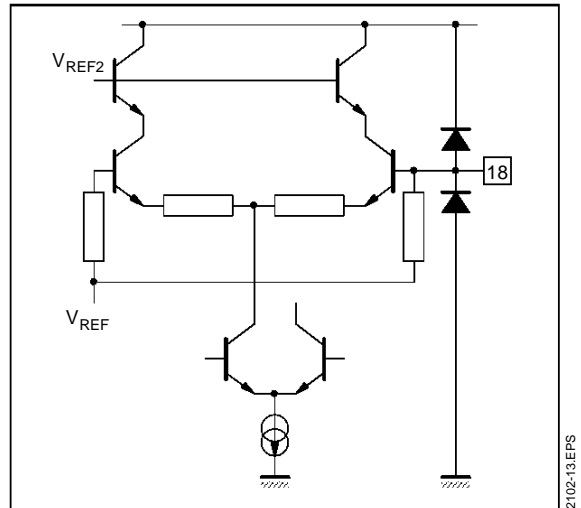
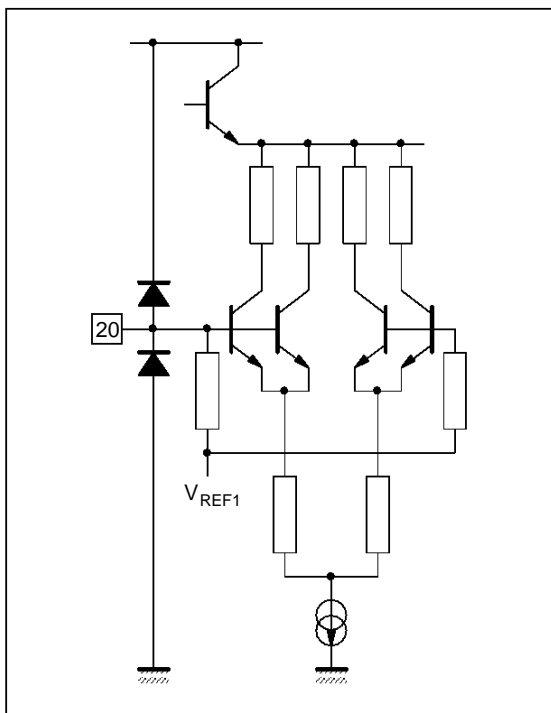
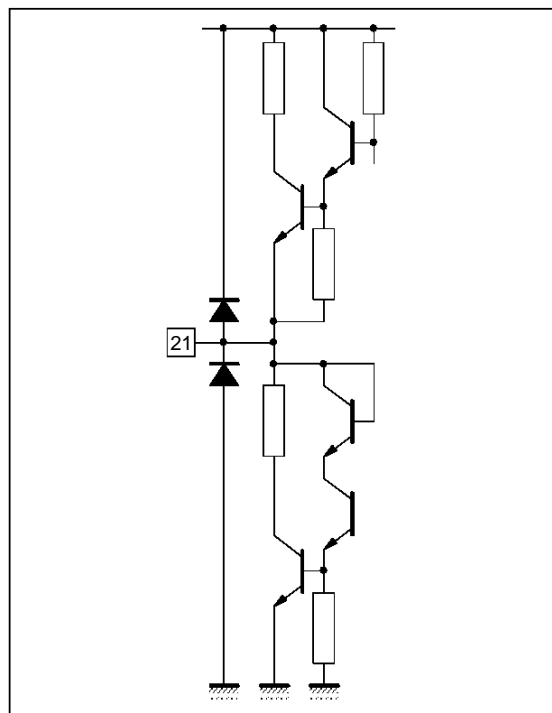


Figure 11 : Pin 20 (DLI)



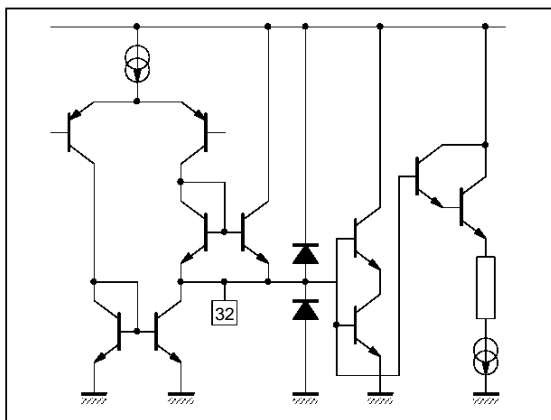
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Figure 12 : Pin 21 (PS)



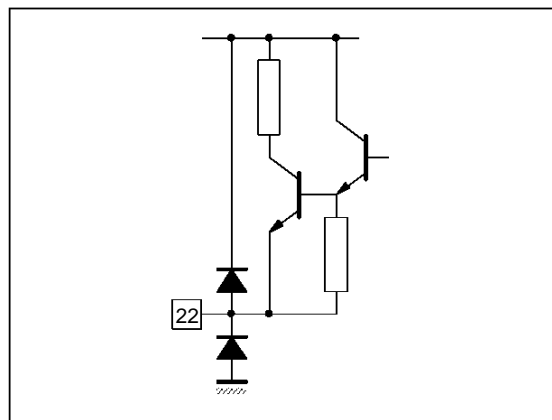
2102-15.EPS

Figure 14 : Pin 32 (CKP)



2102-16.EPS

Figure 15 : Pin 22 (DLO)



2102-17.EPS

Figure 16 : Pin 30 (ACC)

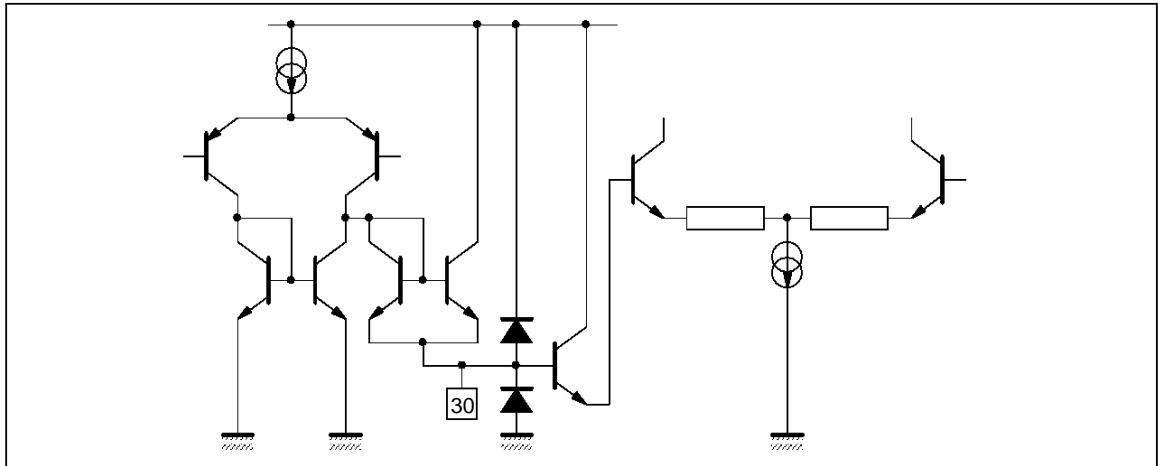


Figure 17 : Pin 36 (BRIG)

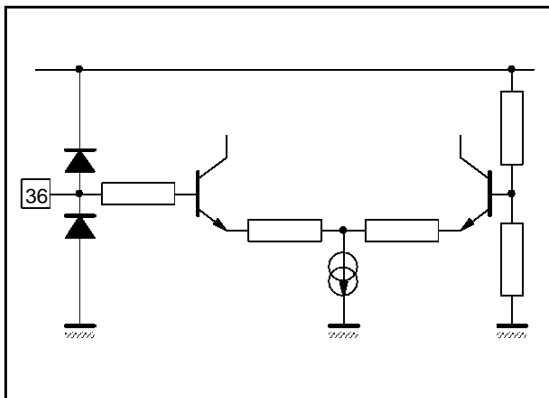


Figure 18 : Pin 33 (CXTL)

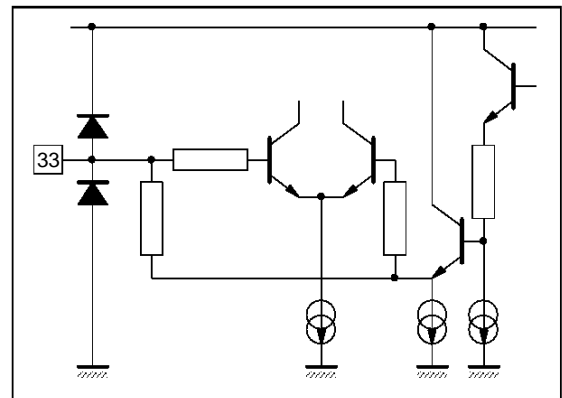


Figure 19 : Pin 34 (CLPF)

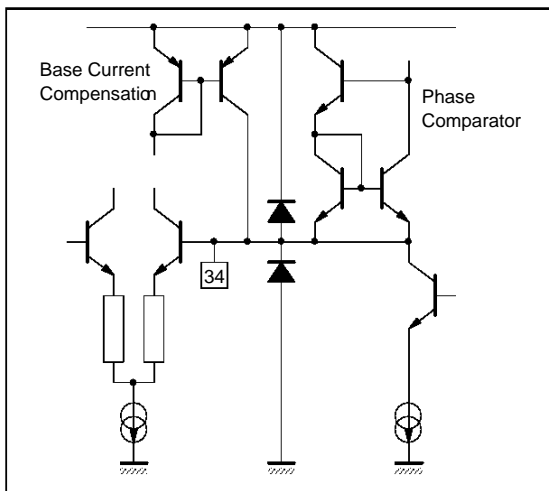
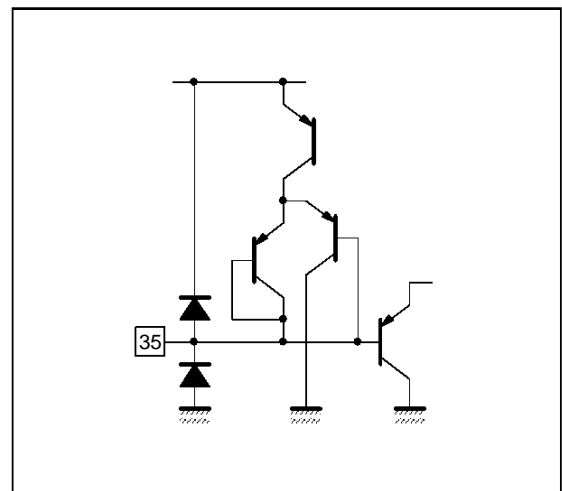
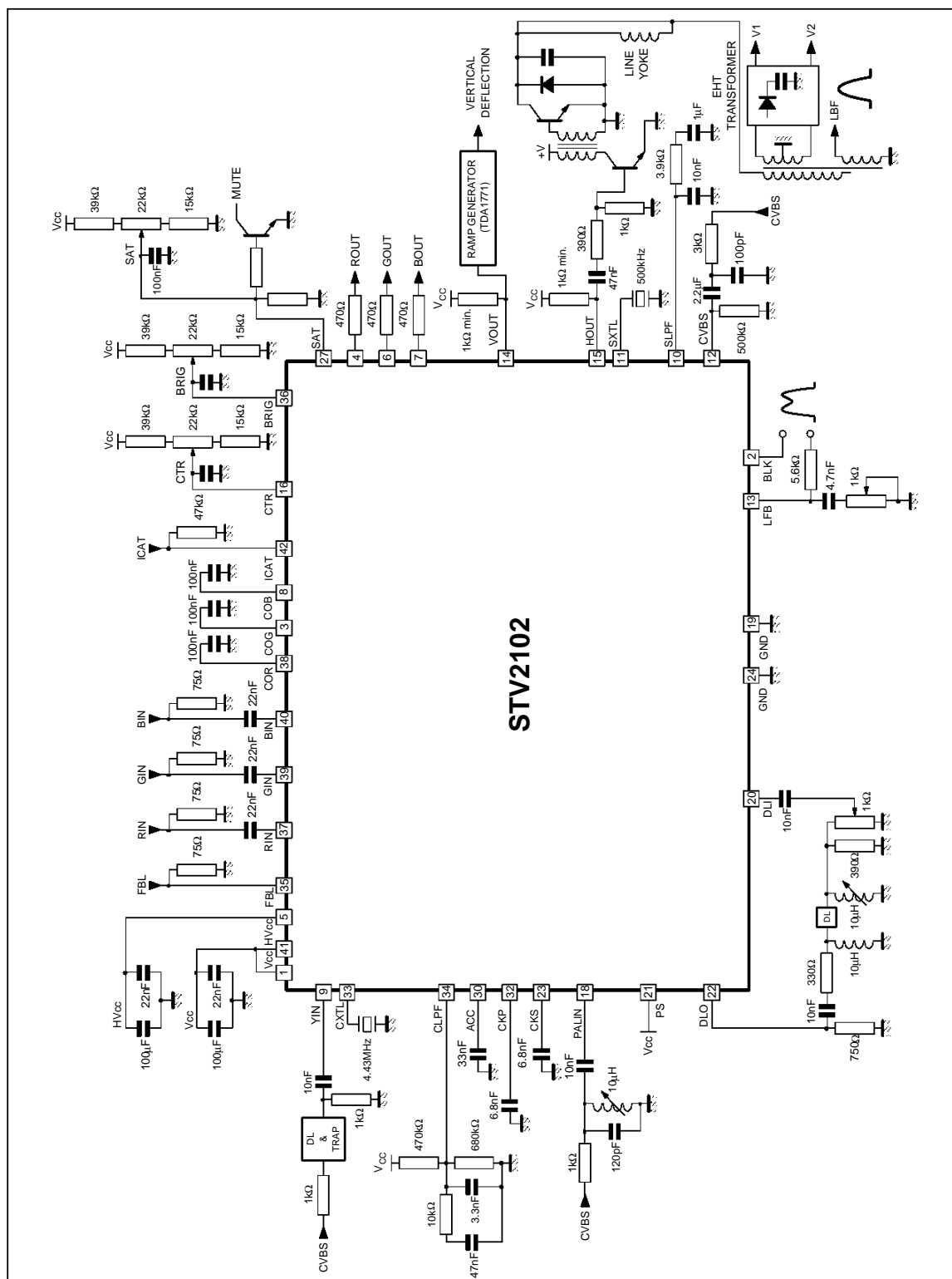


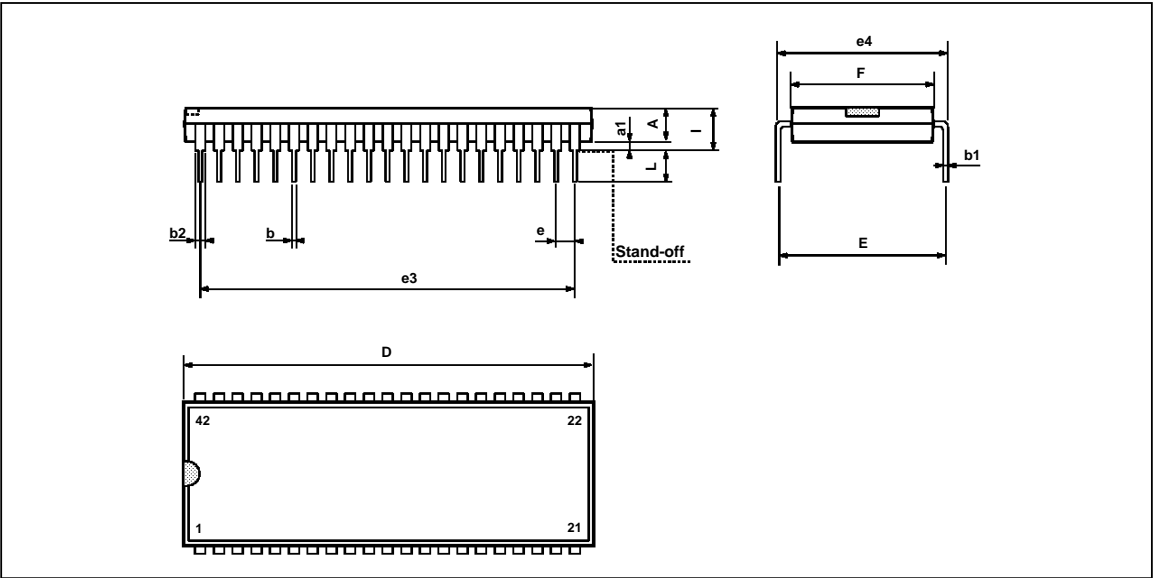
Figure 20 : Pin 35 (FBL)



APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA
42 PINS - PLASTIC SHRINK DIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.30			0.130		
a1		0.51			0.020	
b		0.35	0.59		0.014	0.023
b1		0.20	0.36		0.008	0.014
b2		0.75	1.42		0.030	0.056
b3		0.75			0.030	
D			39.12			1.540
E		15.57	17.35		0.613	0.683
e	1.778			0.070		
e3	35.56			1.400		
e4	15.24			0.600		
F			14.48			0.570
i			5.08			0.200
L		2.54			0.100	

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