

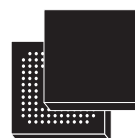


TRANSCEIVER MODULE

REV. 1.0 - PRODUCT PREVIEW

1 FEATURES

- Triple-band (GSM850 / DCS1800 / PCS1900).
- Supports data transfer applications in multi-slots GPRS class-12
- EDGE Receive capability
- Integrates:
 - BiCMOS6G RF transceiver
 - 3 Receive Band Pass filters
 - 3 Receive Matching Network between filters output & LNA input
 - PLL loop filter
 - Decoupling / DC blocking capacitors
- Insures compatibility with different Power Modules
 - STW3102 Power Module
 - Power Module coming from the competition
- RF interfaces:
 - Single-ended 50 ohms acceses
 - 3 in Rx
 - 2 in Tx
- Noise Figure in
 - Low band : 5.5 dB typ
 - Hign bands : 6 dB typ
- Transmit output level:
 - GSM850 band : 1 or 5 dBm typ
 - DCS & PCS bands : 1 or 5 dBm typ
- Standard Rx / Tx differential I/Q analogue interface
- Supply voltage range: 2.7V min / 3.3V max
- Embedded voltage regulators to supply on chip RF functions
- Package:
 - Full lead-free
 - 104 -BGA 7 x 7 pack
- Temperature range:
 - Case operating temperature range: -20°/ +70°C (fulfil specification)
- ESD handling:



LFBGA104 (7x7x1.4mm)
ORDERING NUMBER: STW3101

- ± 2 kV Human Body Model
- Control interfaces:
 - Towards Baseband: 3-wire serial interface with a Clock (Clk), enable (En) and a data line (Data).
 - Towards Front-End functions 3 control pins

2 DESCRIPTION

In a 1.4 x 7 x 7mm low-profile Ball Grid Array package, the new modules integrate all of the key functions, requiring only a 26MHz crystal and a power amplifier module (PA+antenna switch functions) to build a complete triple-band solution from antenna to base band interface. Two versions are offered: type STw3100 addresses the European EGSM900, DCS1800, and PCS1900 bands while the STw3101 targets the US GSM850, DCS1800, and PCS1900 bands. The transceiver modules are compatible with the STMicroelectronics STw3102 power-amplifier module and most of the standard power amplifiers available on the market.

3 ELECTRICAL CHARACTERISTICS

3.1 DC SECTION

Limiting value

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Absolute Maximum Ratings						
V _{CC}	Maximum voltage supply				3.6	V
T _{stg}	Storage Temperature		-55	25	125	°C
P _{diss}	Maximum Power dissipation				500	mW
Operating Functionality range						
T _{op}	Operating Temperature		-40	25	85	°C
V _{CC}	Supply voltage on Vcc_SYN and Vcc_RX/TX pins		2.7		3.3	V
Operating Specified range						
T _{op}	Operating Temperature		-20	25	70	°C
V _{CC}	Supply voltage on Vcc_SYN and Vcc_RX/TX pins		2.7		3.3	V

DC characteristics

V_{CC} = 2.7V;

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Pin Vcc_syn						
I _{cc}	Supply current in power off mode			10		μA
I _{cc}	Supply current in REF mode			3		mA
I _{cc}	Supply in Syn mode			35		mA
Pin Vcc_RX/TX						
I _{cc}	Supply current in power off mode			10		μA
I _{cc}	Supply current in RX mode			35		mA
I _{cc}	Supply current in TX mode GSM bands			88		mA
I _{cc}	Supply current in TX mode DCS or PCS bands			88		mA
Pin Vccreg_RFVCO						
V _{ccreg}	Internal regulated supply voltage			2		V
Pin Vccreg_TXVCO						
V _{ccreg}	Internal regulated supply voltage			2		V
Pin Vccreg_Digital						
V _{ccreg}	Internal regulated supply voltage			1.8		V

3.2 Receive Section

V_{CC} = 2.7V;

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f _{RX2}	Input Frequency	GSM850	869		894	MHz
f _{RX3}		GSM1800	1805		1880	
f _{RX4}		GSM1900	1930		1990	
Z _{in}	Input impedance	Single-Ended		50		Ω
VSWR _{in}	Input VSWR into 50 ohm			1.8	2.3	
Ripple	Gain Flatness over the Frf band			1	2	dB
G _{max}	Total max gain	in 2Vpp Mode	74		79	dB
		in 4Vpp Mode	80		85	
ΔG	Gain range			66		dB
	AGC gain step		-	3	-	
	AGC linearity		-1		+1	dB
NF	Noise figure DSB	Low Band		5.5		dB
		High Band		6		
ICP _{-1dB}	1dB Input Compression Point @ Low gain, 0kHz offset	Low Band	-23	-20		dBm
		High Band	-26	-23		
IIP3	Third Order Input Intercept Point @ High Front-end gain	Low Band	-14	-10		dBm
		High Band	-14	-12		
IIP2	2 nd Order Input Intercept Point	High Front-end gain	+44			dBm
C/N	Out-of-band Blocking (a, b, c, d) in Low-Band & (a, d) in High-Band	P _{wanted} = -100 dBm, P _{interf} = -1 dBm (1 dB Insertion Losses for antenna switch)	9			dB
C/N	Out-of-band Blocking (c, b) in High-Band	P _{wanted} = -100 dBm, P _{interf} = -13 dBm	9			dB
C/N	In-Band Blocking @ IF-Fol > 3 MHz	P _{wanted} = -100 dBm, P _{interf} = -24 dBm (LB) P _{interf} = -27 dBm (HB)	9			dB
C/N	In-Band Blocking @ 1.6 MHz < IF-Fol < 3 MHz	P _{wanted} = -100 dBm, P _{interf} = -34 dBm	9			dB
C/N	In-Band Blocking @ 600 kHz < IF-Fol < 1.6 MHz	P _{wanted} = -100 dBm, P _{interf} = -44 dBm	9			dB
BW _{GMSK} BW _{EDGE}	3 dB Channel bandwidth	after calibration	90 110		110 140	kHz
Att _{GMSK} Mode	Channel response attenuation @ 200 kHz @ 400 kHz @ 600 kHz		15 50 58	18 51 62		dB
Att _{EDGE} Mode	Channel response attenuation @ 200 kHz @ 400 kHz @ 600 kHz		4 45 52	7 48 55		dB
T _{delay}	Group delay variation	Between 0 & 67.7 kHz		1.8	2.5	us
Spurs	Spurious emission @ RF input @ 9 kHz – 1 GHz @ 1 GHz – 12.75 GHz				-57 -47	dBm

3.2 Receive Section (continued)

V_{CC} = 2.7V;

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Δ GIQ	I & Q Gain mismatch		-1		+1	dB
$\Delta\Phi$ IQ	I & Q quadrature mismatch		-5		+5	deg
V _{Cm}	Output Common mode voltage		1.2	1.35	1.5	V
V _{Swing}	Maximum single ended Output Voltage	4Vpp mode 2Vpp mode	0.75 0.375			V _{pk}
V _{offset}	Differential Output Offset Voltage	after calibration	-150	±20	+150	mV
T _{offset}	Offset voltage calibration settling time (during the locking time phase)				200	us

3.3 Transmit Section

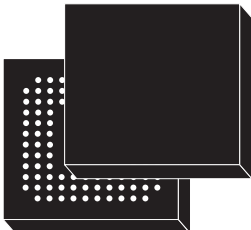
V_{CC} = 2.7V;

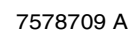
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Pins ITX(+), ITX(-), QTX(+) and QTX(-)						
F _{mod}	Modulation frequency range	3dB low pass cut-off frequency	1	-	-	MHz
V _{DC mod}	Input Common mode voltage		0.8	1	1.4	V
V _{mod}	Modulation level	Single ended; peak to peak value	0.8	1	1.2	V _{pp}
V _{DC offset}	Input DC offset permissible	Differential			10	mV
R _{IN}	Dynamic input resistance	Single ended	10	-	-	kΩ
C _{IN}	Dynamic input capacitance	Single ended	-	-	20	pF
		differential			56	
RF Tx performances						
f _{TX2}	Output frequency	GSM850	824		849	MHz
f _{TX3}		GSM1800	1710		1785	
f _{TX4}		GSM1900	1850		1910	
Z _{out}	Output impedance	Single-Ended		50		Ω
VSWR _{out}	Output VSWR into 50 ohm			1.5	2	
POUTGMSK	Output power into 50 ohm load	Set to Pout _0		+1		dBm
		Set to Pout _1		+5		
ACPR400	ACPR @ 400 kHz offset (BW = 30 kHz)	Low Band		-65	-62	dBc/BW
		High Band		-63	-61	
N20MHz	Output Phase Noise @ 20 MHz offset	Low Band		-164	-159	dBc/Hz
		High Band		-156	-152	
RMS	RMS phase error			1.2	2.5	deg
H2LB	2 nd Harmonic level				-20	dBc
H3LB	3 rd Harmonic level				-20	dBc
IMout	Unwanted sideband suppression			-45	-35	dBc
Crej	Carrier rejection			-40	-32	dBc

3.4 Frequency generation Section

V_{CC} = 2.7V;

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
RF synthesizer						
Tlock_time	Settling Time	$\phi_{\text{peak}} < 20^\circ$		150	200	us
	GSM850 Frequency Range		824.2		993.8	MHz
	DCS1800 Frequency Range		1710.2		1879.8	MHz
	DCS1900 Frequency Range		1850.2		1989.8	MHz
Fchannel	Channel spacing			200		kHz
Fstep	Synthesizer frequency step (Fract-N PLL)			0.0022		ppm
DCXO						
Fref	Reference Frequency (quartz input)			26		MHz
Frange crystal	Capacitor bank frequency range		-30		+30	ppm
Fstep crystal	Capacitor bank step		-	1	-	ppm

<p>OUTLINE AND MECHANICAL DATA</p>
 <p>Body: 7 x 7 x 1.4mm</p>
<p>LFBGA104 Low Fine Ball Grid Array</p>



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