

## High-Voltage Ring Generator

### Ordering Information

Operating Voltage	Package Options
$V_{PP1} - V_{NN1}$	SOW-16
220V	HV440WG

### Features

- ☐ 220V maximum operating voltage
- ☐ Integrated high voltage transistors
- ☐ Up to 70  $V_{RMS}$  ring signal
- ☐ Pulse by pulse output over current protection
- ☐ 5 REN output capability
- ☐ External MOSFETs enhance output rating to 20 REN

### Applications

- ☐ Microcontroller or microprocessor controlled high voltage ring generator
- ☐ Set-top/Street box ring generator
- ☐ Pair gain ring generator
- ☐ Wireless local loops
- ☐ Fiber in the loop/to the curb
- ☐ Coax cable loop

### Absolute Maximum Ratings

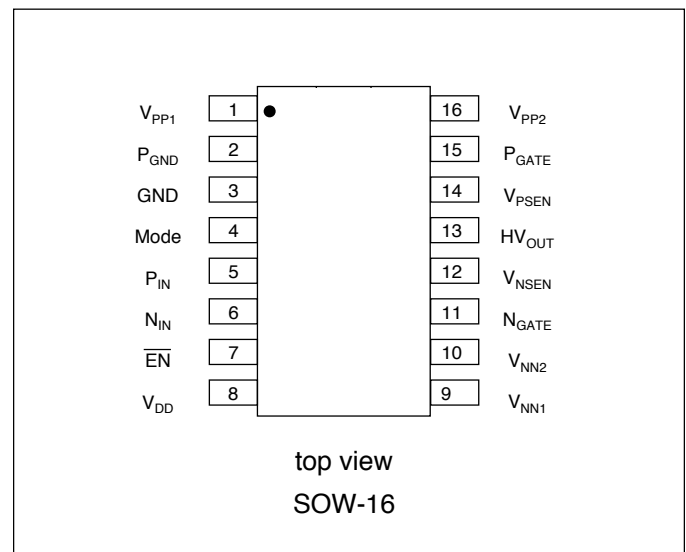
$V_{PP1} - V_{NN1}$ , power supply voltage	+240V
$V_{PP1}$ , positive high voltage supply	+120V
$V_{PP2}$ , positive gate voltage supply	+120V
$V_{NN1}$ , negative high voltage supply	-170V
$V_{NN2}$ , negative gate voltage supply	-170V
$V_{DD}$ , logic supply	+7.5V
Storage temperature	-65°C to +150°C
Power dissipation	800mW

### General Description

The Supertex HV440 is a monolithic integrated circuit capable of generating up to a 70V RMS sine wave output at frequencies of 15Hz to 60Hz with a load of 5 North American RENs. Its output rating can be enhanced to 20 North American RENs with the addition of two Supertex MOSFETs: one N-Channel MOSFET, the TN2524N8 and one P-Channel MOSFET, the TP2522N8.

The high voltage output P- and N-Channel transistors are controlled independently by the logic inputs  $P_{IN}$  and  $N_{IN}$ . Connecting the mode pin to ground will enable the device to be controlled with a single input,  $N_{IN}$ . This adds a 200ns deadband on the control logic to avoid cross conduction on the high voltage output. A logic high on  $N_{IN}$  will turn the high voltage P-Channel on and the N-Channel off. The high voltage outputs have pulse by pulse over current protection set by two external sense resistors. Nominal PWM logic input frequency is 100KHz.

### Pin Configuration



# Electrical Characteristics

(Over operating supply voltage unless otherwise specified,  $T_A = 25^\circ\text{C}$ .)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
$V_{PP1}$	High voltage positive supply	15		110	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$V_{PP2}$	Positive linear regulator output voltage	$V_{PP1} - 9.9$		$V_{PP1} - 19.1$	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$V_{NN1}$	High voltage negative supply	$V_{PP1} - 220$		-110	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$V_{NN2}$	Negative linear regulator output voltage	$V_{NN1} + 5.6$		$V_{NN1} + 10.5$	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$V_{DD}$	Logic supply voltage	4.5		5.5	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$I_{PP1Q}$	$V_{PP1}$ quiescent current		250	400	$\mu\text{A}$	$P_{IN} = N_{IN} = 0V$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$I_{NN1Q}$	$V_{NN1}$ quiescent current		250	550	$\mu\text{A}$	$P_{IN} = N_{IN} = 0V$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$I_{DDQ}$	$V_{DD1}$ quiescent current			10	$\mu\text{A}$	$P_{IN} = N_{IN} = 0V$
$I_{PP1}$	$V_{PP1}$ operating current			1.7	mA	No load, $V_{OUTP}$ and $V_{OUTN}$ switching at 100KHz, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$I_{NN1}$	$V_{NN1}$ operating current			1.9	mA	No load, $V_{OUTP}$ and $V_{OUTN}$ switching at 100KHz, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$I_{DD}$	$V_{DD}$ operating current			1.0	mA	
$I_{IL}$	Mode logic input low current		25		$\mu\text{A}$	Mode = 0V
$V_{IL}$	Logic input low voltage	0		1.0	V	$V_{DD} = 5.0V$
$V_{IH}$	Logic input high voltage	4.0		5.0	V	$V_{DD} = 5.0V$

## High Voltage Output

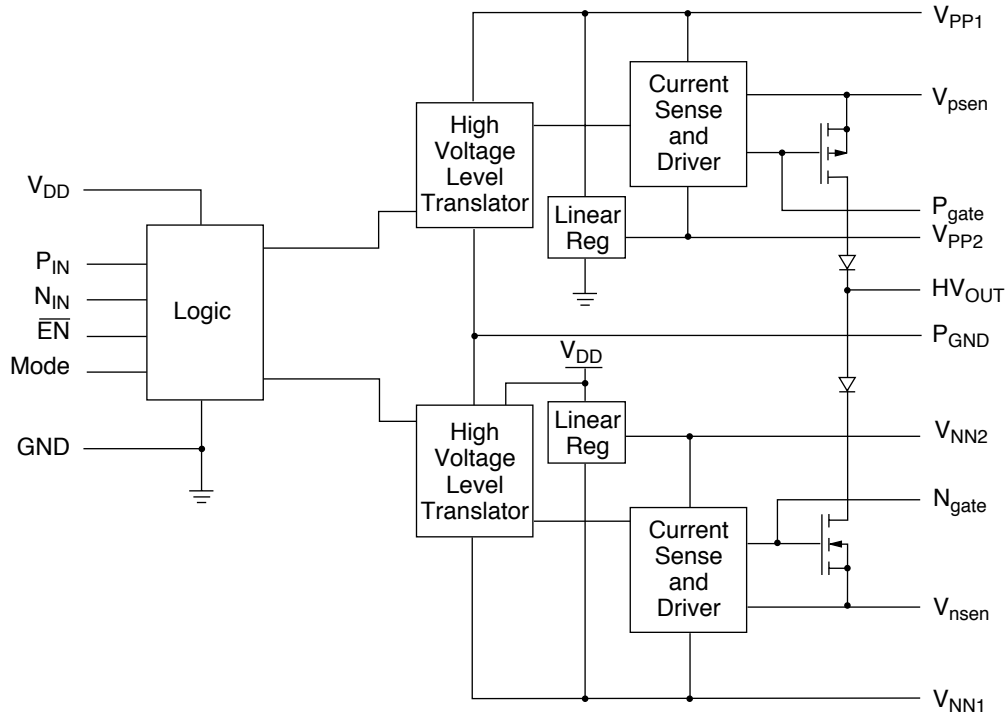
Symbol	Parameters	Min	Typ	Max	Unit	Conditions
$R_{SOURCE}$	$V_{OUTP}$ source resistance		60	80	$\Omega$	$I_{OUT} = 100\text{mA}$
$R_{SINK}$	$V_{OUTP}$ sink resistance		60	80	$\Omega$	$I_{OUT} = -100\text{mA}$
$\Delta R/\Delta T$	Change in source/sink resistance over temperature		0.33		$\Omega/^\circ\text{C}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$t_{d(ON)}$	HV <sub>OUT</sub> delay time		150		ns	$P_{IN}$ = high to low, Mode = high
$t_{rise}$	HV <sub>OUT</sub> rise time			50	ns	$P_{IN}$ = high to low
$t_{d(OFF)}$	HV <sub>OUT</sub> delay time		200		ns	$N_{IN}$ = low to high, Mode = high
$t_{fall}$	HV <sub>OUT</sub> fall time			50	ns	$N_{IN}$ = low to high
$t_{db}$	Logic deadband time			200	ns	Mode = low
$V_{psen}$	HV <sub>OUT</sub> current source sense voltage	$V_{PP1} - 0.75$	$V_{PP1} - 1.00$	$V_{PP1} - 1.25$	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
		$V_{PP1} - 0.67$		$V_{PP1} - 1.31$		
$V_{nsen}$	HV <sub>OUT</sub> current sink sense voltage	$V_{NN1} + 0.75$	$V_{NN1} + 1.00$	$V_{NN1} + 1.25$	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
		$V_{NN1} + 0.65$		$V_{NN1} + 1.33$		
$t_{shortP}$	HV <sub>OUT</sub> off delay time when current source sense is activated			100	ns	
$t_{shortN}$	HV <sub>OUT</sub> off time when current sink sense is activated			100	ns	
$t_{WHOUT}$	Minimum pulse width for HV <sub>OUT</sub> at $V_{PP1}$			500	ns	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
$t_{WLOUT}$	Minimum pulse width for HV <sub>OUT</sub> at $V_{NN1}$			500	ns	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

## Truth Table

$N_{IN}$	$P_{IN}$	Mode	$\overline{EN}$	HV <sub>OUT</sub>
L	L	H	L	$V_{PP1}$
L	H	H	L	High Z
H*	L*	H	L	—
H	H	H	L	$V_{NN1}$
L	X	L	L	$V_{NN1}$
H	X	L	L	$V_{PP1}$
X	X	X	H	High Z

\*This state will short  $V_{PP1}$  to  $V_{NN1}$  and should therefore be avoided.

## Block Diagram



## Pin Description

$V_{PP1}$	Positive high voltage supply.
$V_{PP2}$	Positive gate voltage supply. Generated by an internal linear regulator. A 0.1 $\mu$ F capacitor should be connected between $V_{PP2}$ and $V_{PP1}$ .
$V_{NN1}$	Negative high voltage supply.
$V_{NN2}$	Negative gate voltage supply. Generated by an internal linear regulator. A 0.1 $\mu$ F capacitor should be connected between $V_{NN2}$ and $V_{NN1}$ .
$V_{DD}$	Logic supply voltage.
GND	Low voltage ground.
PGND	High voltage power ground.
$P_{IN}$	Logic control input. When mode is high, logic input high turns OFF output high voltage P-Channel.
$N_{IN}$	Logic control input. When mode is high, logic input high turns ON output high voltage N-Channel.
EN	Logic enable bar input. Logic low enables IC.
Mode	Logic mode input. Logic low activates 200nsec deadband. When mode is low, $N_{IN}$ turns on and off the high voltage N- and P-Channels. Pin is not used and should be connected to $V_{DD}$ or ground.
HV <sub>OUT</sub>	High voltage output. Voltage swings from $V_{PP1}$ to $V_{NN1}$ .
$V_{psen}$	Pulse by pulse over current sensing for P-Channel MOSFET.
$V_{nsen}$	Pulse by pulse over current sensing for N-Channel MOSFET.
$P_{gate}$	Gate drive for external P-channel MOSFET.
$N_{gate}$	Gate drive for external N-channel MOSFET.

# Typical Application Circuit

