

32-Channel Serial To Parallel Converter with P-Channel Open Drain Outputs

Ordering Information

Device	Recommended Operating V _{PP} Max	Package Options		
		44 J-Lead Quad Plastic Chip Carrier	44 Quad Plastic Gullwing	Die
HV4530	-300	HV4530PJ	HV4530PG	HV4530X
HV4630	-300	HV4630PJ	HV4630PG	HV4630X

Features

- ❑ Processed with HVCMOS Technology
- ❑ Output voltages to -300V
- ❑ Source current minimum 60 mA
- ❑ Shift register speed 8 MHz
- ❑ Polarity and blanking inputs
- ❑ CMOS compatible inputs
- ❑ Forward and reverse shifting options
- ❑ 44-lead plastic and ceramic surface mount packages
- ❑ Hi-Rel processing available
- ❑ Can be used with the HV55 and HV56 to provide 300V push pull operation

Absolute Maximum Ratings¹

Supply voltage, V _{DD}	+0.5V to -16V	
Off state output voltage	HV4630	+0.5V to -315V
	HV4622	+0.5V to -240V
Logic input levels	+0.5V to V _{DD} - 0.3V	
Ground current ²	1.5A	
Continuous total power dissipation ³	1200mW	
Operating temperature range	-40°C to +85°C	
Storage temperature range	-65°C to +150°C	
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C	

Notes:

1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.

General Description

The HV45 and HV46 are low-voltage serial to high-voltage parallel converters with P-Channel open drain outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current source capabilities such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

These devices consist of a 32-bit shift register, 32 data latches, and control logic to perform polarity and blanking functions. Data is shifted through the shift register on the logic high-to-low transition of the clock. The HV45 shifts in the counterclockwise direction when viewed from the top of the package and the HV46 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. The data in the shift register is latched when the latch enable pin is brought to logic high and then returned to ground. If the latch enable pin is held high, the latch becomes transparent and the shift register data is directly reflected in the outputs.

For applications requiring active pull down as well as pull up, the HV45 and HV46 can be paired with the HV55 and HV56 devices, respectively.

Electrical Characteristics¹ (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-15	mA	$f_{CLK} = 8 \text{ MHz}$ $F_{DATA} = 4 \text{ MHz}$
I_{DDQ}	Quiescent V_{DD} supply current		-100	μA	$V_{IN} = V_{SS}$ or V_{DD}
$I_{O(OFF)}$	Off state output current		-100	μA	All SWS parallel
I_{IH}	High-level logic input current		-1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		+1	μA	$V_{IL} = V_{SS}$
V_{OH}	High-level output data out	$V_{DD} + 1.0\text{V}$		V	$I_{Dout} = -100\mu\text{A}$
V_{OL}	Low-level output voltage	HV _{OUT}	-30.0	V	$I_{HVout} = -60\text{mA}$
		Data out	-1.0	V	$I_{Dout} = -100\mu\text{A}$
V_{OC}	HV _{OUT} clamp voltage		+1.5	V	$I_{OL} = +60\text{mA}$

AC Characteristics ($V_{DD} = -12\text{V}$, $T_C = 25^\circ\text{C}$)

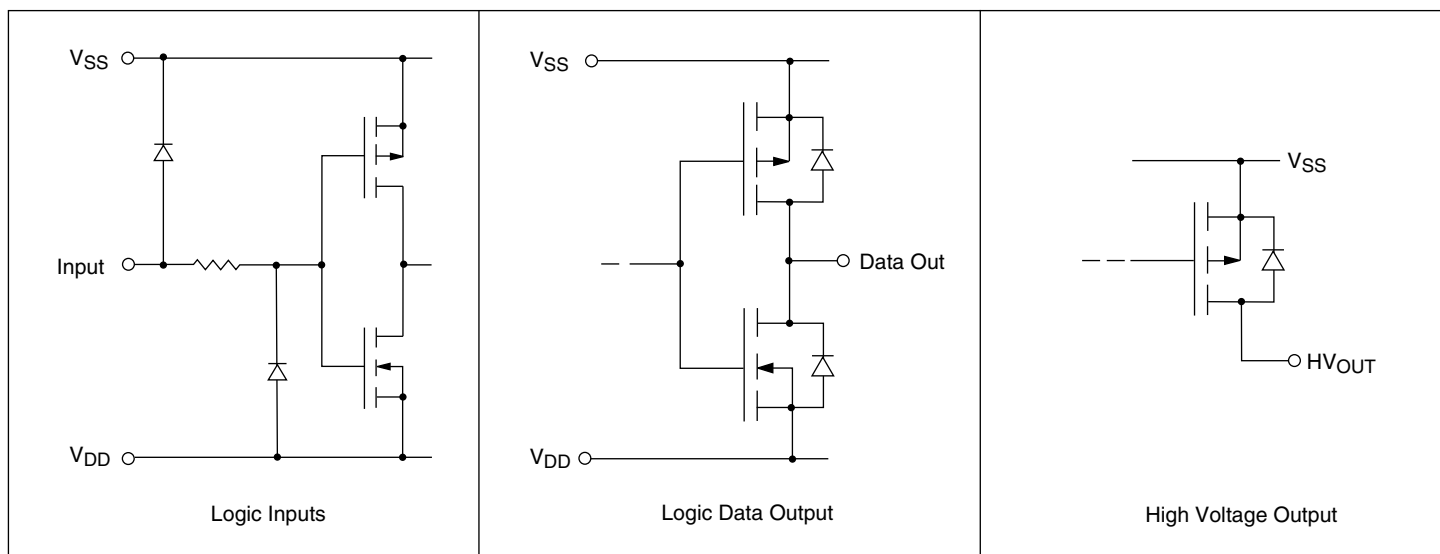
Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WH}/t_{WL}	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	50		ns	
t_H	Data hold time after clock rises	20		ns	
t_{ON}	Turn ON time, HV _{OUT} from enable		400	ns	$R_L = 10\text{K}$ to $V_{OO} \text{ MAX}$
t_{DHL}	Delay time clock to data high to low		100	ns	$C_L = 15\text{pF}$
t_{DLH}	Delay time clock to data low to high		100	ns	$C_L = 15\text{pF}$
t_{DLE}	Delay time clock to LE low to high	50		ns	
t_{WLE}	Width of LE pulse	50		ns	
t_{SLE}	LE set-up time before clock falls	50		ns	

Recommended Operating Conditions

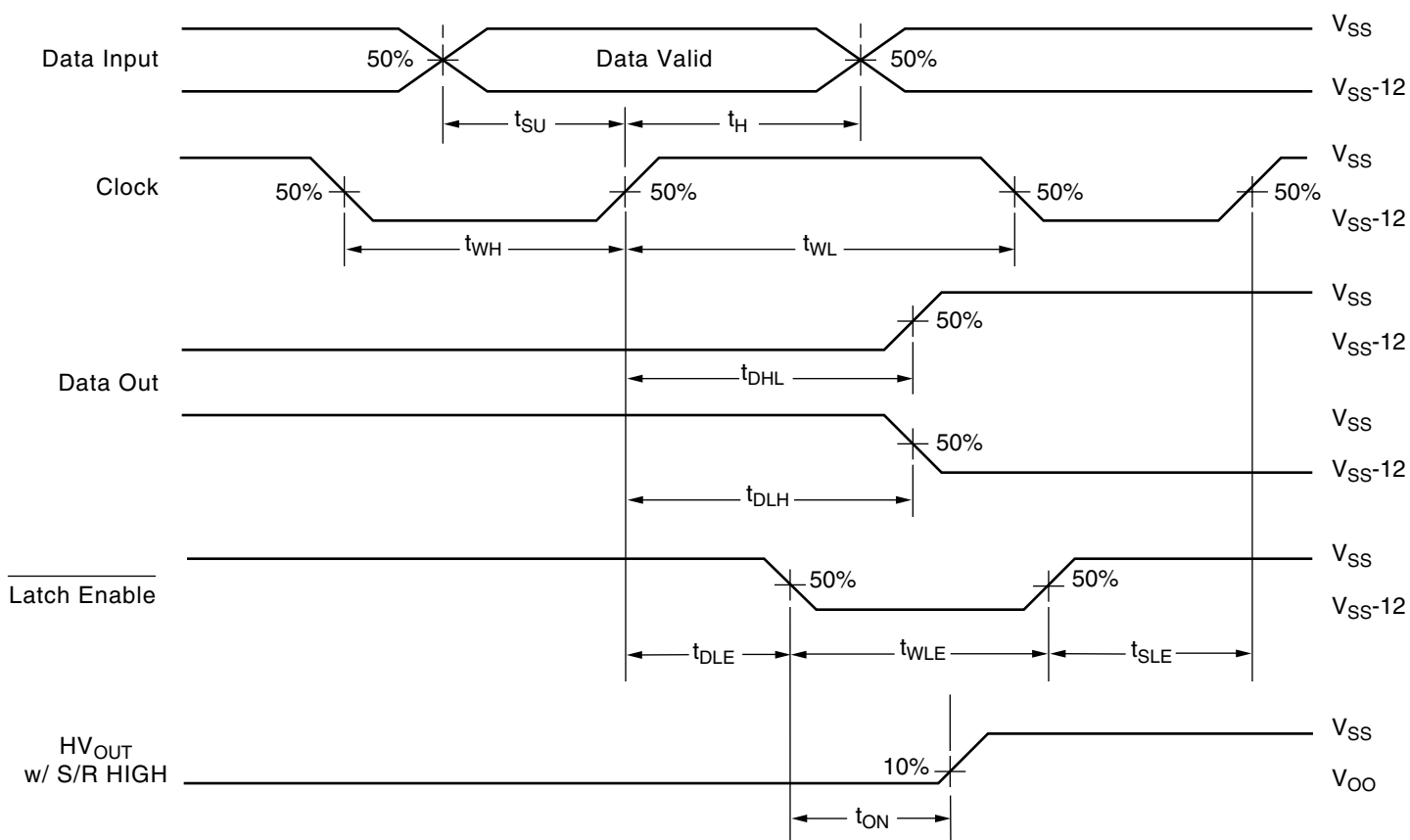
Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	-10.8	-13.2	V
HV _{OUT}	Output off voltage	+0.3	-300	V
V_{IH}	High-level input voltage (LOGIC "1")	$V_{DD} + 2\text{V}$	V_{DD}	V
V_{IL}	Low-level input voltage (LOGIC "0")	0	-2.0	V
f_{CLK}	Clock frequency		8	MHz
T_A	Operating free-air temperature	-40	+85	$^\circ\text{C}$

Note: All voltages are referenced to V_{SS} .

Input and Output Equivalent Circuits



Switching Waveforms





* = dependent on previous stage's state before the last CLK high-to-low transition or last $\overline{\text{LE}}$ high.

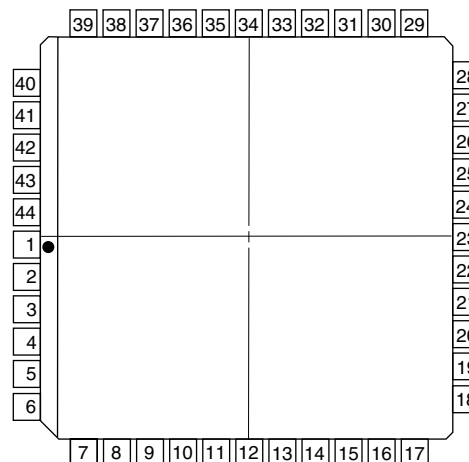
Pin Configurations

Package Outline

HV45

44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV _{OUT} 17	23	Clock
2	HV _{OUT} 18	24	V _{SS}
3	HV _{OUT} 19	25	V _{DD}
4	HV _{OUT} 20	26	Latch Enable
5	HV _{OUT} 21	27	Data In
6	HV _{OUT} 22	28	Blanking
7	HV _{OUT} 23	29	HV _{OUT} 1
8	HV _{OUT} 24	30	HV _{OUT} 2
9	HV _{OUT} 25	31	HV _{OUT} 3
10	HV _{OUT} 26	32	HV _{OUT} 4
11	HV _{OUT} 27	33	HV _{OUT} 5
12	HV _{OUT} 28	34	HV _{OUT} 6
13	HV _{OUT} 29	35	HV _{OUT} 7
14	HV _{OUT} 30	36	HV _{OUT} 8
15	HV _{OUT} 31	37	HV _{OUT} 9
16	HV _{OUT} 32	38	HV _{OUT} 10
17	N/C	39	HV _{OUT} 11
18	Data Out	40	HV _{OUT} 12
19	N/C	41	HV _{OUT} 13
20	N/C	42	HV _{OUT} 14
21	N/C	43	HV _{OUT} 15
22	Polarity	44	HV _{OUT} 16



top view

44-pin J-Lead Package

HV46

44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV _{OUT} 16	23	Clock
2	HV _{OUT} 15	24	V _{SS}
3	HV _{OUT} 14	25	V _{DD}
4	HV _{OUT} 13	26	Latch Enable
5	HV _{OUT} 12	27	Data In
6	HV _{OUT} 11	28	Blanking
7	HV _{OUT} 10	29	HV _{OUT} 32
8	HV _{OUT} 9	30	HV _{OUT} 31
9	HV _{OUT} 8	31	HV _{OUT} 30
10	HV _{OUT} 7	32	HV _{OUT} 29
11	HV _{OUT} 6	33	HV _{OUT} 28
12	HV _{OUT} 5	34	HV _{OUT} 27
13	HV _{OUT} 4	35	HV _{OUT} 26
14	HV _{OUT} 3	36	HV _{OUT} 25
15	HV _{OUT} 2	37	HV _{OUT} 24
16	HV _{OUT} 1	38	HV _{OUT} 23
17	N/C	39	HV _{OUT} 22
18	Data Out	40	HV _{OUT} 21
19	N/C	41	HV _{OUT} 20
20	N/C	42	HV _{OUT} 19
21	N/C	43	HV _{OUT} 18
22	Polarity	44	HV _{OUT} 17

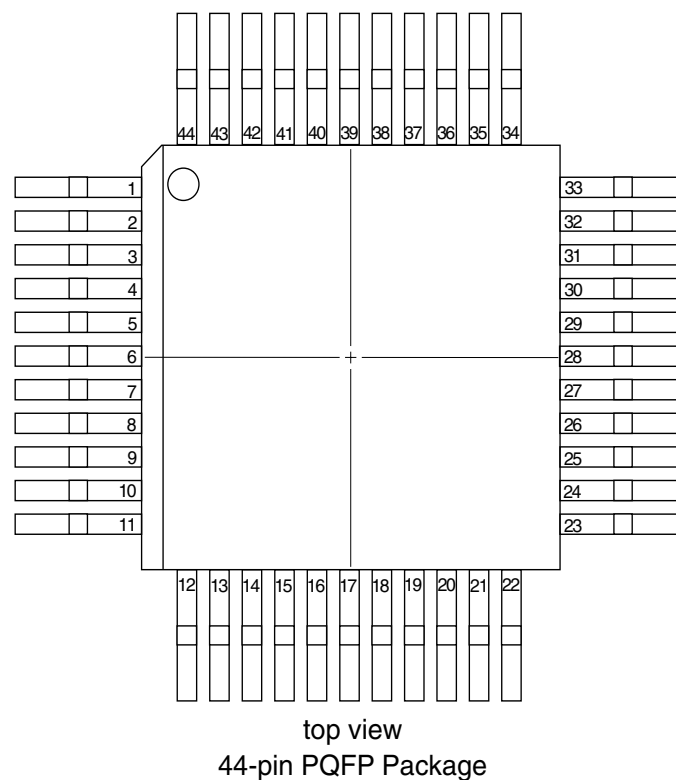
Pin Configurations

HV45

44-Pin Plastic Gullwing (QFP) Package

Pin	Function	Pin	Function
1	HV _{OUT} 12	23	Data Out
2	HV _{OUT} 13	24	N/C
3	HV _{OUT} 14	25	N/C
4	HV _{OUT} 15	26	N/C
5	HV _{OUT} 16	27	Polarity
6	HV _{OUT} 17	28	Clock
7	HV _{OUT} 18	29	V _{SS}
8	HV _{OUT} 19	30	V _{DD}
9	HV _{OUT} 20	31	Latch Enable
10	HV _{OUT} 21	32	Data In
11	HV _{OUT} 22	33	Blanking
12	HV _{OUT} 23	34	HV _{OUT} 1
13	HV _{OUT} 24	35	HV _{OUT} 2
14	HV _{OUT} 25	36	HV _{OUT} 3
15	HV _{OUT} 26	37	HV _{OUT} 4
16	HV _{OUT} 27	38	HV _{OUT} 5
17	HV _{OUT} 28	39	HV _{OUT} 6
18	HV _{OUT} 29	40	HV _{OUT} 7
19	HV _{OUT} 30	41	HV _{OUT} 8
20	HV _{OUT} 31	42	HV _{OUT} 9
21	HV _{OUT} 32	43	HV _{OUT} 10
22	N/C	44	HV _{OUT} 11

Package Outline



HV46

44-Pin Plastic Gullwing (QFP) Package

Pin	Function	Pin	Function
1	HV _{OUT} 21	23	Data Out
2	HV _{OUT} 20	24	N/C
3	HV _{OUT} 19	25	N/C
4	HV _{OUT} 18	26	N/C
5	HV _{OUT} 17	27	Polarity
6	HV _{OUT} 16	28	Clock
7	HV _{OUT} 15	29	V _{SS}
8	HV _{OUT} 14	30	V _{DD}
9	HV _{OUT} 13	31	Latch Enable
10	HV _{OUT} 12	32	Data In
11	HV _{OUT} 11	33	Blanking
12	HV _{OUT} 10	34	HV _{OUT} 32
13	HV _{OUT} 9	35	HV _{OUT} 31
14	HV _{OUT} 8	36	HV _{OUT} 30
15	HV _{OUT} 7	37	HV _{OUT} 29
16	HV _{OUT} 6	38	HV _{OUT} 28
17	HV _{OUT} 5	39	HV _{OUT} 27
18	HV _{OUT} 4	40	HV _{OUT} 26
19	HV _{OUT} 3	41	HV _{OUT} 25
20	HV _{OUT} 2	42	HV _{OUT} 24
21	HV _{OUT} 1	43	HV _{OUT} 23
22	N/C	44	HV _{OUT} 22