

## 32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

### Ordering Information

Device	Package Options				
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	44 Lead Quad Plastic Gullwing	Die	44 J-Lead Quad Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV5308	HV5308DJ	HV5308PJ	HV5308PG	HV5308X	RBHV5308DJ
HV5408	HV5408DJ	HV5408PJ	HV5408PG	HV5408X	RBHV5408DJ

\* For Hi-Rel process flows, please refer to page 5-3 in the Databook.

### Features

- ☐ Processed with HVCMOS® technology
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to  $V_{PP}$  allows efficient power recovery

### Absolute Maximum Ratings<sup>1</sup>

Supply voltage, $V_{DD}$ <sup>2</sup>	-0.5V to +16V
Supply voltage, $V_{PP}$	-0.5V to +90V
Logic input levels <sup>2</sup>	-0.5 to $V_{DD} + 0.5V$
Ground current <sup>3</sup>	1.5A
Continuous total power dissipation <sup>4</sup>	Plastic 1200mW Ceramic 1500mW
Operating temperature range	Plastic -40°C to +85°C Ceramic -55°C to 125°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

#### Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.

12/13/01

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### General Description

The HV53 and HV54 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. Q1 is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. The HV54 shifts in the counterclockwise direction when viewed from the top of the package and the HV53 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the  $\overline{LE}$  (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the  $\overline{LE}$  input is high. The data in the latch is retained when  $\overline{LE}$  is low.

# Electrical Characteristics ( $V_{PP} = 60V$ , $V_{DD} = 12V$ , $T_A = 25^\circ C$ )

## DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
$I_{PP}$	$V_{PP}$ Supply Current		0.5	mA	HVoutputs HIGH to LOW
$I_{DDQ}$	$I_{DD}$ Supply Current (Quiescent)		100	$\mu A$	All inputs = $V_{DD}$ or GND
$I_{DD}$	$I_{DD}$ Supply Current (Operating)		15	mA	$V_{DD} = V_{DD} \text{ max}$ , $f_{CLK} = 8 \text{ MHz}$
$V_{OH} \text{ (Data)}$	Shift Register Output Voltage	10.5		V	$I_O = 100\mu A$
$V_{OL} \text{ (Data)}$	Shift Register Output Voltage		1	V	$I_O = 100\mu A$
$I_{IH}$	Current Leakage, any input		1	$\mu A$	$V_{IN} = V_{DD}$
$I_{IL}$	Current Leakage, any input		-1	$\mu A$	$V_{IN} = 0$
$V_{OC}$	HV Output Clamp Diode Voltage		-1.5	V	$I_{OL} = -100mA$
$V_{OH}$	HV Output when Sourcing	52		V	$I_{OH} = -20mA$ , -40 to $85^\circ C$
$V_{OL}$	HV Output when Sinking		8	V	$I_{OL} = 20mA$ , -40 to $85^\circ C$
$V_{OH}$	HV Output when Sourcing	52		V	$I_{OH} = -15mA$ , -55 to $125^\circ C$
$V_{OL}$	HV Output when Sinking		8	V	$I_{OL} = 15mA$ , -55 to $125^\circ C$

## AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
$f_{CLK}$	Clock Frequency		8	MHz	
$t_{WL}$ or $t_{WH}$	Clock width, HIGH or LOW	62		ns	
$t_{SU}$	Setup time before CLK rises	25		ns	
$t_H$	Hold time after CLK rises	10		ns	
$t_{DLH} \text{ (Data)}$	Data Output Delay after L to H CLK		110	ns	$C_L = 15pF$
$t_{DHL} \text{ (Data)}$	Data Output Delay after H to L CLK		110	ns	$C_L = 15pF$
$t_{DLE}$	$\overline{LE}$ Delay after L to H CLK	50		ns	
$t_{WLE}$	Width of $\overline{LE}$ Pulse	50		ns	
$t_{SLE}$	$\overline{LE}$ Setup Time before L to H CLK	50		ns	
$t_{ON}$	Delay from $\overline{LE}$ to $HV_{OUT}$ , L to H		500	ns	
$t_{OFF}$	Delay from $\overline{LE}$ to $HV_{OUT}$ , H to L		500	ns	

## Recommended Operating Conditions

(over  $-40$  to  $85^\circ C$  for plastic and  $-55^\circ C$  to  $125^\circ C$  for ceramic)

Symbol	Parameter	Min	Max	Units
$V_{DD}$	Logic Voltage Supply	10.8	13.2	V
$V_{PP}$	High Voltage Supply	8.0	80	V
$V_{IH}$	Input HIGH Voltage	$V_{DD}-2$	$V_{DD}$	V
$V_{IL}$	Input LOW Voltage	0	2	V
$f_{CLK}$	Clock Frequency	0	8	MHz

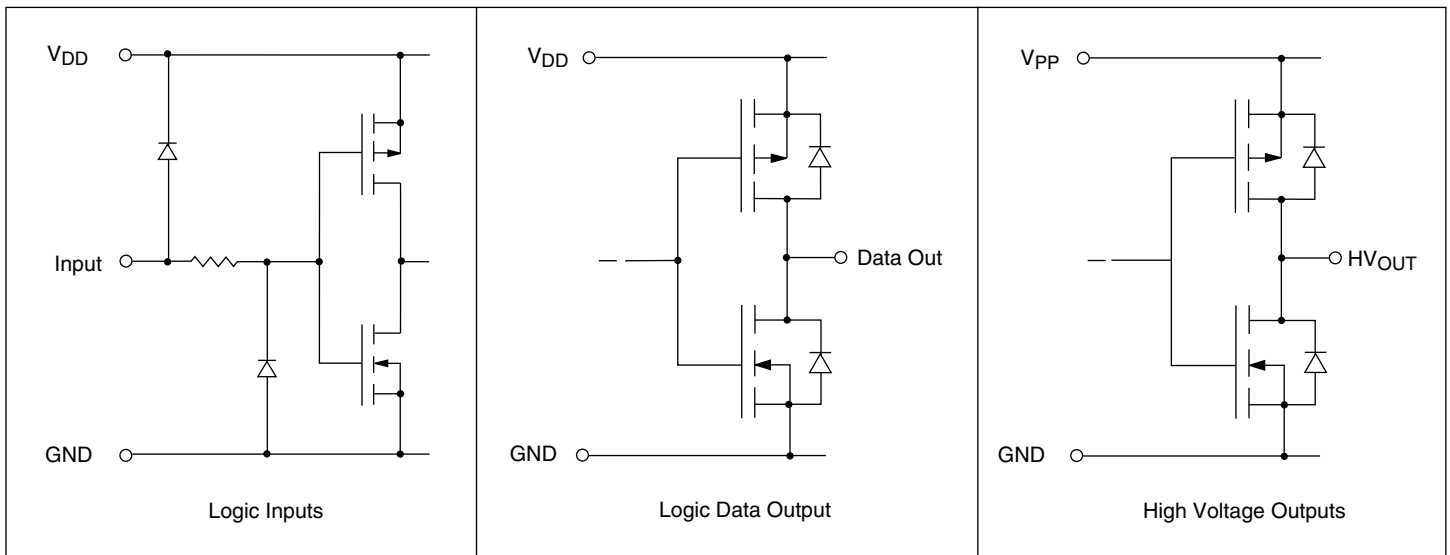
### Note:

Power-up sequence should be the following:

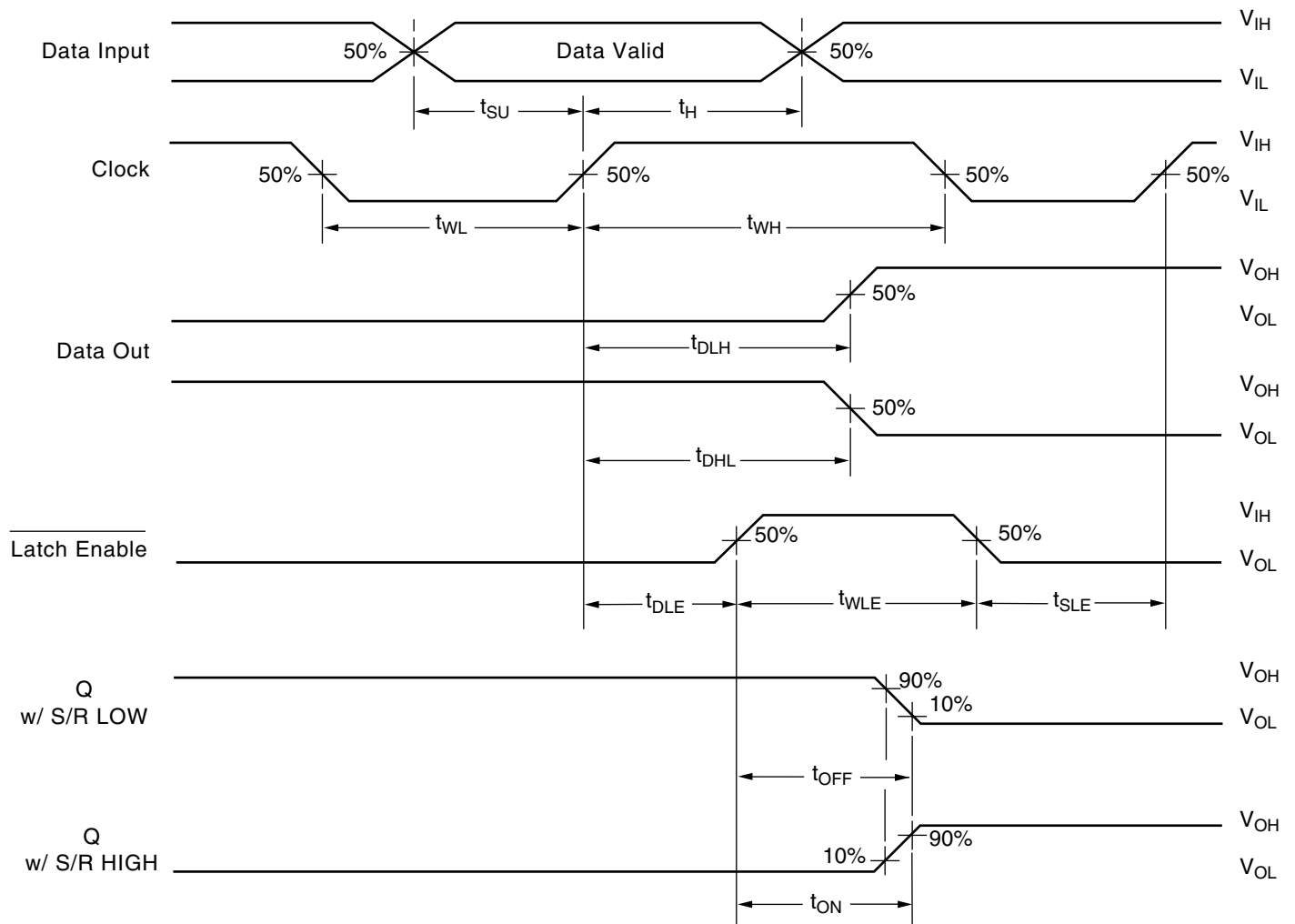
1. Connect ground.
2. Apply  $V_{DD}$ .
3. Set all inputs (Data, CLK,  $\overline{LE}$ , etc.) to a known state.
4. Apply  $V_{PP}$ .
5. The  $V_{PP}$  should not fall below  $V_{DD}$  or float during operation.

Power-down sequence should be the reverse of the above.

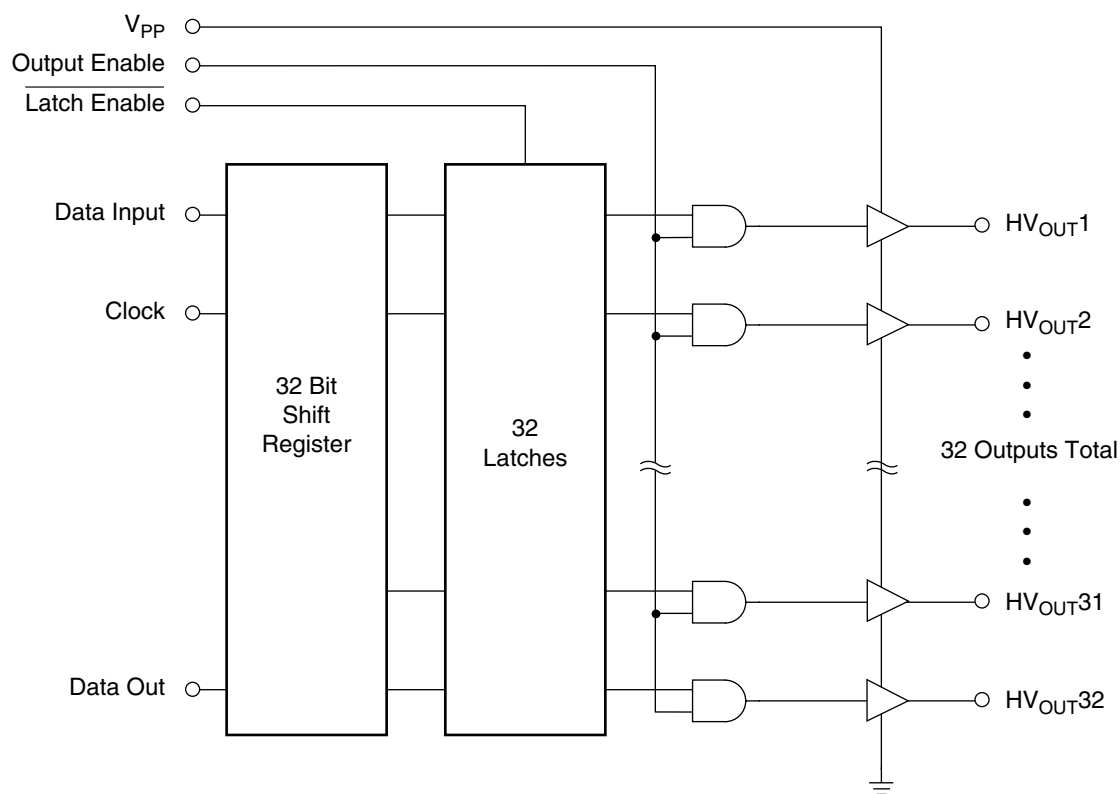
## Input and Output Equivalent Circuits



## Switching Waveforms



## Functional Block Diagram



## Function Tables

Data Input	CLK*	Data Output
H		H
L		L
X	No	No Change

\* = LOW-to-HIGH level transition

Data Input	$\overline{LE}$	OE	HV Output
X	X	L	All HV <sub>OUT</sub> = LOW
X	L	H	Previous Latched Data
H	H	H	H
L	H	H	L

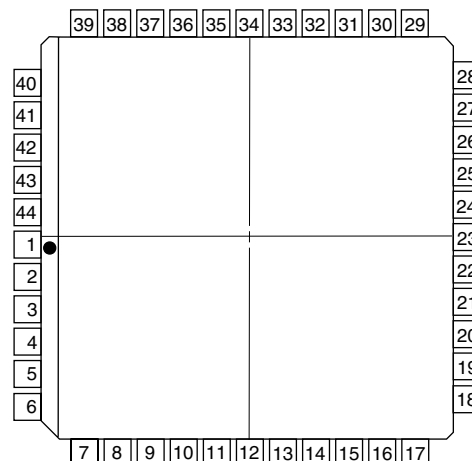
## Pin Configuration

### HV53

#### 44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 17	23	GND
2	HV <sub>OUT</sub> 16	24	V <sub>PP</sub>
3	HV <sub>OUT</sub> 15	25	V <sub>DD</sub>
4	HV <sub>OUT</sub> 14	26	Latch Enable
5	HV <sub>OUT</sub> 13	27	Data In
6	HV <sub>OUT</sub> 12	28	Output Enable
7	HV <sub>OUT</sub> 11	29	N/C
8	HV <sub>OUT</sub> 10	30	HV <sub>OUT</sub> 32
9	HV <sub>OUT</sub> 9	31	HV <sub>OUT</sub> 31
10	HV <sub>OUT</sub> 8	32	HV <sub>OUT</sub> 30
11	HV <sub>OUT</sub> 7	33	HV <sub>OUT</sub> 29
12	HV <sub>OUT</sub> 6	34	HV <sub>OUT</sub> 28
13	HV <sub>OUT</sub> 5	35	HV <sub>OUT</sub> 27
14	HV <sub>OUT</sub> 4	36	HV <sub>OUT</sub> 26
15	HV <sub>OUT</sub> 3	37	HV <sub>OUT</sub> 25
16	HV <sub>OUT</sub> 2	38	HV <sub>OUT</sub> 24
17	HV <sub>OUT</sub> 1	39	HV <sub>OUT</sub> 23
18	Data Out	40	HV <sub>OUT</sub> 22
19	N/C	41	HV <sub>OUT</sub> 21
20	N/C	42	HV <sub>OUT</sub> 20
21	N/C	43	HV <sub>OUT</sub> 19
22	Clock	44	HV <sub>OUT</sub> 18

## Package Outline



top view

44-pin J-Lead Package

### HV54

#### 44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 16	23	GND
2	HV <sub>OUT</sub> 17	24	V <sub>PP</sub>
3	HV <sub>OUT</sub> 18	25	V <sub>DD</sub>
4	HV <sub>OUT</sub> 19	26	Latch Enable
5	HV <sub>OUT</sub> 20	27	Data In
6	HV <sub>OUT</sub> 21	28	Output Enable
7	HV <sub>OUT</sub> 22	29	N/C
8	HV <sub>OUT</sub> 23	30	HV <sub>OUT</sub> 1
9	HV <sub>OUT</sub> 24	31	HV <sub>OUT</sub> 2
10	HV <sub>OUT</sub> 25	32	HV <sub>OUT</sub> 3
11	HV <sub>OUT</sub> 26	33	HV <sub>OUT</sub> 4
12	HV <sub>OUT</sub> 27	34	HV <sub>OUT</sub> 5
13	HV <sub>OUT</sub> 28	35	HV <sub>OUT</sub> 6
14	HV <sub>OUT</sub> 29	36	HV <sub>OUT</sub> 7
15	HV <sub>OUT</sub> 30	37	HV <sub>OUT</sub> 8
16	HV <sub>OUT</sub> 31	38	HV <sub>OUT</sub> 9
17	HV <sub>OUT</sub> 32	39	HV <sub>OUT</sub> 10
18	Data Out	40	HV <sub>OUT</sub> 11
19	N/C	41	HV <sub>OUT</sub> 12
20	N/C	42	HV <sub>OUT</sub> 13
21	N/C	43	HV <sub>OUT</sub> 14
22	Clock	44	HV <sub>OUT</sub> 15

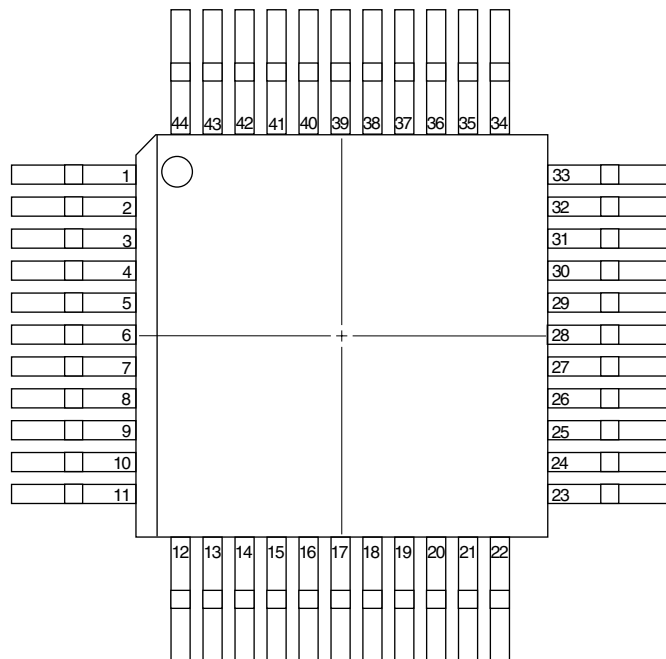
## Pin Configuration

### HV53

#### 44 Pin Quad Plastic Gullwing Package

Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 22	23	Data Out
2	HV <sub>OUT</sub> 21	24	N/C
3	HV <sub>OUT</sub> 20	25	N/C
4	HV <sub>OUT</sub> 19	26	N/C
5	HV <sub>OUT</sub> 18	27	Clock
6	HV <sub>OUT</sub> 17	28	GND
7	HV <sub>OUT</sub> 16	29	V <sub>PP</sub>
8	HV <sub>OUT</sub> 15	30	V <sub>DD</sub>
9	HV <sub>OUT</sub> 14	31	Latch Enable
10	HV <sub>OUT</sub> 13	32	Data In
11	HV <sub>OUT</sub> 12	33	Output Enable
12	HV <sub>OUT</sub> 11	34	N/C
13	HV <sub>OUT</sub> 10	35	HV <sub>OUT</sub> 32
14	HV <sub>OUT</sub> 9	36	HV <sub>OUT</sub> 31
15	HV <sub>OUT</sub> 8	37	HV <sub>OUT</sub> 30
16	HV <sub>OUT</sub> 7	38	HV <sub>OUT</sub> 29
17	HV <sub>OUT</sub> 6	39	HV <sub>OUT</sub> 28
18	HV <sub>OUT</sub> 5	40	HV <sub>OUT</sub> 27
19	HV <sub>OUT</sub> 4	41	HV <sub>OUT</sub> 26
20	HV <sub>OUT</sub> 3	42	HV <sub>OUT</sub> 25
21	HV <sub>OUT</sub> 2	43	HV <sub>OUT</sub> 24
22	HV <sub>OUT</sub> 1	44	HV <sub>OUT</sub> 23

## Package Outline



top view  
44-pin Quad Plastic Gullwing Package

### HV54

#### 44 Pin Quad Plastic Gullwing Package

Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 11	23	Data Out
2	HV <sub>OUT</sub> 12	24	N/C
3	HV <sub>OUT</sub> 13	25	N/C
4	HV <sub>OUT</sub> 14	26	N/C
5	HV <sub>OUT</sub> 15	27	Clock
6	HV <sub>OUT</sub> 16	28	GND
7	HV <sub>OUT</sub> 17	29	V <sub>PP</sub>
8	HV <sub>OUT</sub> 18	30	V <sub>DD</sub>
9	HV <sub>OUT</sub> 19	31	Latch Enable
10	HV <sub>OUT</sub> 20	32	Data In
11	HV <sub>OUT</sub> 21	33	Output Enable
12	HV <sub>OUT</sub> 22	34	N/C
13	HV <sub>OUT</sub> 23	35	HV <sub>OUT</sub> 1
14	HV <sub>OUT</sub> 24	36	HV <sub>OUT</sub> 2
15	HV <sub>OUT</sub> 25	37	HV <sub>OUT</sub> 3
16	HV <sub>OUT</sub> 26	38	HV <sub>OUT</sub> 4
17	HV <sub>OUT</sub> 27	39	HV <sub>OUT</sub> 5
18	HV <sub>OUT</sub> 28	40	HV <sub>OUT</sub> 6
19	HV <sub>OUT</sub> 29	41	HV <sub>OUT</sub> 7
20	HV <sub>OUT</sub> 30	42	HV <sub>OUT</sub> 8
21	HV <sub>OUT</sub> 31	43	HV <sub>OUT</sub> 9
22	HV <sub>OUT</sub> 32	44	HV <sub>OUT</sub> 10