



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

$BV_{DSS} /$ $BV_{DGS}$	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	Die†
60V	3.0Ω	2A	2.0V	TN0106N3	—
100V	3.0Ω	2A	2.0V	TN0110N3	TN0110ND

† MIL visual screening available

### Features

- ☐ Low threshold — 2.0V max.
- ☐ High input impedance
- ☐ Low input capacitance — 50pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

### Applications

- ☐ Logic level interfaces – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drives
- ☐ Analog switches
- ☐ General purpose line drivers
- ☐ Telecom switches

### Absolute Maximum Ratings

Drain-to-Source Voltage	$BV_{DSS}$
Drain-to-Gate Voltage	$BV_{DGS}$
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

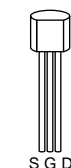
\* Distance of 1.6 mm from case for 10 seconds.

### Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



TO-92

Note: See Package Outline section for dimensions.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-92	0.5A	2.0A	1.0W	125	170	0.5A	2.0A

\*  $I_D$  (continuous) is limited by max rated  $T_J$ .

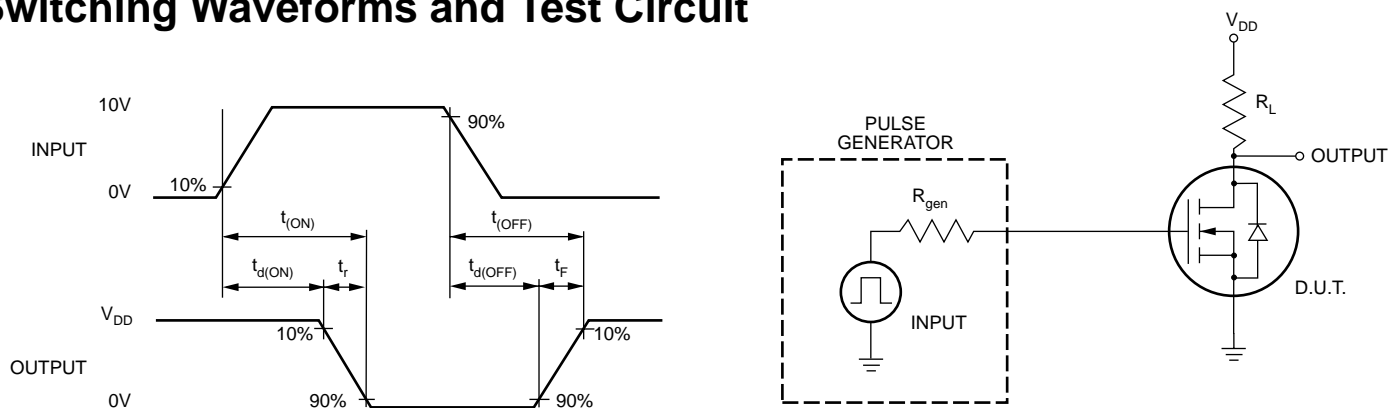
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	TN0110	100			V	$I_D = 1\text{mA}$ , $V_{GS} = 0\text{V}$
		TN0106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		2.0	V	$V_{GS} = V_{DS}$ , $I_D = 0.5\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.2	-5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}$ , $I_D = 1.0\text{mA}$
$I_{GSS}$	Gate Body Leakage				100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current				10	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = \text{Max Rating}$
					500		$V_{GS} = 0\text{V}$ , $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		0.75	1.4		A	$V_{GS} = 5\text{V}$ , $V_{DS} = 25\text{V}$
			2.0	3.4			$V_{GS} = 10\text{V}$ , $V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	4.5	$\Omega$	$V_{GS} = 4.5\text{V}$ , $I_D = 250\text{mA}$
				1.6	3.0		$V_{GS} = 10\text{V}$ , $I_D = 500\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1.1	%/ $^\circ\text{C}$	$I_D = 0.5\text{A}$ , $V_{GS} = 10\text{V}$
$G_{FS}$	Forward Transconductance		225	400		mS	$V_{DS} = 25\text{V}$ , $I_D = 500\text{mA}$
$C_{ISS}$	Input Capacitance			50	60	pF	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ $f = 1\text{MHz}$
$C_{OSS}$	Common Source Output Capacitance			25	35		
$C_{RSS}$	Reverse Transfer Capacitance			4.0	8.0		
$t_{d(ON)}$	Turn-ON Delay Time			2.0	5.0	ns	$V_{DD} = 25\text{V}$ $I_D = 1.0\text{A}$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			3.0	5.0		
$t_{d(OFF)}$	Turn-OFF Delay Time			6.0	7.0		
$t_f$	Fall Time			3.0	6.0		
$V_{SD}$	Diode Forward Voltage Drop			1.0	1.5	V	$I_{SD} = 0.5\text{A}$ , $V_{GS} = 0\text{V}$
$t_{rr}$	Reverse Recovery Time			400		ns	$I_{SD} = 0.5\text{A}$ , $V_{GS} = 0\text{V}$

### Notes:

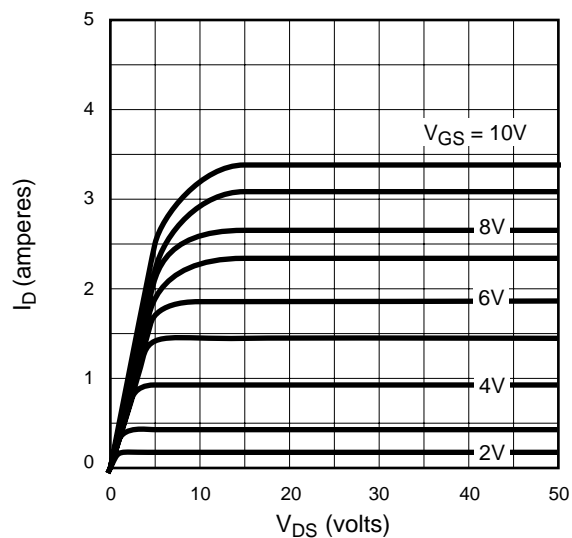
1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

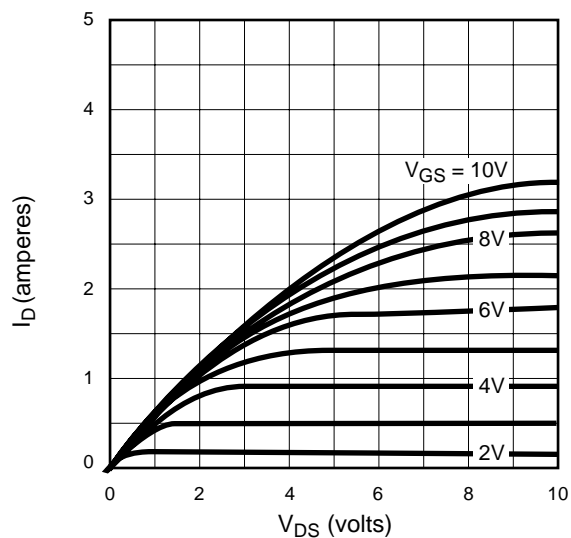


# Typical Performance Curves

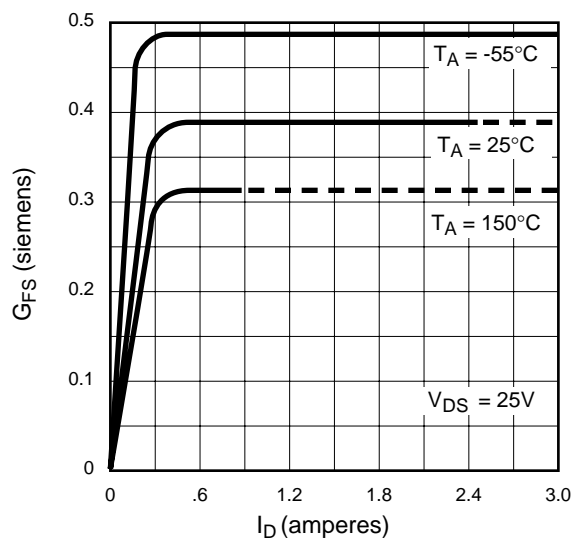
Output Characteristics



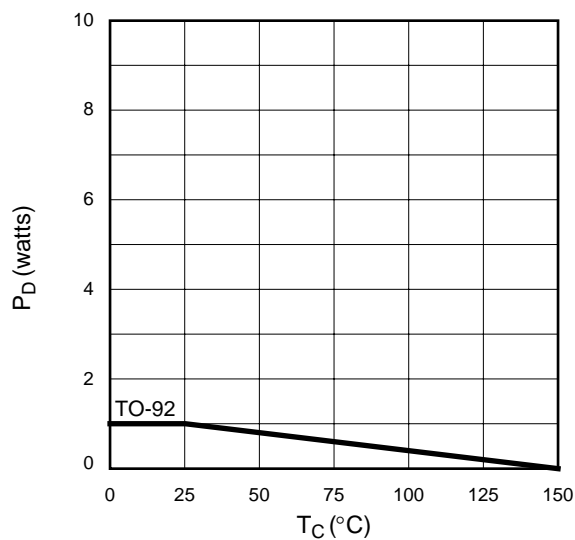
Saturation Characteristics



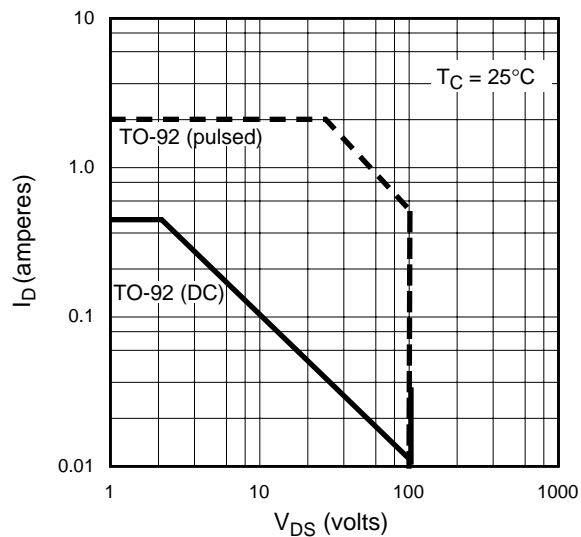
Transconductance vs. Drain Current



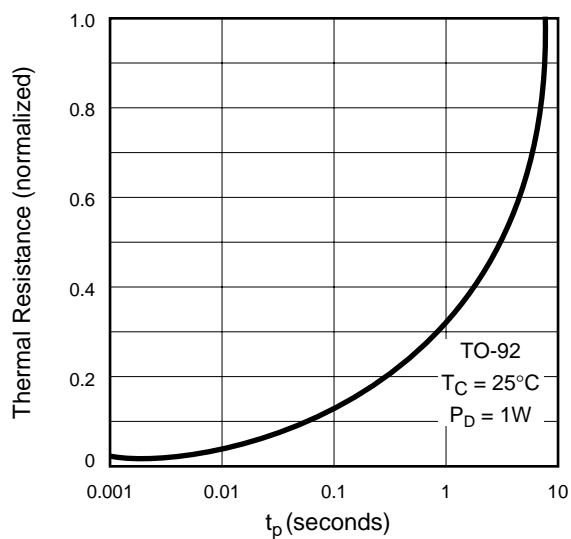
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

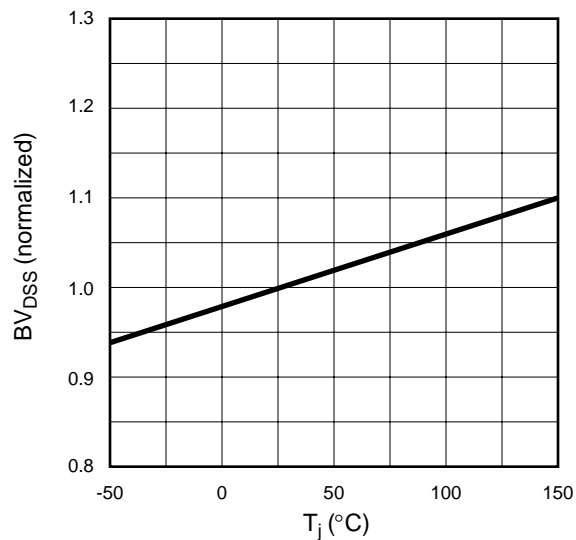


Thermal Response Characteristics

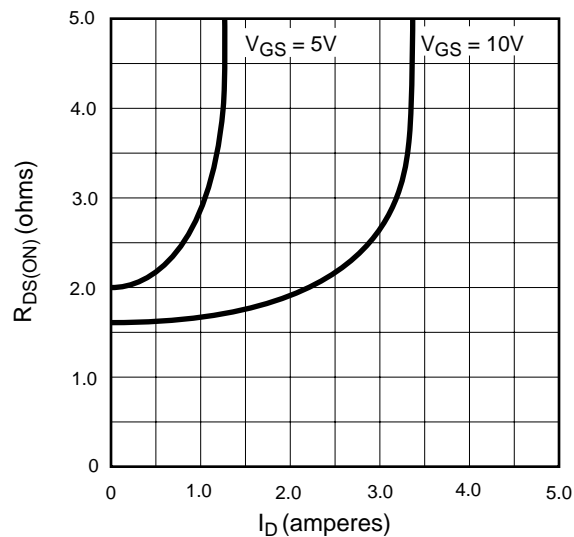


# Typical Performance Curves

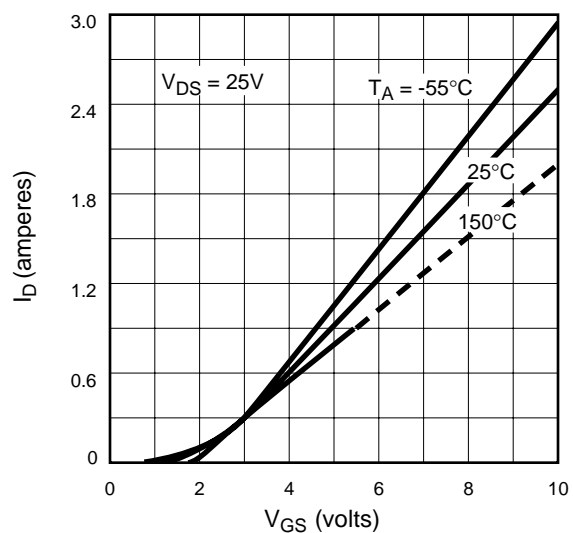
## BV<sub>DSS</sub> Variation with Temperature



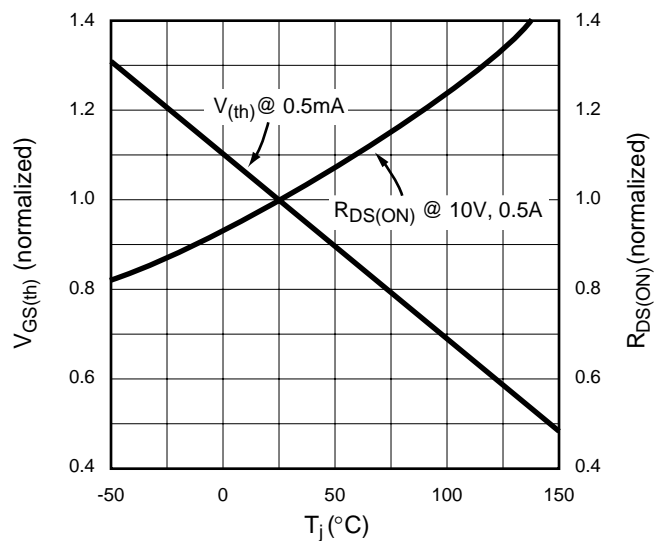
## On-Resistance vs. Drain Current



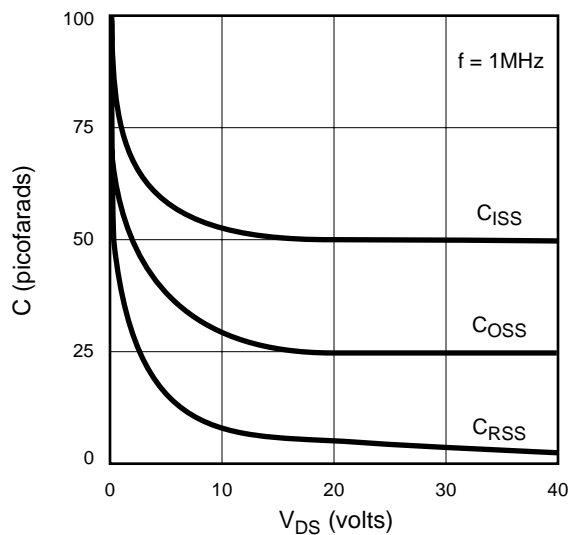
## Transfer Characteristics



## V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



## Capacitance vs. Drain-to-Source Voltage



## Gate Drive Dynamic Characteristics

