

JULY 2003

## DESCRIPTION

The 78P2343JAT is a low-power, 3-port DS3/E3/STS1 Line Interface Unit (LIU) with integrated Jitter Attenuator (JAT). It includes clock recovery and transmitter pulse shaping functions for applications using 75-ohm coaxial cable at distances up to 1350 feet. These applications include DSLAMs, T1,3/E1,3 digital multiplexers, SONET Add/Drop multiplexers, PDH equipment, DS3 to Fiber optic and microwave modems and ATM WAN access for routers and switches.

The receiver recovers clock and data from a B3ZS or HDB3 coded AMI signal. It can compensate for over 12dB of cable and 6dB of flat loss. The transmitter generates a signal that meets the standard pulse shape requirements. It has a B3ZS/HDB3 ENDEC with a receive line code violation detector, a loop-back mode, an input receive MUX that can select a redundant channel, a clock polarity selection mode, and the ability to receive a DSX3 monitor signal.

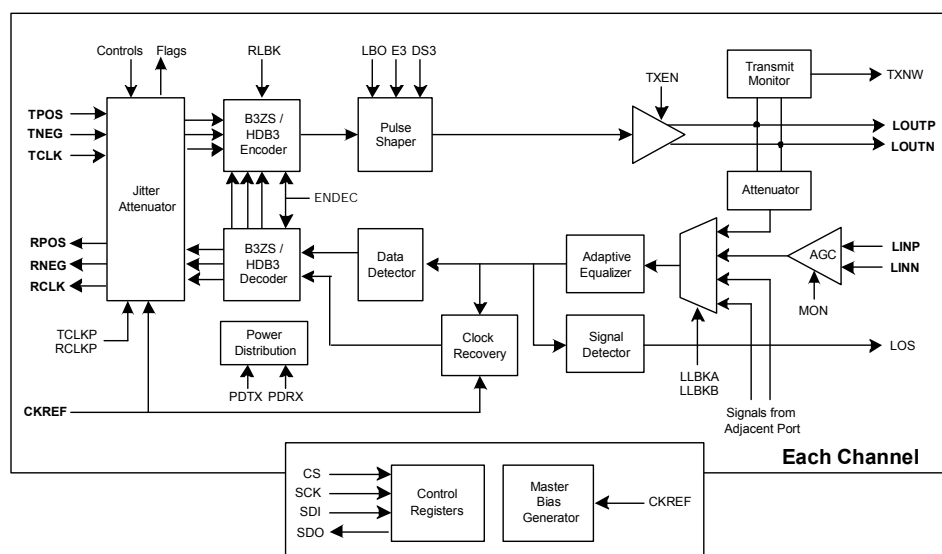
## STANDARDS

- Jitter Tolerance: Telcordia GR-499-CORE [DS3] and GR-253-CORE [STS1], ITU-T G.823 [E3] and G.824 [DS3]
- Loss of Signal: ITU-T G.775
- Jitter Transfer: ETSI TBR-24 1997 [E3]; Telcordia GR-499-CORE [DS3] and GR-253-CORE [DS3/STS1]

## FEATURES

- Transmit and receive interfaces for E3, DS3 and STS-1 applications
- Designed for use with 75 ohm coaxial cable up to 1350 ft long end-to-end or up to 900 ft long from a DS3 cross-connect
- Receives DS3-high and DSX3 monitor signals
- Local and Remote loopback
- Selectable B3ZS/HDB3 ENDEC with line code violation detector
- Standards-based LOS function
- Optional serial-port based mode selection and channel status monitoring
- Receiver AGC corrects for up to 6dB of flat loss
- Adaptive digital clock recovery (uses line-rate reference clock input)
- Receive output clock maintains nominal line-rate frequency at all times
- Fully integrated Jitter Attenuation function provided for all line rates (no external VCXO required)
- Jitter Attenuator configurable for transmit or receive path
- Transmit line fault monitor
- Requires no external current-setting resistor or loop filter components
- Single 3.3V supply operation
- Available in 100-pin Exposed Pad JEDEC LQFP

## BLOCK DIAGRAM



# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### FUNCTIONAL DESCRIPTION

The 78P2343JAT contains all the necessary transmit and receive circuitry for connection between E3, DS3, or STS-1 line interfaces and digital Framer/Mapper ICs.

#### OPERATING RATE

The Master Control Register (MSCR) determines which mode the device operates in according to the table below. The MSL0 pin is also provided for mode selection in applications without a serial control interface. Upon power-up or reset, the state of the MSL0 pin is sensed and mapped into the DS3 and E3 register bits representing the appropriate mode of operation. After power-up/reset, the state of the MSL0 pin is ignored.

Standard	MSL0 pin	DS3 bit	E3 bit
E3	L	0	1
DS3	H	1	0
STS-1	Z	0	0
STS-1	Z	1	1

#### RECEIVER OPERATION

The receiver input is either transformer-coupled or capacitor-coupled to the line signal. In applications where the highest performance and isolation are required, a 1:1 transformer is used in the receive path. In applications where isolation is provided elsewhere in the circuit, capacitor coupling can be used. The receiver input should be line terminated externally with a termination resistor.

The AMI signal first enters an AGC, which has a selectable gain range setting. In normal operation, the AGC can compensate for signals with up to 6dB of flat loss. When Receiver Monitor Mode is enabled, the AGC can compensate for a DSX3 monitor signal with 16 to 20 dB of flat loss. The signal then enters a high performance adaptive equalizer. The equalizer is designed to overcome inter-symbol interference caused by long cable lengths. Because the equalizer is adaptive, the circuit will work with all square-shaped signals such as DS3-high or 34.368 Mbit/s E3. The variable gain differential amplifier automatically controls the gain to maintain a constant voltage level output regardless of the input voltage level.

The outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a digital PLL, which uses a line-rate reference clock frequency applied to the CKREF pin.

The jitter tolerance of 78P2343 meets the requirements of ITU-T G.823 for E3 rates; the requirements of ITU-T G.824, GR-499 (Cat I and II) for DS3 rates; and the requirements of GR-253 for STS1 rates.

Without the Jitter Attenuator, the jitter transfer function meets the requirements of GR-499 for Category II DS3 interfaces.

When the Jitter Attenuator is enabled, the 78P2343JAT meets the requirements of GR-499 and GR-253 for all categories of DS3/STS1 equipment and the ETSI TBR-24 requirements for E3 rates. To check conformance with other standards, please refer to the JITTER ATTENUATOR TRANSFER FUNCTION section for more detailed info.

#### RECEIVER MONITOR MODE

When in monitor mode, 20dB of flat gain is applied to the incoming signal before it is fed to the receive equalizer. This mode is controlled by the MON bit in the Mode Control Register.

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## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### LOCAL LOOPBACK AND REDUNDANCY MUX

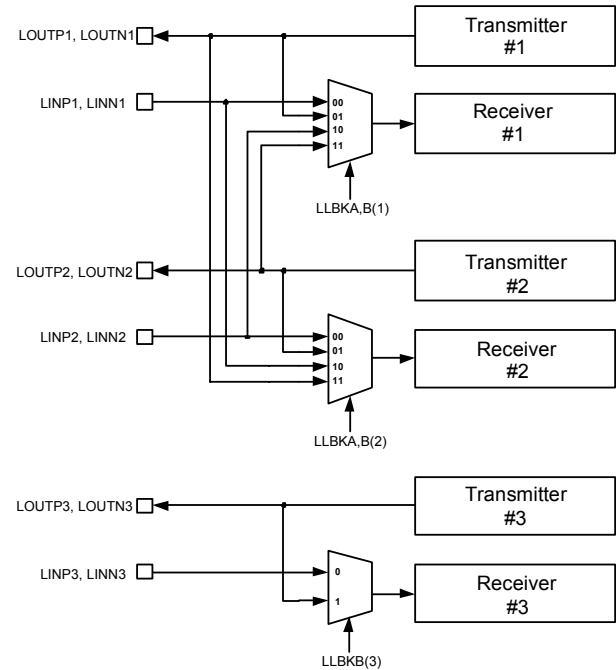
Receivers 1 and 2 have a 4-input MUX as shown in the adjacent figure. In multiport applications where redundant channels are required, the receiver MUX can be configured to provide the necessary multiplexing functions. This allows the user to use one port as a redundant monitor for the other port. The tables below show the register settings for selecting the desired receiver input source.

LLBKA (Port 1)	LLBKB (Port 1)	Receiver #1 Input Source
0	0	LINP1/LINN1
0	1	LOUTP1/LOUTN1
1	0	LINP2/LINN2
1	1	LOUTP2/LOUTN2

LLBKA (Port 2)	LLBKB (Port 2)	Receiver #2 Input Source
0	0	LINP2/LINN2
0	1	LOUTP2/LOUTN2
1	0	LINP1/LINN1
1	1	LOUTP1/LOUTN1

LLBKB (Port 3)	Receiver #3 Input Source
0	LINP3/LINN3
1	LOUTP3/LOUTN3

**Note:** The LLBKA and LLBKB bits are located in the Mode Control Register (MDCR). The Register Control bit, REGEN, should be enabled when using the register settings to avoid conflict with external loopback setting pins.



When serial interface control is not available, the respective LPBKx pin for each of the channels can also be used to activate local loopback mode as shown below. Note that redundant channel modes can only be activated using the serial interface.

LPBKx pin	Loopback Mode
L	Normal Operation Same as LLBKA,B = '00'
Z	Remote (Digital) Loopback Same as RLBK = '1'
H	Local (Analog) Loopback Same as LLBKA,B = '01'

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## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### SIGNAL DETECT

When the received signal is below a minimum threshold, the corresponding LOS signal (bit) is asserted. A time delay is provided before this output is active so that transient interruptions do not cause false indications. The LOS signal can also be used to trigger an interrupt on the INTRx pin when serial interface control is not available. This is controlled by setting the RXER bit in the Interrupt Control Register (INTC).

**Note:** In DS3 or STS-1 mode, when LBO is not enabled, the transmitters have to be properly terminated to ensure reliable LOS detection. If a transmitter is not terminated, the resultant 2x signal is large enough to couple to the neighboring receivers through the ESD diodes, causing false Signal Detect indication.

#### B3ZS/HDB3 ENDEC WITH LINE CODE VIOLATION DETECT

The 78P2343JAT includes a selectable B3ZS/HDB3 Encoder/Decoder (ENDEC). The ENDEC function can be enabled or disabled through pin selection or register setting. When the ENDEC is enabled, the decoder generates a composite NRZ logic data stream following the B3ZS (for DS3/STS-1) or HDB3 (for E3) substitution codes via the RPOS pin as shown below:

ENDEC bit/pin	RPOSx	RNEGx
0 / L	NRZ data	Receive Line Code Violation Indicator
1 / H	Positive AMI	Negative AMI

The decoder also detects Receive Line Code Violations (RLCV) and outputs a pulse via the RNEG pin. Three different classes of line code violations are detected.

- 1) Too many zeros: More than two (three) consecutive zeros in B3ZS (HDB3) mode.
- 2) Not enough zeros between bipolar pulse (B) and bipolar violation pulse (V): (B,V) for B3ZS. (B,V) or (B,0,V) for HDB3.
- 3) Code violation: Even number of bipolar pulses (B) detected between bipolar violation pulses (V).

On the transmit side, when the ENDEC is enabled, NRZ input data is encoded to Positive and Negative AMI logic data following the B3ZS (for DS3/STS-1) or HDB3 (for E3) substitution codes. The NRZ data is input to the TPOS pin as shown below:

ENDEC bit/pin	TPOSx	TNEGx
0 / L	NRZ data	'Don't Care'
1 / H	Positive AMI	Negative AMI

#### TRANSMITTER OPERATION

Transmitters 1-3 are enabled by their corresponding TXEN bit. When enabled, each transmitter accepts logic level clock (TCLKx), positive data (TPOSx) and negative data (TNEGx) signals and generates current pulses on the LOU TPx and LOU TNx pins. When properly connected to a 1:2CT center-tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable.

When the recommended transformer is used and when DS3 mode is selected, the transmitted pulse shape at the end of the 75Ω terminated cable of 0 to 450 feet will fit the DS3 template in ANSI T1.102-1993 and Telcordia GR-499-CORE standard documents. For STS-1 applications, the transmitted pulse for a short cable meets the requirements of Telcordia GR-253-CORE.

For E3 applications, the transmitted pulse for a short cable meets the requirements of ITU-T G.703.

In either DS3 and STS-1 modes, the LBOx pin or LBO bit should be set high for short cable (< 225 ft), and should be set low for long cable (> 225 ft). The LBO settings are ignored in E3 mode.

#### RCLK/TCLK POLARITY REVERSAL

To simplify the interface with various framer circuitry, TCLK polarity can be internally inverted by setting the TCLKP bit, and RCLK polarity can be inverted by setting the RCLKP bit. Both bits are located in the Master Control Register (MSCR).

#### REMOTE (DIGITAL) LOOPBACK

When the Register Control bit, REGEN, is disabled and the LPBKx pin is floating; or when the Register Control bit, REGEN, is enabled and the RLBK bit is set, RCLKx, RNEGx, and RPOSx outputs are internally looped back to the TCLKx, TNEGx, and TPOSx inputs respectively.

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## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### LINE BUILD-OUT

The Line Build-Out (LBO) function controls the transmit amplitude and pulse shape in DS3 and STS-1 modes. The selection of LBO depends on the amount of cable the transmitter is connected to. When less than 225 ft of cable is used, the corresponding LBOx pin or LBO bit should be high. When 225ft or more cable is used the corresponding LBO setting (LBOx pin or LBO bit) should be low. LBO can be controlled either from pins or from register settings, depending on the status of the Register Control bit, REGEN.

### TRANSMIT ENABLE

The TXEN bit in the Mode Control Register controls the transmitter output. When logic zero, the transmitter output is disabled. This feature is used to disable ports as well as to multiplex two or more transceivers to one port. The transmitter of any port can also be disabled by floating the respective LBOx pin, in which case it will also power-down the entire transmitter. See section on the Power-Down Function for more info.

### TRANSMIT MONITOR

The transmit monitor function detects activity on the transmitter output at the LOUTPx and LOUTNx pins. When there is a transmitter fault, in the case of an open or short on the chip, the transformer, or the circuit board, the transmit signal amplitude will be altered. The transmit monitor detects the amplitude of the driven signal. The TXNW signal (bit) goes high when the amplitude of the transmit signal is outside a valid amplitude range. When the signal amplitude is either too high or too low for longer than a specified duration, the TXNW bit goes high. The TXNW signal can be also used to trigger an interrupt on the INTRx pin when serial interface control is not available. This is accomplished by setting the TXER bit in the Interrupt Control Register (INTC).

### JITTER ATTENUATOR

Jitter Attenuation function is provided on-chip. The Jitter Attenuator can be configured to be in the transmit or the receive path. When configured in the transmit path, the input clock at TCLK pin is passed through a very low bandwidth digital PLL. The corresponding transmit data is buffered into a FIFO and clocked out using the de-jittered output clock of the PLL. When configured in the receive path, the recovered clock is passed through the low bandwidth digital PLL, and the corresponding receive data is buffered into the FIFO and clocked out using the de-jittered clock.

The Jitter Attenuator can be configured independently for each channel by writing to the Jitter Attenuator Control Register (JACR) as follows:

JAEN bit	JASL bit	Jitter Attenuator Mode
0	X	Jitter Attenuator disabled
1	0	Jitter Attenuator configured to be in the receive path
1	1	Jitter Attenuator configured to be in the transmit path

When serial interface control is not available, the MSL1 pin is provided for Jitter Attenuator mode selection. Upon power-up or reset, the state of the MSL1 pin is sensed and mapped into the JAEN and JASL register bits for all channels, representing the appropriate mode of operation. After power-up or reset, the state of the MSL1 pin is ignored. The state of the MSL1 pin, and the corresponding Jitter Attenuator configuration is shown below.

MSL1 pin	Jitter Attenuator Mode
L	Jitter Attenuator in receive path
H	Jitter Attenuator in transmit path
Z	Jitter Attenuator disabled

### PLL Bandwidth

A PLL response with effectively one pole below 27 Hz is adequate to meet the ETSI TBR24 E3 standards. A PLL response with one pole below 40 Hz is adequate to meet the GR-499 (Cat I) DS3 standards. Either of the two bandwidths can be selected via register setting. In either high or low bandwidth mode, the PLL bandwidth is proportional to the data rate as follows:

Line Rate	JABW bit	PLL Bandwidth (Hz)
E3	0	13
	1	188
DS3	0	17
	1	245
STS1	0	20
	1	283

The default state of the JABW bit depends on which line-rate is selected through the MSL0 pin. If E3 or DS3 mode is selected, the default state is '0'. If STS1 mode is selected, the default state is '1'.

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## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### Elastic Store Depth

To optimize the trade-off between data latency and clock wander tolerance, the FIFO elastic store depth can be selected through the serial port by writing to the Jitter Attenuator Control Register (JACR) as follows:

ESP[1:0] bits	Elastic Store Depth
00	Pass-Through mode
01	16 UI
10	32 UI
11	64 UI (default)

The Elastic Store Depth selects the nominal FIFO read pointer address. The total or maximum elastic store depth is set to be twice as deep as the nominal pointer address. The circular buffer length is always twice as long as the nominal pointer address.

### POWER-DOWN FUNCTION

Power-down control is provided to allow the transceivers to be shut off individually. Transmit and receive power-down can be set independently via the PCTX and PDRX bits in the Mode Control Register. Floating the respective LBOx pin can also set PCTX for each channel. The Serial Control Interface and Configuration Registers are not affected by power-down.

### INTERNAL POWER-ON RESET

The 78P2343JAT includes on-chip Power-On Reset (POR) function to ensure the serial-port registers are initialized to known default states upon power-up. This reset signal also sets all state machines within the transceivers to nominal operational states. The internal reset signal is also brought out to the POR pin. This pin is a multi-function pin which allows for the following:

- 1) Override the internal  $\overline{\text{POR}}$  signal by driving in an external active-low reset signal;
- 2) Monitor the state of the internal  $\overline{\text{POR}}$  signal (for test and debug only);
- 3) Add external capacitor to delay the release of the internal power-on reset signal to allow the MSL0 pin to stabilize prior to release of reset (approximately 8 $\mu$ s per nF added).

The internal resistance of the  $\overline{\text{POR}}$  pin is approximately 5k $\Omega$ .

### SERIAL CONTROL INTERFACE

The serial port controlled register allows a generic controller to interface with the 78P2343JAT. It is used for mode settings, diagnostics and test, and the retrieval of status and performance information.

The serial interface consists of four pins: Chip Select (CS), Serial Clock (SCK), Serial Data In (SDI), and Serial Data Out (SDO). The CS pin initiates the read and write operations. It can also be used to select a particular device allowing SCK, SDI and SDO to be bussed together. SCK is the clock input that times the data on SDI and SDO. Data on SDI is latched in on the rising-edge of SCK, and data on SDO is clocked out using the falling edge of SCK.

SDI is used to insert mode, address, and register data into the chip. Address and Data information are input least significant bit (LSB) first.

SDO is a tristate capable output. It is used to output register data during a read operation. SDO output is normally high impedance, and is enabled only during the duration when register data is being clocked out. Read data is clocked out least significant bit (LSB) first.

If SDI coming out of the micro-controller chip is also tristate capable, SDI and SDO can be connected together to simplify connections.

The maximum clock frequency for register access is 20MHz.

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## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### REGISTER DESCRIPTION

#### REGISTER ADDRESSING

Address Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Port Address				Sub-Address			Read/ Write
Assignment	PA[3]	PA[2]	PA[1]	PA[0]	SA[2]	SA[1]	SA[0]	R/W*

#### REGISTER TABLE

##### a) PA[3:0] = 0 : Global Registers

Sub Addr	Reg. Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	MSCR (R/W)	Master Control	REGEN <0>	DS3 <X>	E3 <X>	ENDEC <0>	RCLKP <0>	TCLKP <0>	--	SRST <0>
1	INTC (R/W)	Interrupt Control	INPOL <0>	--	--	--	JAFLG <0>	JAER <0>	RXER <1>	TXER <1>
2	RSVD	Reserved	--	--	--	--	--	--	--	--
3	RSVD	Reserved	<0>	<0>	<0>	<0>	<0>	<0>	<0>	<0>
4	RSVD	Reserved	--	--	--	--	--	--	--	--
5	RSVD	Reserved	--	--	--	--	--	--	--	--
6	RSVD	Reserved	<0>	<0>	<0>	<0>	<0>	<0>	<0>	<0>
7	RSVD	Reserved	<0>	<0>	<0>	<0>	<0>	<0>	<0>	<0>

##### b) PA[3:0] = 1-3 : Port-Specific Registers

Sub Addr	Reg. Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	MDCR (R/W)	Mode Control	PDTX <0>	PDRX <0>	LBO <1>	LLBKA <0>	LLBKB <0>	RLBK <0>	MON <0>	TXEN <1>
1	STAT (R/O)	Status Monitor	FERR	--	--	--	LOS	TXNW	--	SGLO
2	RSVD	Reserved	<1>	<1>	<0>	<1>	<0>	<1>	<0>	<0>
3	JACR (R/W)	Jitter Attenuator Control	JAEN <X>	JASL <X>	JLBK <0>	<0>	ESP[1] <1>	ESP[0] <1>	<0>	JABW <X>
4	RSVD	Reserved	--	--	--	--	--	--	--	--
5	RSVD	Reserved	<0>	--	--	<0>	<0>	<0>	<0>	<0>
6	RSVD	Reserved	--	--	--	--	--	--	--	--
7	RSVD	Reserved	<0>	<0>	<0>	<0>	<0>	<0>	<0>	<0>

Note: Shaded registers in Register Table are reserved for TDK internal use only. Accessing reserved or undefined registers may cause undesirable operation.

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## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### REGISTER DESCRIPTION (continued)

#### LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
R/O	Read only	R/W	Read or Write

#### GLOBAL REGISTERS

##### ADDRESS 0-0: MASTER CONTROL REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	REGEN	R/W	0	Register Control Enable: 0 : Pin selection overrides register settings 1 : Device is controlled via register set. <b>NOTE: Pin 15 (ENDEC) must be tied low when REGEN is enabled.</b>
6	DS3	R/W	X	Line Speed Selection: Selects the line speed of all channels as well as the input clock frequency at the CKREF pin. [DS3 E3] = 00 : STS-1 (51.840MHz) 01 : E3 (34.368MHz) 10 : DS3 (44.736MHz) 11 : STS-1 (51.840MHz)  NOTE: The default values of these register bits depend on the state of the MSL0 pin upon power-up or reset.
5	E3	R/W	X	
4	ENDEC	R/W	0	Encoder/Decoder Disable: 0 : selects NRZ digital data interface 1 : selects AMI digital data interface NOTE: Relevant only when the REGEN bit is set. Otherwise, ENDEC pin selection prevails.
3	RCLKP	R/W	0	RCLK Polarity Selection: 0 : Receive Data clocked out on the falling-edge of RCLK 1 : Receive Data clocked out on the rising-edge of RCLK
2	TCLKP	R/W	0	TCLK Polarity Selection: 0 : Transmit Data clocked in on the rising-edge of TCLK 1 : Transmit Data clocked in on the falling-edge of TCLK
1	RSVD	R/O	X	Reserved
0	SRST	R/W	0	Register Soft-Reset: When this bit is set, all registers are reset to their default values. Also resets Jitter Attenuator to “centered” states. This register bit is self-clearing.



# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### REGISTER DESCRIPTION (continued)

#### ADDRESS 0-1: INTERRUPT CONTROL REGISTER

This register selects the events that would cause the respective interrupt pin (INTRx) for each of the ports to be activated. User may set as many bits as required.

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	INPOL	R/W	0	Interrupt Pin Polarity Selection: 0 : Interrupt output is active-low 1 : Interrupt output is active-high
6:3	RSVD	R/O	0	Reserved
2	JAER	R/W	0	Jitter Attenuator Error Event: When set, JAT FIFO overflow or underflow (as indicated by the FERR bit) will cause an interrupt to be flagged.
1	RXER	R/W	1	Receiver Error Event: When set, loss of receive signal (as indicated by the LOS bit) will cause an interrupt to be flagged.
0	TXER	R/W	1	Transmitter Error Event: When set, transmitter fault (as indicated by the TXNW bit) will cause an interrupt to be flagged.

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## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### REGISTER DESCRIPTION (continued)

##### PORT-SPECIFIC REGISTERS

For PA[3:0] = N = 1-3 only. Accessing a register with port address greater than 3 constitutes an invalid command, and the read/write operation will be ignored.

##### ADDRESS N-0: MODE CONTROL REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	PDTX	R/W	0	Transmitter Power-Down: 0 : Normal Operation 1 : Power-Down NOTE: Relevant only when the REGEN bit is set. Otherwise, LBOx pin selection prevails.
6	PDRX	R/W	0	Receiver Power-Down: 0 : Normal Operation 1 : Power-Down
5	LBO	R/W	1	Transmitter Line Build-Out (DS3 and STS-1 only): 0 : ≥ 225ft of cable attached to the cross-connect 1 : < 225ft of cable attached to the cross-connect NOTE: Relevant only when the REGEN bit is set. Otherwise, LBOx pin selection prevails.
4	LLBKA	R/W	0	Local (Analog) Loopback Mode Selection: [LLBKA LLBKB] = 00 : Normal operation 01 : Transmitter loopback 10 : Adjacent receiver input 11 : Adjacent transmitter loopback NOTE: Relevant only when the REGEN bit is set. Otherwise, LPBKx pin selection prevails.
3	LLBKB	R/W	0	
2	RLBK	R/W	0	Remote (Digital) Loopback Enable: 0 : Normal Operation 1 : Loops RCLK, RPOS, and RNEG back onto TCLK, TPOS, and TNEG NOTE: Relevant only when the REGEN bit is set. Otherwise, LPBKx pin selection prevails.
1	MON	R/W	0	Monitor Mode Enable: Used for reception of split-off signals that are flat attenuated by at least 16dB but no more than 20dB. 0 : Disable 1 : Enable
0	TXEN	R/W	1	Transmitter Output Enable: 0 : Transmit driver is disabled 1 : Normal Operation NOTE: Relevant only when the REGEN bit is set. Otherwise, LBOx pin selection prevails.

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**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

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**REGISTER DESCRIPTION** (continued)

**ADDRESS N-1: STATUS MONITOR REGISTER**

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	FERR	R/O	X	Jitter Attenuator FIFO Error Flag: This bit is set whenever a FIFO overflow or underflow occurred. It is reset after a read operation to this register. 0 : Proper Operation 1 : FIFO Overflow/Underflow
6:4	RSVD	R/O	X	Reserved
3	LOS	R/O	X	Loss-of-Signal Indication: 0 : Signal Detector detecting a valid receive input signal 1 : Standards-based Loss-of-Signal indication NOTE: RPOSx and RNEGx are forced low when LOS='1'. RCLK will continue to output a line rate clock
2	TXNW	R/O	X	Transmitter Not-Working Indication: 0 : Transmitter OK 1 : Transmitter not working
1	RSVD	R/O	X	Reserved
0	SGLO	R/O	X	Signal Low Indication: 0 : Receive signal level OK 1 : Receive signal level too low / Loss of signal

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## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### REGISTER DESCRIPTION (continued)

#### ADDRESS N-3: JITTER ATTENUATOR CONTROL REGISTER

BIT	NAME	TYPE	DFLT VALUE	DESCRIPTION
7	JAEN	R/W	X	Jitter Attenuator Enable: 0 : Disables jitter attenuation function 1 : Enables jitter attenuation function NOTE: The default values of these register bits depend on the state of the MSL1 pin upon power-up or reset.
6	JASL	R/W	X	Jitter Attenuation Selection: 0 : Jitter Attenuator on the receive path 1 : Jitter Attenuator on the transmit path NOTE: The default values of these register bits depend on the state of the MSL1 pin upon power-up or reset.
5	JLBK	R/W	0	Jitter Attenuator Local Loopback Enable: 0 : Normal Operation 1 : TCLKx, TPOSx, TNEGx connected to JAT input and RCLKx, RPOSx, RNEGx connected to JAT output NOTE: If both RLBK and JLBK bits are set, RLBK mode takes priority.
4	RSVD	R/W	0	Reserved. Must be set to zero.
3:2	ESP [1:0]	R/W	11	FIFO Elastic Store Pointer Selection: 00 : Pass-through 01 : 8 UI 10 : 16 UI 11 : 32 UI
1	RSVD	R/W	0	Reserved. Must be set to zero.
0	JABW	R/W	X	Jitter Attenuator Bandwidth Selection: 0 : Low bandwidth 1 : High bandwidth (see JAT Bandwidth Selection Table on page 5) NOTE: The default values of these register bits depend on the state of the MSL1 pin upon power-up or reset. If the state of the MSL0 pin selects E3 or DS3 mode, the default value of JABW is '0'. If the state of the MSL0 pin selects STS1 mode, the default value of JABW is '1'.

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**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

**PIN DESCRIPTION**

**LEGEND**

TYPE	DESCRIPTION	TYPE	DESCRIPTION
A	Analog Pin	CIT	CMOS 3-State Input
CI	CMOS Digital Input	CO	CMOS Digital Output
CIU	CMOS Digital Input w/ Pull-up	COZ	CMOS Tristate Digital Output
CID	CMOS Digital Input w/ Pull-down	S	Supply
CIS	CMOS Schmitt Trigger Input	G	Ground

**TRANSMITTER PINS**

NAME	PIN	TYPE	DESCRIPTION
TPOSx	23, 31 39	CI	Transmit Positive Data/Transmit NRZ: When ENDEC bit = '1', a logic one on this pin generates a positive AMI pulse on the coax. This pin should not be high at the same time that corresponding TNEGx is high. When ENDEC bit = '0', data on this pin is encoded and converted into positive and negative AMI pulses.
TNEGx	24, 32 40	CI	Transmit Negative Data: When ENDEC bit = '1', a logic one on this pin generates a negative AMI pulse on the coax. This pin should not be high at the same time that corresponding TPOSx is high. When ENDEC bit = '0', this pin is ignored.
TCLKx	25, 33 41	CIS	Transmitter Clock Input: This signal is used to latch the respective TPOSx and TNEGx signals into the 78P2343JAT.
LOUTPx	98, 92 85	A	Line Out: Differential AMI Outputs. Requires a 1:2CT center-tapped transformer and a shunt termination resistor. See APPLICATION INFORMATION section for more info.
LOUTNx	99, 93 86		

# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### PIN DESCRIPTION (continued)

##### RECEIVER PINS

NAME	PIN	TYPE	DESCRIPTION
CKREF	57	CIS	Reference Clock Input: This clock should be from a clean source ( $\pm 20$ ppm) and represents the line-rate frequency as follows: E3 : 34.368 MHz DS3: 44.736 MHz STS-1: 51.840 MHz
RCLKx	27, 35 43	CO	Receive Clock: Recovered receive clock. Note: During LOS conditions, RCLKx will continue to output a line rate clock
RNEGx	28, 36 44	CO	Receive Negative Data: When ENDEC bit = '1', this pin indicates reception of a negative AMI pulse on the coax. When ENDEC bit = '0', this pin outputs a one when a receive line code violation is detected.
RPOSx	29, 37 45	CO	Receive Positive Data/NRZ Data: When ENDEC bit = '1', this pin indicates reception of a positive AMI pulse on the coax cable. When ENDEC bit = '0', it outputs decoded NRZ data.
LINPx  LINNx	96, 90 83  95, 89 82	A	Line In: Differential AMI Inputs. Should be 1:1 transformer-coupled and terminated with a shunt resistor. See APPLICATION INFORMATION section for more info.

##### CONTROL AND STATUS PINS

NAME	PIN	TYPE	DESCRIPTION
MSL0	19	CIT	Data-Rate Mode Selection: Low = E3 mode High = DS3 mode Float = STS-1 mode NOTE: Pin state is latched-in on rising-edge of POR signal
MSL1	20	CIT	Jitter Attenuator Mode Selection: Low = JAT in Receive path High = JAT in Transmit path Float = JAT is bypassed NOTE: Pin state is latched-in on rising-edge of POR signal
POR	14	A	Chip Reset (active-low): Forces hardware reset on device. See description on <i>Internal Power-on Reset</i> for complete use of this pin.
ENDEC	15	CID	ENDEC Enable (active-low): Set high to disable internal ENDEC function. NOTE: Relevant only when the REGEN bit is '0'. <b>Pin must be held low when the REGEN bit is set.</b>

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## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### PIN DESCRIPTION (continued)

#### CONTROL AND STATUS PINS (continued)

LBOx	5, 6 7	CIT	Line Build-Out: Low = Used with 225ft or more of cable. High = Used with less than 225ft of cable. Float = Disable and power down transmitter. [TXEN=0; PDTX=1] NOTE: Relevant only when the REGEN bit is '0'. Pin state sampled approximately once every 0.5ms.
LPBKx	10, 11 12	CIT	Loopback Enable: Low = Normal Operation High = Local Loopback. Transmitter looped back to Receiver Float = Remote Loopback. Receiver looped back to Transmitter NOTE: Relevant only when the REGEN bit is '0'. Pin state sampled approximately once every 0.5ms.
INTRx	64, 63 62	CO	Interrupt Flag: This pin is normally high when the INPOL bit is '0' (default), and normally low when the INPOL bit is '1'. When an interrupt event occurs (as defined in the Interrupt Control Register description), the respective INTRx pin will change state.

#### SERIAL-PORT PINS

NAME	PIN	TYPE	DESCRIPTION
CS	65	CI	Chip Select: High during write and read operations. Low disables the serial port. While CS is low, SDO remains in high impedance state, and SDI and SCK activities are ignored.
SCK	66	CIS	Serial Clock: Controls the timing of SDI and SDO.
SDI	68	CI	Serial Data Input: Inputs mode and address information. Also inputs register data during a Write operation. Both address and data are input least significant bit first.
SDO	67	COZ	Serial Data Output: Outputs register information during a Read operation. Data is output least significant bit first.

#### POWER AND GROUND PINS

It is recommended that all supply pins be connected to a single power supply plane and all ground pins be connected to a single ground plane.

NAME	PIN	TYPE	DESCRIPTION
VCC	1, 2, 3, 4, 17, 59, 72, 73, 74, 75	S	Analog Power Supply
GND	18, 60, 78, 81, 84, 87, 91, 94, 97, 100	S	Analog Ground
VCCD	16, 22, 30, 38, 46, 54, 55, 58	S	Digital Power Supply
GNDD	9, 21, 26, 34, 42, 50, 56, 69	S	Digital Ground

# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### ELECTRICAL SPECIFICATIONS

##### ABSOLUTE MAXIMUM RATINGS

Operation beyond these limits may permanently damage the device.

PARAMETER	RATING
Supply Voltage (VCC/VCCD)	-0.5 to 4.0 VDC
Storage Temperature	-65 to 150 °C
Junction Temperature	-40 to 125 °C
Pin Voltage (LOUTPx, LOUTNx)	VCC + 1.5 VDC
Pin Voltage (all other pins)	-0.3 to (VCC+0.6) VDC
Pin Current	±100 mA

##### RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

PARAMETER	RATING
DC Voltage Supply (VCC/VCCD)	3.0 to 3.6 V
Ambient Operating Temperature	-40 to 85°C

##### DC CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	I <sub>dd</sub>	All channels on DS3 mode JAT Enabled: JAT Disabled:		257 240	282 263	mA mA
Receive-only Supply Current	I <sub>ddr</sub>	All channels PDTX = 1 DS3 mode JAT Enabled: JAT Disabled:		91 73		mA mA
Transmit-only Supply Current	I <sub>ddt</sub>	All channels PDRX = 1 DS3 mode JAT Enabled: JAT Disabled:		173 155		mA mA
Supply Current per Port (including transmitter current through transformer)	I <sub>ddx</sub>	DS3 mode JAT Enabled: JAT Disabled:		82 76		mA mA
Power-Down Current	I <sub>ddq</sub>	DS3 mode PDTX = 1, PDRX = 1 All clocks off		11	15	mA



# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### ELECTRICAL SPECIFICATIONS (continued)

#### ANALOG PINS CHARACTERISTICS:

The following table is provided for informative purpose only. Not tested in production.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
LINPx and LINNx Common-Mode Bias Voltage	Vblin	Ground reference	1.9	2.25	2.6	V
LINPx and LINNx Differential Input Impedance	Rilin			10		kΩ
POR Input Impedance	Ripor			5		kΩ

#### DIGITAL I/O CHARACTERISTICS:

Pins of type CI, CIU, CID:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	Vil				0.8	V
Input Voltage High	Vih		2.0			V
Input Current	Iil, Iih		-1		1	μA
Pull-up Resistance	Rpu	Type CIU only	38	56	78	kΩ
Pull-down Resistance	Rpd	Type CID only	38	56	78	kΩ
Input Capacitance	Cin			8		pF

Pins of type CIS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Low-to-High Threshold	Vt+		1.3		1.7	V
High-to-Low Threshold	Vt-		0.8		1.2	V
Input Current	Iil, Iih		-1		1	μA
Input Capacitance	Cin			8		pF

# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### ELECTRICAL SPECIFICATIONS (continued)

Pins of type CIT:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	V <sub>til</sub>				0.8	V
Input Voltage High	V <sub>tih</sub>		2.0			V
Minimum impedance to be considered as “float” state	R <sub>tiz</sub>		30			kΩ

Pins of type CO and COZ:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	V <sub>ol</sub>	I <sub>ol</sub> = 8mA			0.4	V
Output Voltage High	V <sub>oh</sub>	I <sub>oh</sub> = -8mA	2.4			V
Output Transition Time	T <sub>t</sub>	C <sub>L</sub> = 20pF; (20-80%)			6	ns
Pin Capacitance	C <sub>out</sub>			8		pF
Effective Source Impedance	R <sub>src</sub>			30		Ω
Tristate Output Leakage Current	I <sub>z</sub>	Type COZ only	-1		1	μA

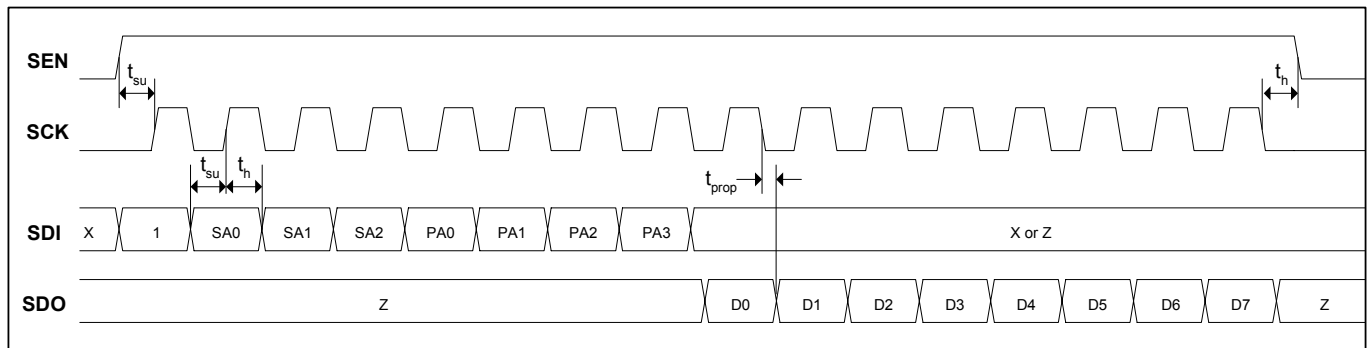
# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

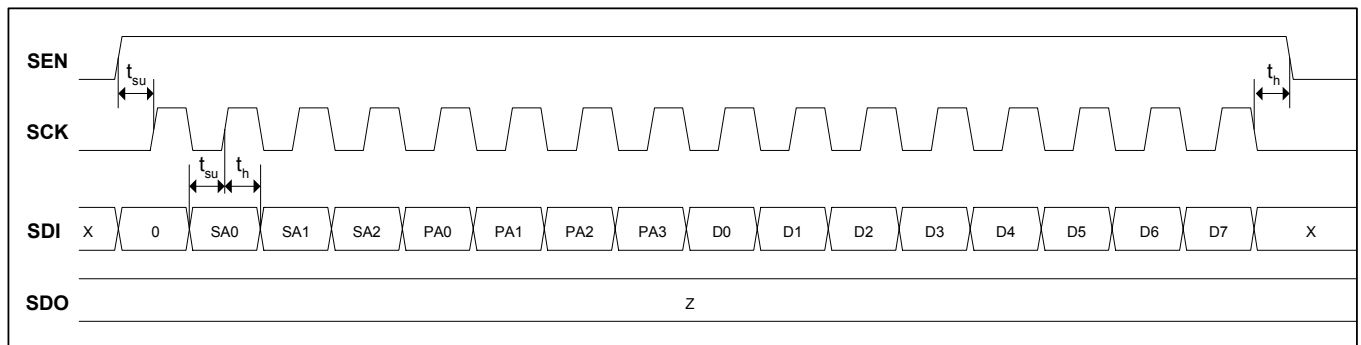
### ELECTRICAL SPECIFICATIONS (continued)

#### SERIAL-PORT TIMING CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
CS or SDI to SCK setup time	$t_{su}$		4			ns
CS or SDI to SCK hold time	$t_h$		4			ns
SCK to SDO propagation delay	$t_{prop}$		5		12	ns



#### Read Operation



#### Write Operation

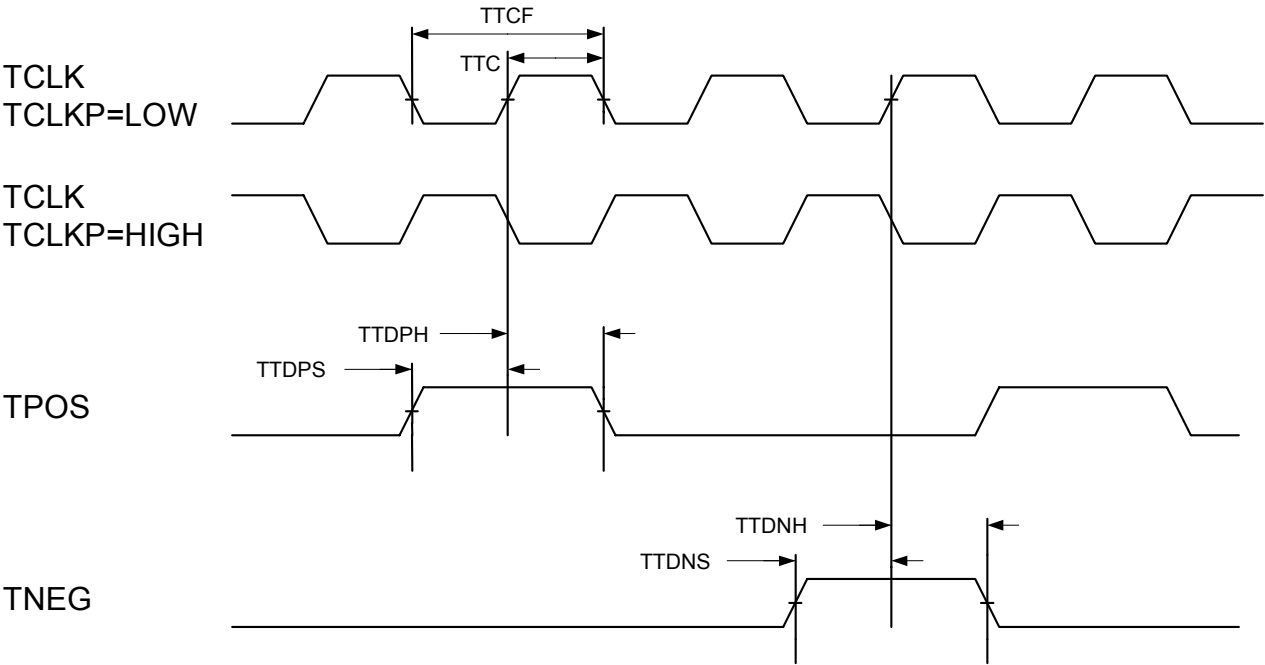
**78P2343JAT**  
**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

**ELECTRICAL SPECIFICATIONS** (continued)

**TRANSMITTER TIMING CHARACTERISTICS:**

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Clock Duty Cycle	TTCF/TTC		40		60	%
Setup Time	TTDPS		2.5			ns
Hold Time	TTDPH		2.5			ns

**TIMING DIAGRAM: Transmitter Waveforms (E3/DS3/STS-1)**



# 78P2343JAT

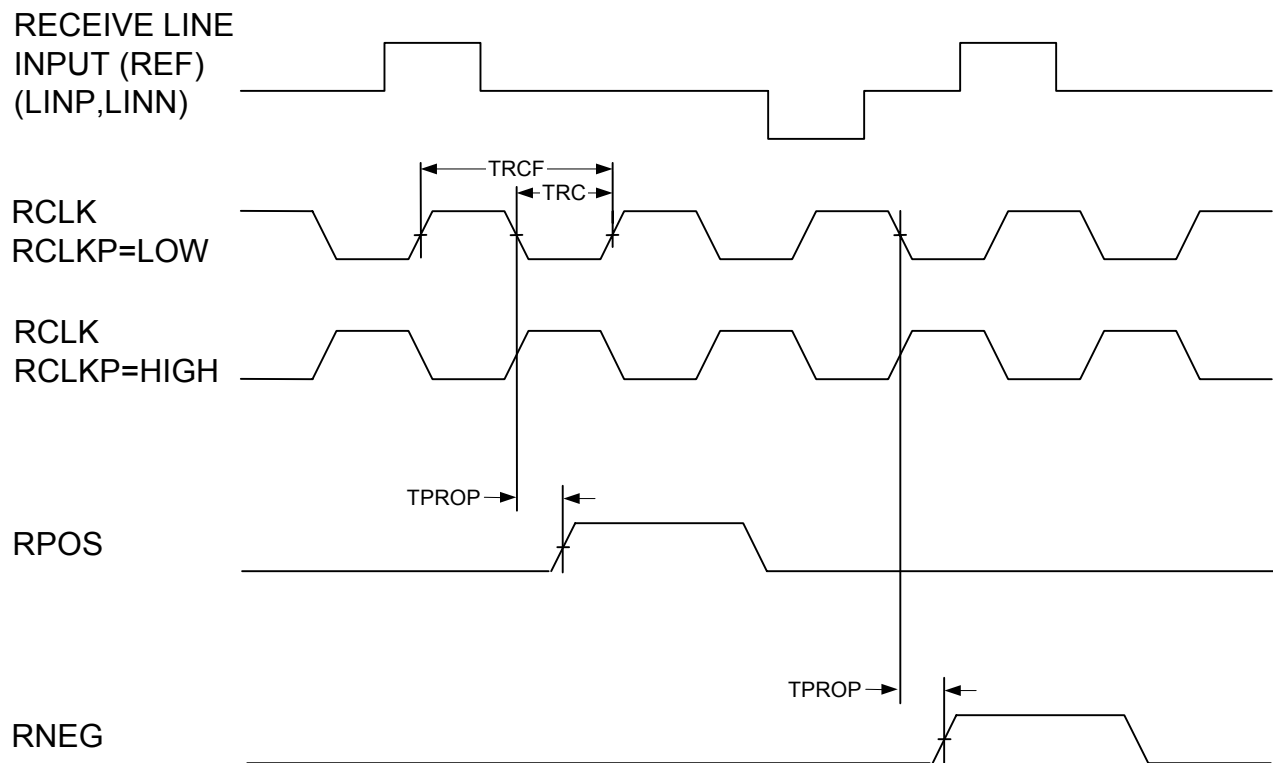
## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### ELECTRICAL SPECIFICATIONS (continued)

#### RECEIVER TIMING CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
CKREF Duty Cycle	--		40		60	%
CKREF Frequency Stability	--	w.r.t. line-rate frequency	-20		+20	ppm
RCLK Duty Cycle	TRCF/TRC		40		60	%
Data Propagation Delay	TPROP		-2		3	ns

#### TIMING DIAGRAM: Receive Waveforms (E3/DS3/STS-1)



# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### ELECTRICAL SPECIFICATIONS (continued)

##### DS3 TRANSMITTER

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Transmitter Amplitude	Measured at LOU TP/LOU TN pins w/ 37.5Ω load and LBO pin held high.	700	800	850	mVpk
Transmitter Amplitude Mismatch	Ratio of amplitudes of positive and negative pulses measured at pulse peaks.	0.9		1.1	
Transmitter Power at 22.368 MHz	All ones pattern, 3kHz bandwidth	-1.8		+5.7	dBm
Harmonic Power at 44.736 MHz	All ones pattern Power below fundamental at 22.368MHz			-20	dBm

##### STS-1 TRANSMITTER

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Transmitter Amplitude	Measured at LOU TP/LOU TN pins w/ 37.5Ω effective load and LBO pin held high.	700	825	950	mVpk
Transmitter Amplitude Mismatch	Ratio of amplitudes of positive and negative pulses measured at pulse peaks.	0.9		1.1	
Transmitter Power	PRBS15 pattern band-limited to 207.36MHz.	-2.7		+4.7	dBm

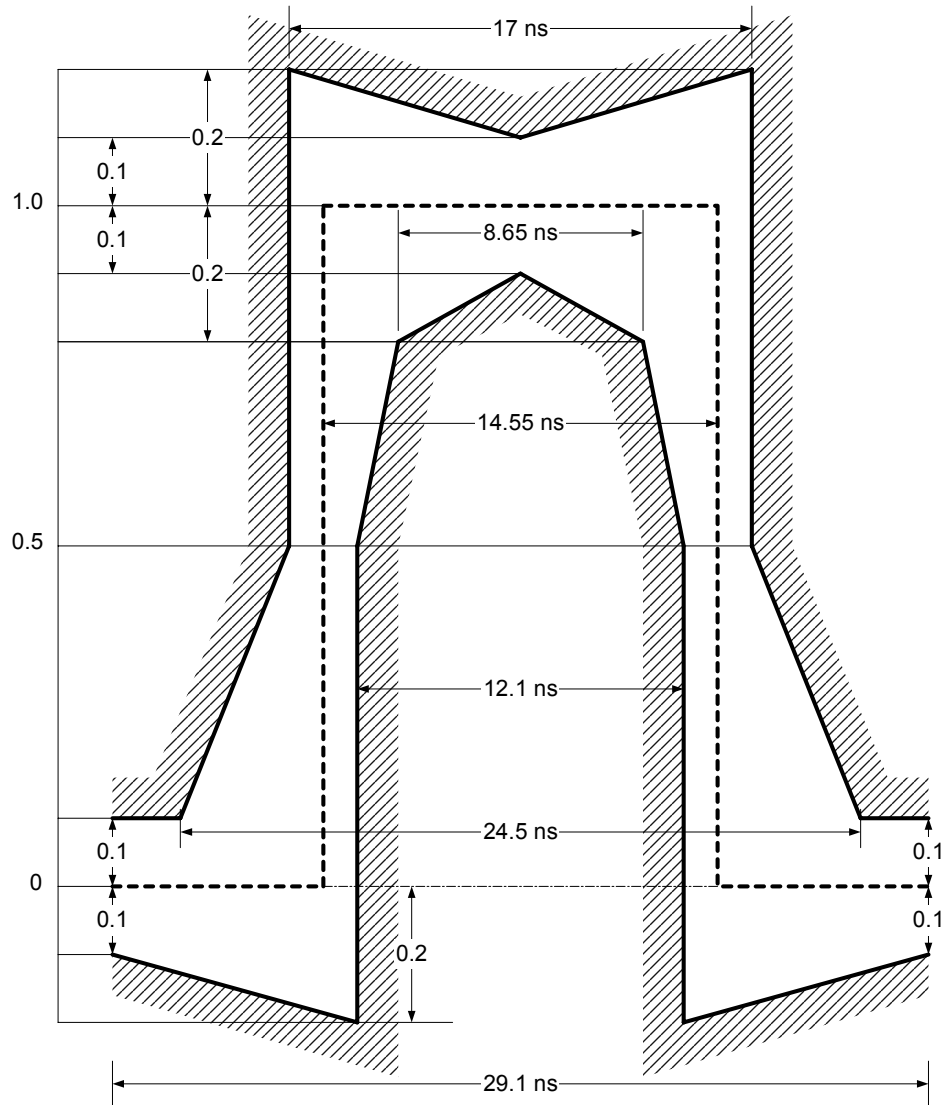
##### E3 – TRANSMITTER

PARAMETER	CONDITION (see timing diagram)	MIN	TYP	MAX	UNIT
Transmitter Amplitude	Measured at LOU TP/LOU TN pins w/ 37.5Ω load.	900	1000	1100	mVpk
Transmitter Amplitude Mismatch	Ratio of amplitudes of positive and negative pulses measured at pulse centers	0.95		1.05	
Transmitter Pulsewidth Mismatch	Ratio of widths of positive and negative pulses measured at pulse half amplitude	0.95		1.05	
Transmitter Pulsewidth	Measured at LOU TP/LOU TN pins		14.8		ns

**78P2343JAT**  
**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

**ELECTRICAL SPECIFICATIONS** (continued)

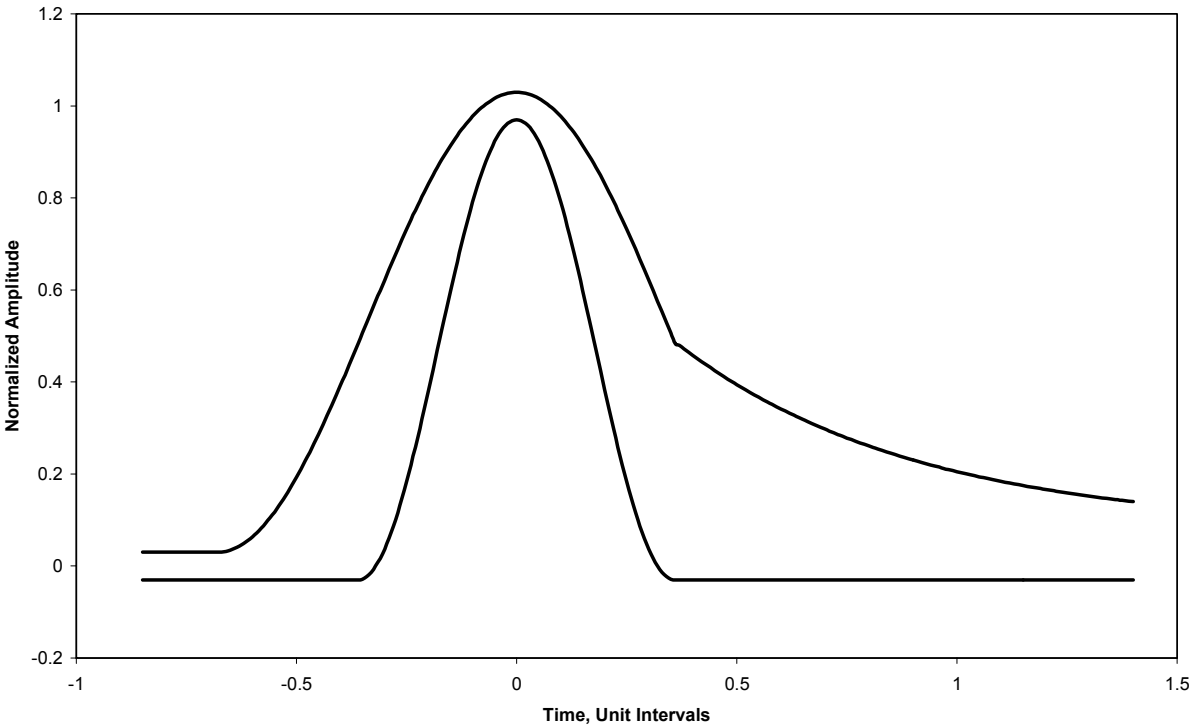
**E3 TRANSMIT PULSE TEMPLATE**



**78P2343JAT**  
**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

**ELECTRICAL SPECIFICATIONS** (continued)

**DS3 TRANSMIT PULSE TEMPLATE**



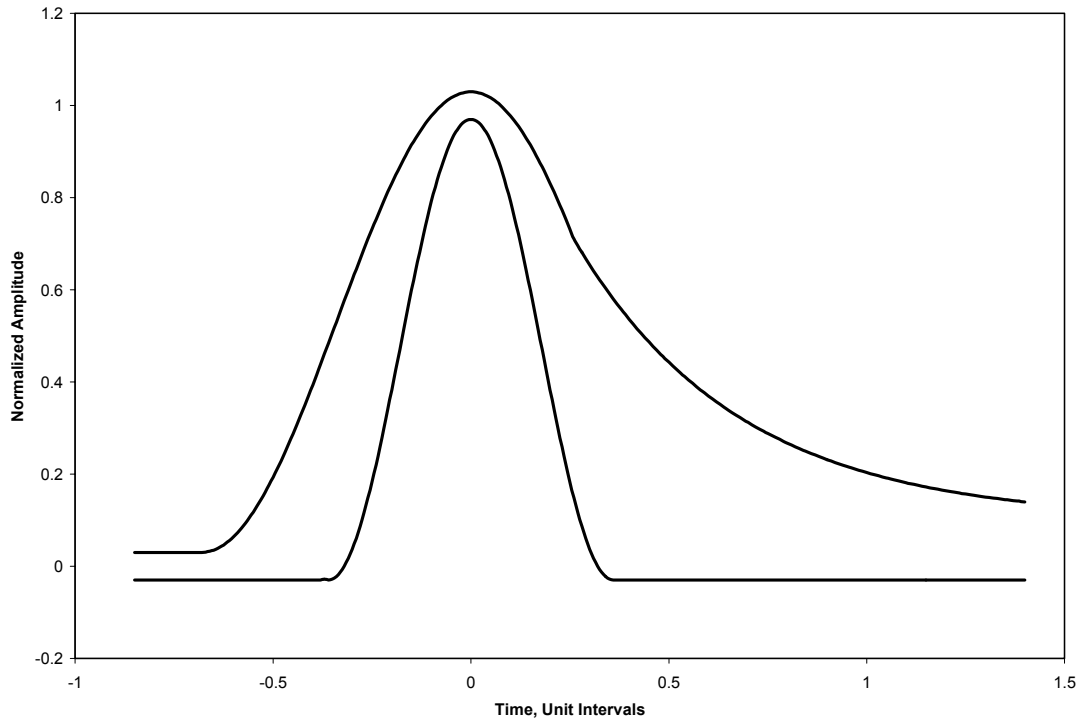
Time axis range (UI)	Normalized amplitude equation
<b>UPPER CURVE</b>	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.03 + 0.5\{1 + \sin[(\pi/2)(1 + T/0.34)]\}$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 e^{-1.84(T-0.36)}$
<b>LOWER CURVE</b>	
$-0.85 \leq T \leq -0.36$	-0.03
$-0.36 \leq T \leq 0.36$	$-0.03 + 0.5\{1 + \sin[(\pi/2)(1 + T/0.18)]\}$
$0.36 \leq T \leq 1.4$	-0.03



**78P2343JAT**  
**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

**ELECTRICAL SPECIFICATIONS** (continued)

**STS-1 TRANSMIT PULSE TEMPLATE**



**STS-1 (Transmit template specs)**

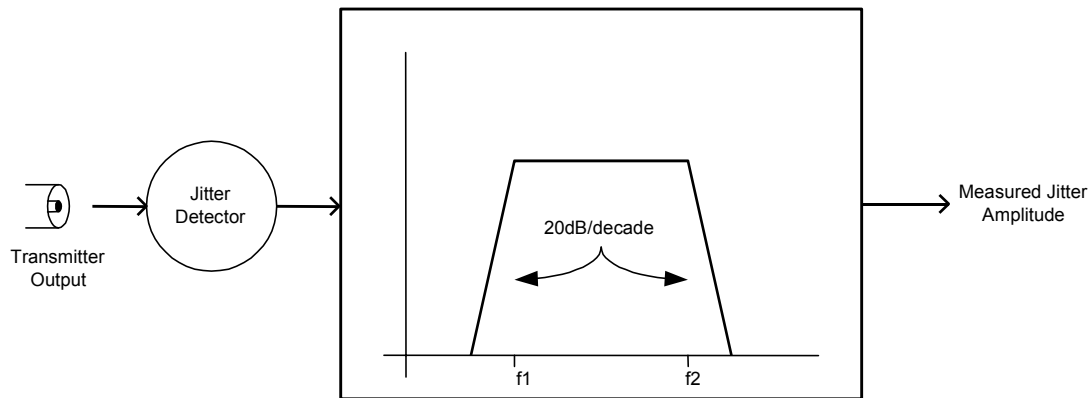
Time axis range (T)	Normalized amplitude equation (A)
<b>UPPER CURVE</b>	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.03 + 0.5\{1 + \sin[(\pi/2)(1 + T/0.34)]\}$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 e^{-2.4(T-0.26)}$
<b>LOWER CURVE</b>	
$-0.85 \leq T \leq -0.38$	-0.03
$-0.38 \leq T \leq 0.36$	$-0.03 + 0.5\{1 + \sin[(\pi/2)(1 + T/0.18)]\}$
$0.36 \leq T \leq 1.4$	-0.03

**78P2343JAT**  
**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

**ELECTRICAL SPECIFICATIONS** (continued)

**TRANSMITTER OUTPUT JITTER**

The transmit jitter specification ensures compliance with ITU-T G.823 and G.824, Telcordia GR-499 CORE(I) and GR-253-CORE, and ANSI T1.102-1993 for all supported rates. Transmit output jitter is guaranteed only if a clean SONET quality transmit clock source is used.



PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Transmitter Output Jitter	10 Hz to 800 kHz			0.15	UIpp
	10 kHz to 800 kHz			0.08	UIpp

Note: Filters defined by standards are used for all testing

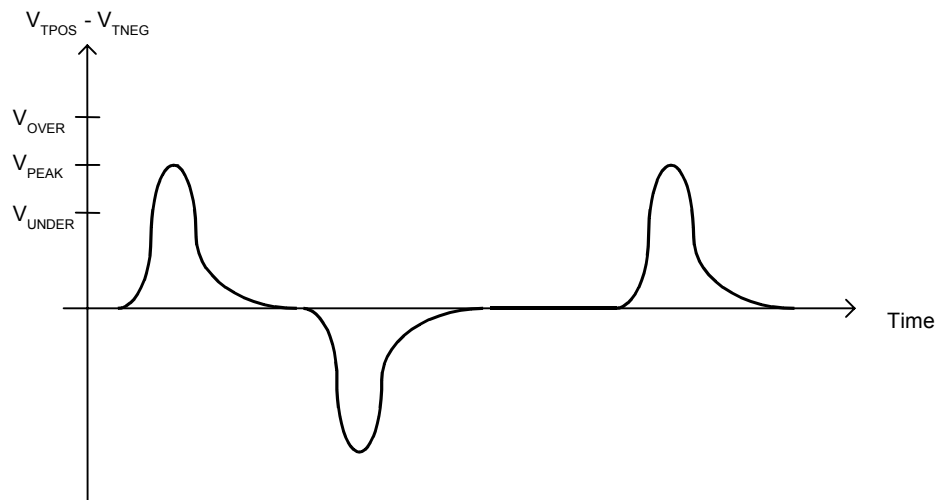
# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### ELECTRICAL SPECIFICATIONS (continued)

#### TRANSMIT MONITOR

The transmit monitor function looks at the signals on the LOUTPx and LOUTNx pins and checks for the existence of a valid signal. The monitor detects the peak of the transmitted signal at the LOUTPx and LOUTNx pins and checks that it is between  $V_{\text{UNDER}}$  and  $V_{\text{OVER}}$  at all times. If the peak level is within the voltage threshold window, the TXNW signal is low. If the peak level falls outside of the threshold limits for more than approximately 32 bit times, the TXNW signal goes high.



PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$V_{\text{UNDER}}$	DS3 mode with LBOx=1 STS-1 mode		320		mVpk
$V_{\text{UNDER}}$	E3 mode DS3 mode with LBOx=0		400		mVpk
$V_{\text{OVER}}$	DS3 mode with LBOx=1 STS-1 mode		1280		mVpk
$V_{\text{OVER}}$	E3 mode DS3 mode with LBOx=0		1600		mVpk

# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### ELECTRICAL SPECIFICATIONS (continued)

##### DS3/STS-1 RECEIVER (Transformer-coupled)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Peak Differential Input Amplitude, LINPx and LINNx	MON=0. Signal at DSX is 360-850 mVpk. See Notes 2, 3	90		850	mVpk
	MON=1	25		80	mVpk
	MON=0. DS3-HIGH	90		1200	mVpk
Flat-loss Tolerance	MON=0. All valid cable lengths.	0		6	dB
Receive Clock Jitter	DS3 mode with 10 Hz – 400 kHz				
	a) Normal receive mode b) Remote loopback mode			0.1 0.06	U <sub>lpp</sub> U <sub>lpp</sub>
Interfering Tone Tolerance (see Note 5)	Maximum ratio of Interference Power to Signal Power for BER < 10 <sup>-8</sup>				
	a) With 0ft cable from DSX		-9		dB
	b) With 450ft cable from DSX		-10		dB

- Note 1: Signal source should meet DS3 template of ANSI-T102.1993 Figure 4 and STS-1 template of ANSI-T102.1993 Figure 5. Loss characteristics of the WE728A or RG59B cable should be better than Figure C2 of ANSI-T102.1993.
- Note 2: Min spec corresponds to minimum DSX amplitude, 5.5dB of cable loss (450ft) and 6dB of flat attenuation. Error-free receiver performance is guaranteed for up to 600ft of cable from DSX cross-connect. Typical part can handle up to 900ft.
- Note 3: Min spec corresponds to amplitude of 425mVpk at DSX, 5.5dB of cable loss (450ft) and 20dB of flat attenuation. In monitor mode, interfering tone performance is not guaranteed.
- Note 4: In this mode, no noise, jitter, or interfering tone impairments should be added for guaranteed receiver performance.
- Note 5: Interfering signal is a non-synchronous sinusoidal tone of 22.368MHz for DS3 or 25.92MHz for STS-1. Data is a PRBS15 (2<sup>15</sup>-1) pattern.

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**3-port E3/DS3/STS-1 LIU**  
**with Jitter Attenuator**

**ELECTRICAL SPECIFICATIONS** (continued)

**E3 – RECEIVER (Transformer-coupled)**

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Peak Differential Input Amplitude, LINP <sub>x</sub> and LINN <sub>x</sub>	MON=0 (See Note 1)	120		1200	mVpk
	MON=1 (See Note 2)	25		100	mVpk
Flat-loss Tolerance	MON=0. All valid cable lengths.	0		6	dB
Receive Clock Jitter	With 100Hz-800kHz filter: a) Normal receive mode b) Remote loopback mode			0.1 0.06	UIpp UIpp
Interfering Tone Tolerance (see Note 3)	Maximum ratio of Interference Power to Signal Power for BER < 10 <sup>-8</sup> a) With 0ft cable b) With 900ft cable		-9 -10		dB dB

Note 1: Min spec corresponds to signal amplitude of 950mVpk at source, 12dB of cable loss (1100ft) and 6dB of flat attenuation. Error-free receiver performance is guaranteed for all cable less than 1100ft. Typical part can handle up to 1350ft.

Note 2: Min spec corresponds to signal amplitude of 1000mVpk at source, 12dB of cable loss (1100ft) and 20dB of flat attenuation. In monitor mode, interfering tone performance is not guaranteed.

Note 3: Interfering signal is a non-synchronous E3 signal of the specified power level below the desired E3 signal. Both data and interfering signals are PRBS23 (2<sup>23</sup>-1) pattern.

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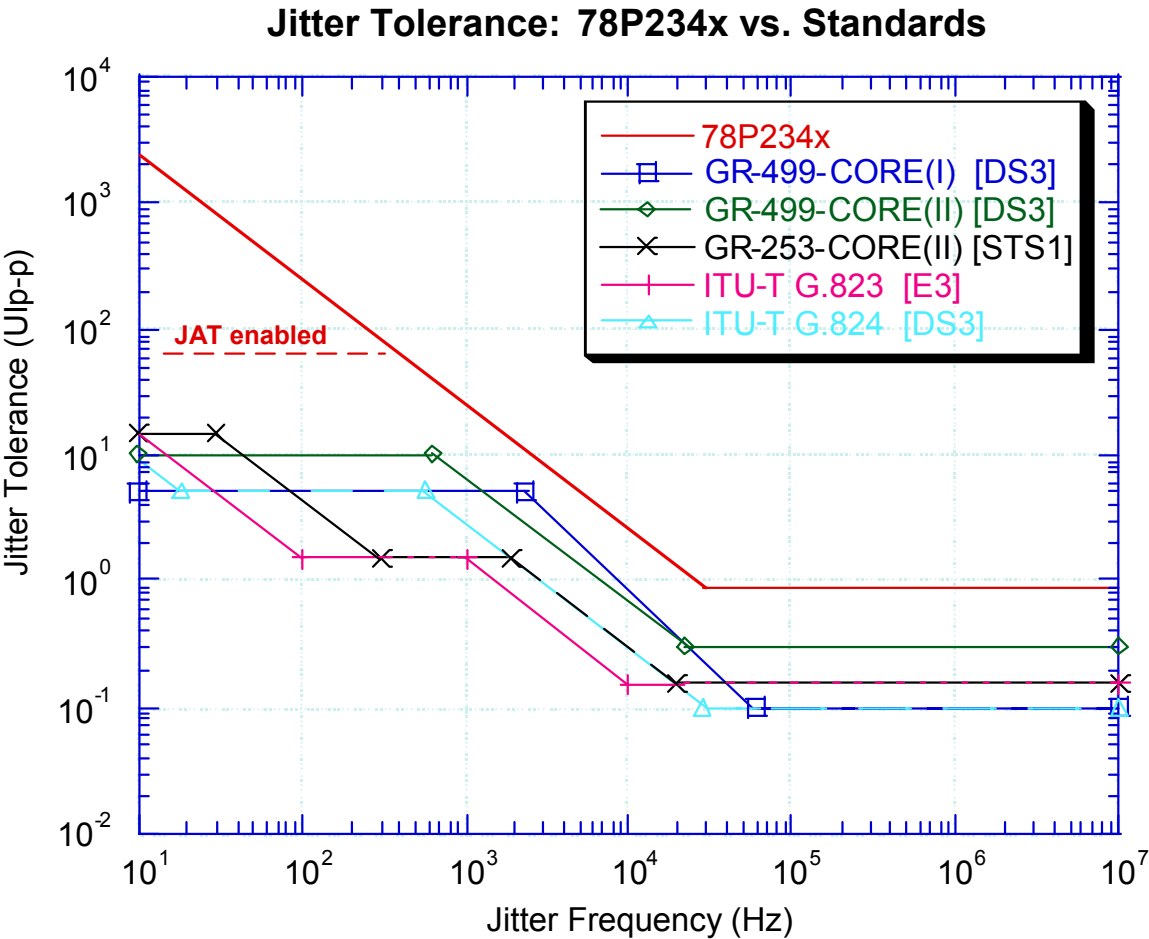
ELECTRICAL SPECIFICATIONS

(continued)

RECEIVER JITTER TOLERANCE

The 78P2343JAT receive jitter tolerance exceeds all specifications as shown on the graph below.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Receiver High Frequency Jitter Tolerance	> 60 kHz	0.75			UIpp



# 78P2343JAT

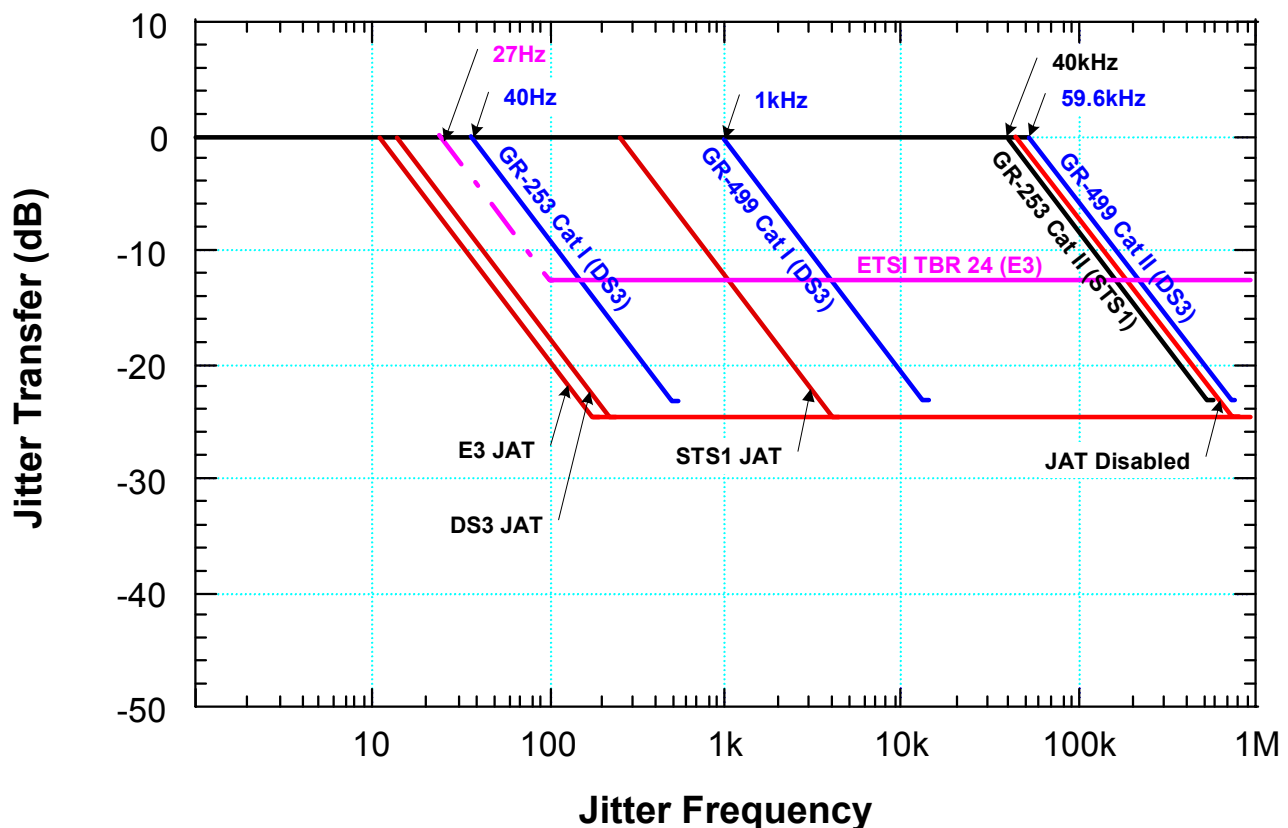
## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### ELECTRICAL SPECIFICATIONS (continued)

#### RECEIVER JITTER TRANSFER FUNCTION

The receiver clock recovery loop characteristics are such that the receiver has the following transfer function. When the Jitter Attenuator (JAT) is enabled in the receive or transmit path, the receiver or transmitter will exhibit a jitter transfer as shown in the graph and table below. Jitter Attenuator operation is guaranteed through digital scan testing. The actual jitter transfer is guaranteed by logic design and is not tested during production testing.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Receiver Jitter transfer function	Below Fc			0.1	dB
Receiver Jitter Bandwidth, Fc	At -3dB point JABW= 0, E3 mode (default) JABW= 1, E3 mode			13 188	Hz
	JABW= 0, DS3 mode (default) JABW= 1, DS3 mode			17 245	
	JABW= 0, STS1 mode JABW= 1, STS1 mode (default)			20 283	
	JAEN= 0, JAT disabled			55	
Jitter transfer function roll-off	After Fc	20			dB per decade



# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

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#### APPLICATION INFORMATION

##### EXTERNAL COMPONENTS:

COMPONENT	PIN(S)	VALUE	UNITS	TOLERANCE
Receiver Termination Resistor	LINPx LINNx	84.5	$\Omega$	1%
Transmitter Termination Resistor	LOUTPx LOUTNx	402	$\Omega$	1%

##### TRANSFORMER SPECIFICATIONS:

COMPONENT	VALUE	UNITS	TOLERANCE
Turns Ratio for the Receiver		1:1	
Turns Ratio for the Transmitter (center-tapped)		1:2CT	

Suggested Manufacturer: Pulse, TDK, Halo

##### THERMAL INFORMATION

PACKAGE	CONDITIONS	$\Theta_{ja}$ (°C/W)
Standard 100-pin JEDEC LQFP (78P2343JAT-IGT)		46
Exposed Pad 100-pin JEDEC LQFP (78P2343JAT-IEL)	No forced air, Die attach pad soldered to PCB	24.8

##### SCHEMATICS

For the latest typical application schematics, please check TDK Semiconductor's website or contact your local sales representative for the latest application note(s) and/or demo board manuals.



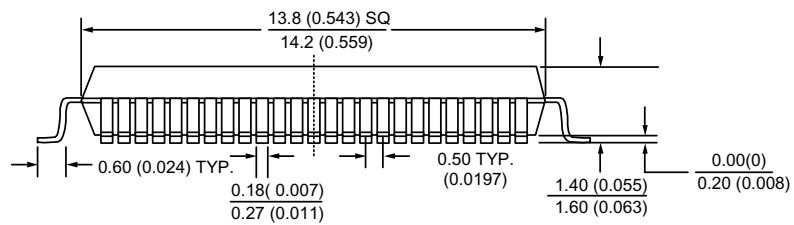
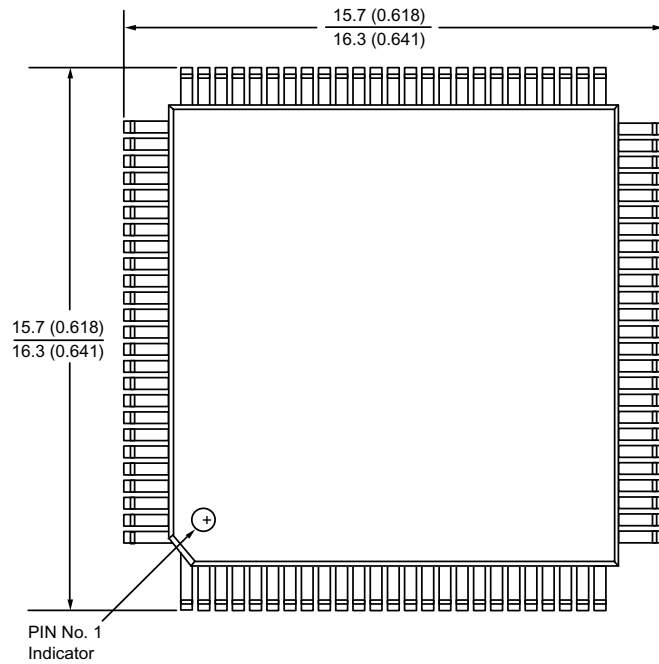
# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

#### MECHANICAL SPECIFICATIONS

(Top View)



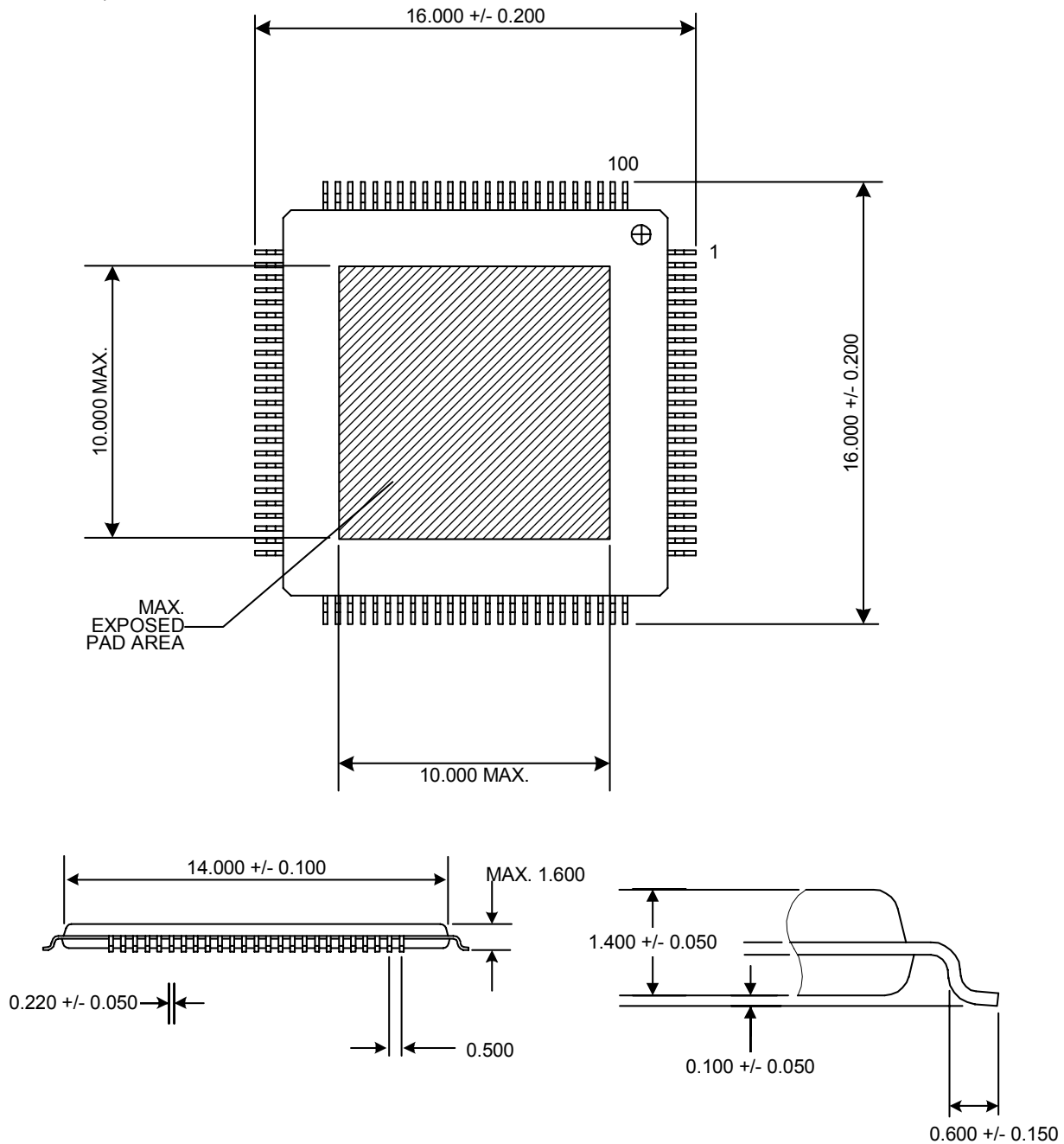
78P2343JAT-IGT Mechanical Specification  
100-pin TQFP (JEDEC LQFP)

## 78P2343JAT

### 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

## MECHANICAL SPECIFICATIONS

(Bottom View)



## 78P2343JAT-IEL Mechanical Specification

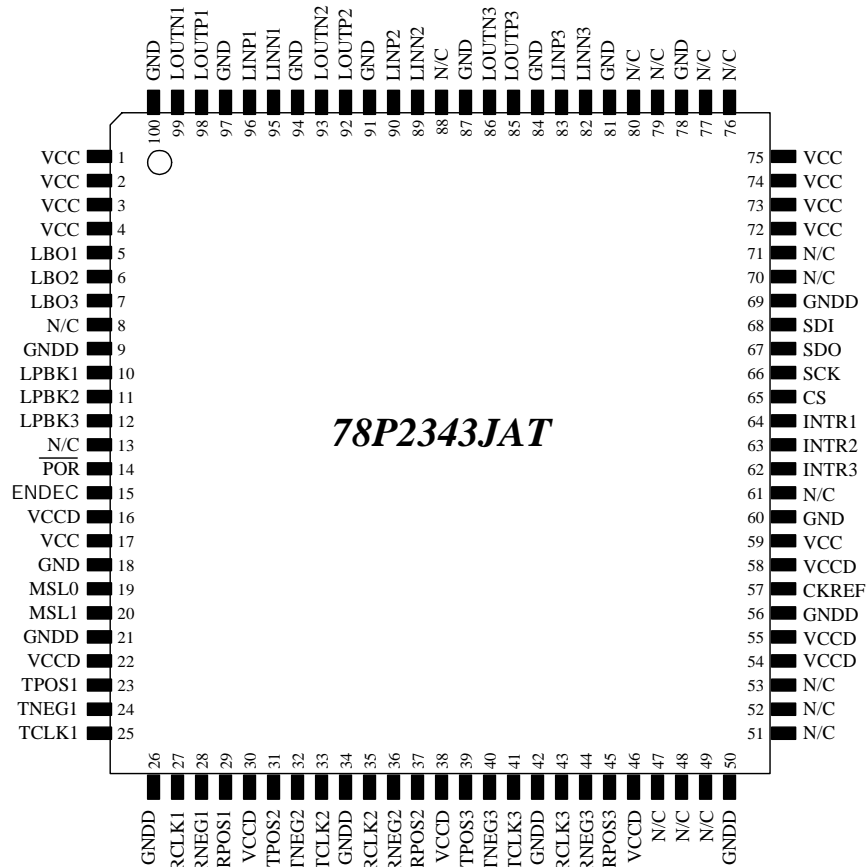
# 78P2343JAT

## 3-port E3/DS3/STS-1 LIU with Jitter Attenuator

### PACKAGE INFORMATION

#### Pin-Out

(Top View)



100-pin TQFP (JEDEC LQFP)

### ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
100-pin JEDEC LQFP	78P2343JAT-IGT	78P2343JAT-IGT
100-pin JEDEC LQFP, <b>No Jitter Attenuator</b>	78P2343-IGT	78P2343-IGT
100-pin JEDEC LQFP w/ Exposed Solder Pad	78P2343JAT-IEL	78P2343JAT-IEL
100-pin JEDEC LQFP w/ Exposed Solder Pad, <b>No Jitter Attenuator</b>	78P2343-IEL	78P2343-IEL
Tape & Reel option	append 'R'	n/a
Lead-free option	append 'IF'	append 'IF'

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## 3-port E3/DS3/STS-1 LIU

### with Jitter Attenuator

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#### REVISION HISTORY

Revision Date:	Revision Description:
June 24, 2002	<ul style="list-style-type: none"><li>▪ ENDEC pin addition (pin 15) and default change to ENDEC bit</li><li>▪ Changed LBOx pin functionality by adding TXEN &amp; PDX control</li><li>▪ Corrected LPBKx pin description and Intrinsic Transmit Jitter spec.</li></ul>
July 10, 2003	<p>Changed to Preliminary Status</p> <ul style="list-style-type: none"><li>▪ Added Exposed Pad package option (-IEL) and Lead-free option (/ F)</li><li>▪ Updated Receive Jitter Tolerance and Jitter Transfer graphs</li><li>▪ Removed SGHI bit definition</li><li>▪ Updated Internal Power on Reset description</li><li>▪ Added pin type CIT</li><li>▪ Updated timing diagrams &amp; e-spec table values</li><li>▪ Changed recommended Rx / Tx termination resistor values to 84.5 / 402 ohm respectively</li><li>▪ Added Thermal Information section</li></ul>

**Preliminary Data Sheet:** This Preliminary Data Sheet describes a product not completely released to production. The specifications are based on preliminary evaluations and may not be accurate. Samples of the described product are available and limited quantities can be purchased. TDK Semiconductor Corporation should be consulted contacted for contacted to obtain the most current up-to-date information about the product.

If and when manufactured and sold, this product is sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement and limitation of liability. TDK Semiconductor Corporation (TSC) reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that a data sheet is current before placing orders. TSC assumes no liability for applications assistance.

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