

# 54ACT11828, 74ACT11828 10-BIT BUFFERS/BUS DRIVERS WITH 3-STATE OUTPUTS

SCAS092 – D3387, APRIL 1993

- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations to Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs

## description

These 10-bit buffers/bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input NOR such that if either  $\overline{G1}$  or  $\overline{G2}$  is high, all ten outputs are in the high-impedance state.

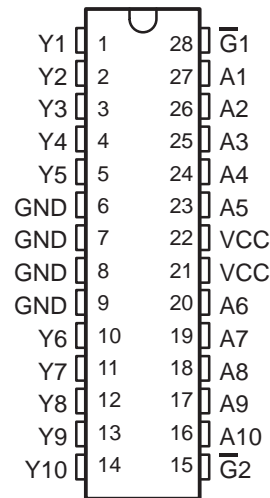
The 'ACT11828 provides inverted data.

The 54ACT11828 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11828 is characterized for operation from – 40°C to 85°C.

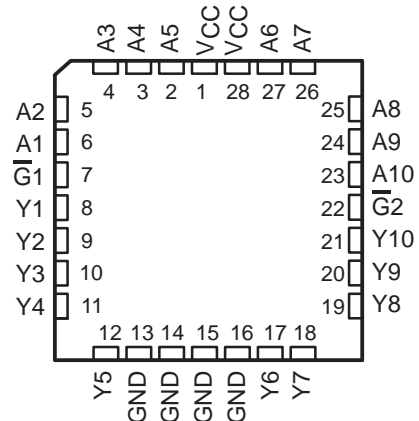
FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{G1}$	$\overline{G2}$	A	
L	L	H	L
L	L	L	H
X	H	X	Z
H	X	X	Z

54ACT11828 . . . JT PACKAGE  
74ACT11828 . . . DW PACKAGE  
(TOP VIEW)



54ACT11828 . . . FK PACKAGE  
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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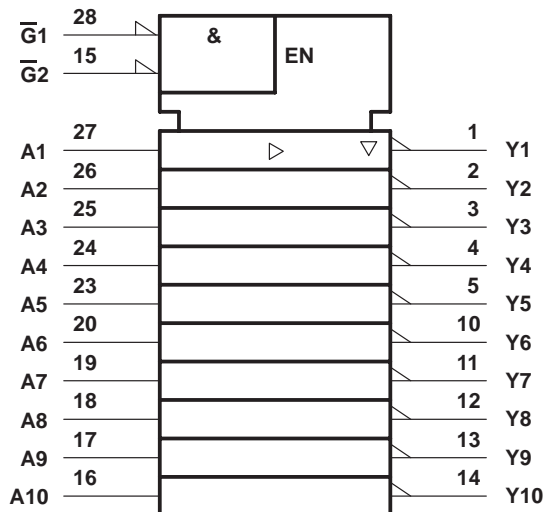
# 54ACT11828, 74ACT11828

## 10-BIT BUFFERS/BUS DRIVERS

### WITH 3-STATE OUTPUTS

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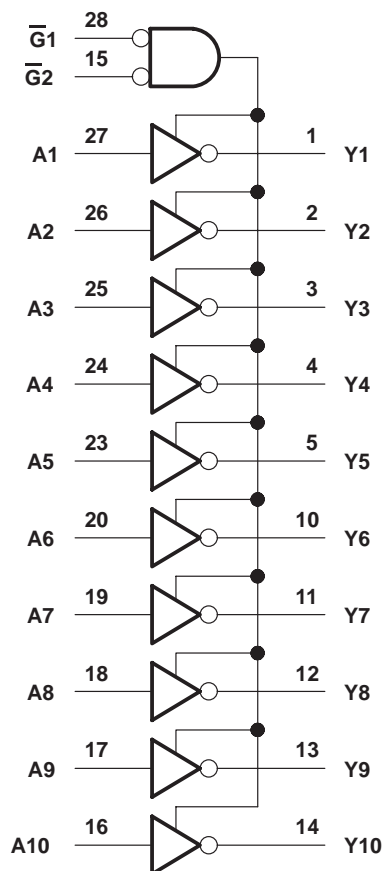
#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 250$ mA
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

		54ACT11828		74ACT11828		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–24	mA
$I_{OL}$	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			54ACT11828		74ACT11828		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24\ \text{mA}$	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50\ \text{mA}^\dagger$	5.5 V				3.85				
	$I_{OH} = -75\ \text{mA}^\dagger$	5.5 V						3.85		
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24\ \text{mA}$	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50\ \text{mA}^\dagger$	5.5 V					1.65			
	$I_{OL} = 75\ \text{mA}^\dagger$	5.5 V							1.65	
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.5$		$\pm 10$		$\pm 5$	$\mu\text{A}$
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V			0.9		1		1	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4.5						pF
$C_o$	$V_I = V_{CC}$ or GND	5 V		12						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to  $V_{CC}$ .

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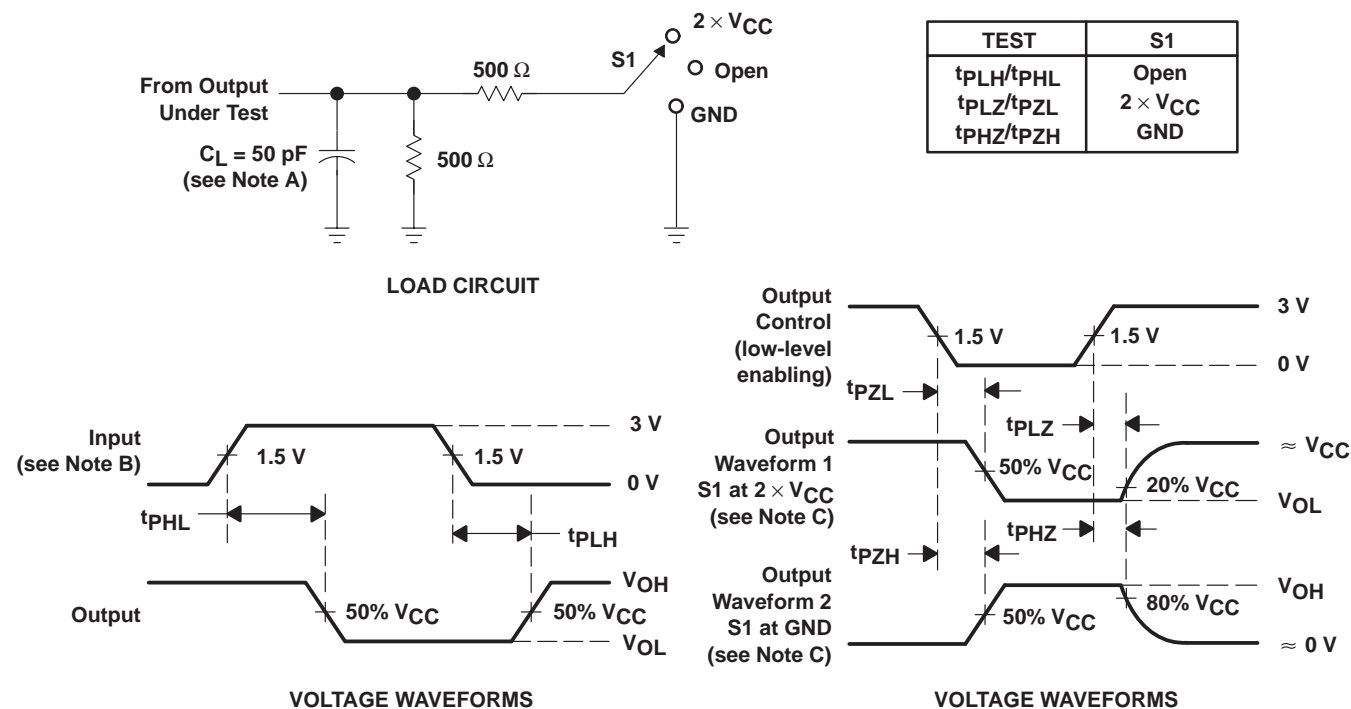
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11828		74ACT11828		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	1.9	5.6	8.3	1.9	10.9	1.9	10.2	ns
$t_{PHL}$			5.2	8	10.3	5.2	12.4	5.2	11.7	
$t_{PZH}$	$\bar{G}1$ or $\bar{G}2$	Y	2.9	7	9.9	2.9	13	2.9	12.1	ns
$t_{PZL}$			3.4	8.3	11.4	3.4	15.8	3.4	14.7	
$t_{PHZ}$	$\bar{G}1$ or $\bar{G}2$	Y	6	9	11.3	6	12.9	6	12.3	ns
$t_{PLZ}$			5.9	8.5	10.9	5.9	12.3	5.9	11.7	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	37	pF
		Outputs disabled		11	

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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