

## CMOS Hex Gate

Four Inverters, One 2-Input NOR Gate, One 2-Input NAND Gate

### Features:

- Pin 7 NOR input positioned adjacent to  $V_{SS}$  for easy use of gate as an inverter
- Pin 15 NAND input positioned adjacent to  $V_{DD}$  for easy use of gate as an inverter
- Standard symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range: 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4572UB Hex Gate provides the system designer with direct implementation of inverter, NAND, and NOR functions and supplements the existing family of CMOS gates.

The CD4572UB devices meet all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

The CD4572UB types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

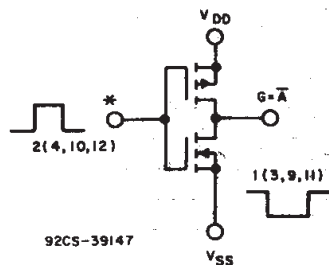
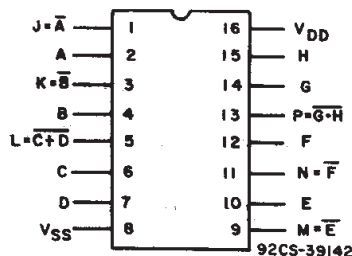
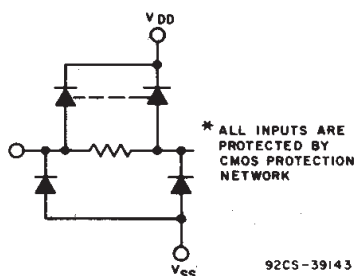


Fig. 1 - Schematic diagram of one of four identical inverters.

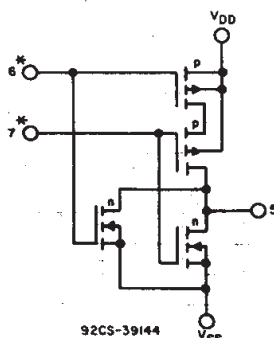


Fig. 2 - Schematic diagram for the 2-input NOR gate.

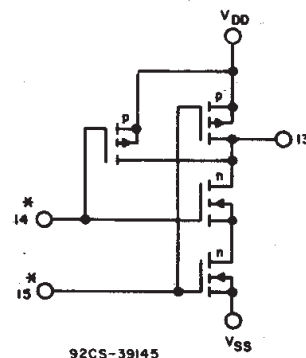


Fig. 3 - Schematic diagram for the 2-input NAND gate.

# CD4572UB Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal)

-0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to  $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT

$\pm 10mA$

POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ C$  to  $+100^\circ C$

500mW

For  $T_A = +100^\circ C$  to  $+125^\circ C$

Derate Linearity at 12mW/ $^\circ C$  to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$

100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ )

$-55^\circ C$  to  $+125^\circ C$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ )

$-65^\circ C$  to  $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79mm$ ) from case for 10s max

$+265^\circ C$

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ )	3	18	V

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)								
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0, 5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA
	—	0, 10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0, 15	15	1	1	30	30	—	0.01	1	
	—	0, 20	20	5	5	150	150	—	0.02	5	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0, 5	5	4.95				4.95	5	—	
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5	1				—	—	1	
	1, 9	—	10	2				—	—	2	
	1.5, 13.5	—	15	2.5				—	—	2.5	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5	4				4	—	—	
	1, 9	—	10	8				8	—	—	
	1.5, 13.5	—	15	12.5				12.5	—	—	
Input Current, I <sub>IN</sub> Max.	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

# CD4572UB Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ\text{C}$ , Input  $t_r, t_f=20\text{ ns}$ ,  $C_L=50\text{ pF}$ ,  $R_L=200\text{ K}\Omega$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
		$V_{DD}$ (V)	Min.	Typ.	Max.	
Propagation Delay Time	$t_{PHL}, t_{PLH}$	5	—	100	200	ns
		10	—	55	110	
		15	—	40	85	
Transition Time	$t_{THL}, t_{TLH}$	5	—	100	200	
		10	—	50	100	
		15	—	40	80	
Input Capacitance	$C_{in}$	Any Input	—	10	15	pF

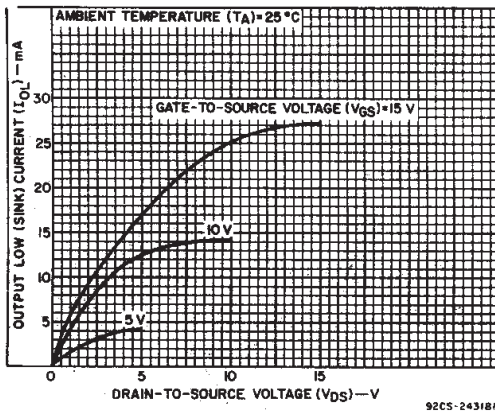


Fig. 4 - Typical output low (sink) current characteristics.

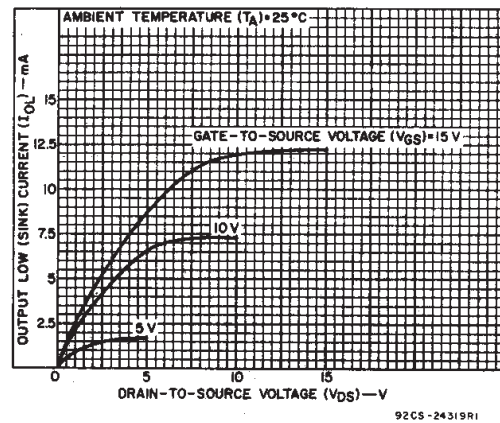


Fig. 5 - Minimum output low (sink) current characteristics.

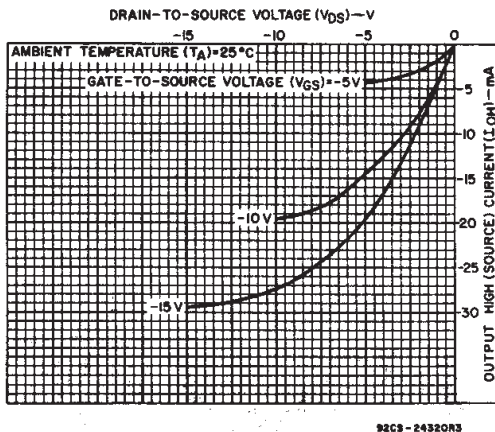


Fig. 6 - Typical output high (source) current characteristics.

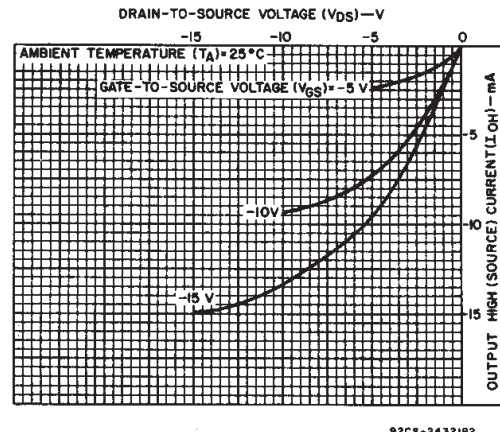


Fig. 7 - Minimum output high (source) current characteristics.

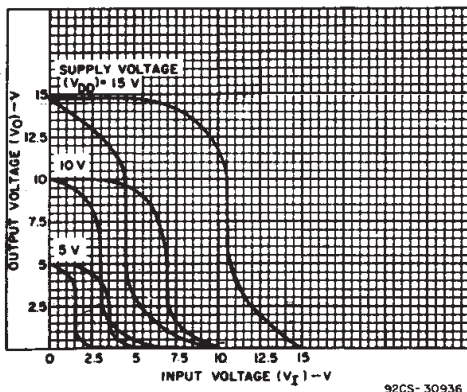


Fig. 8 - Minimum and maximum inverter voltage transfer characteristics.

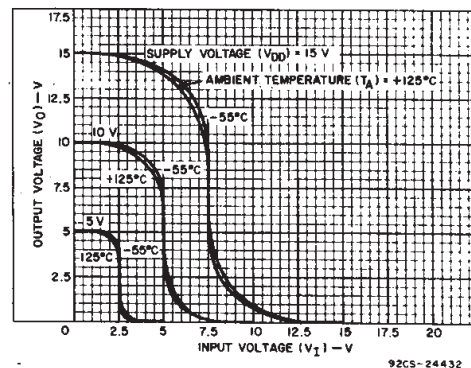


Fig. 9 - Typical inverter voltage transfer characteristics as a function of temperature.

# CD4572UB Types

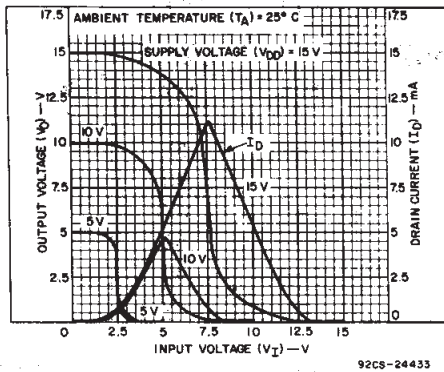


Fig. 10 - Typical inverter current and voltage transfer characteristics.

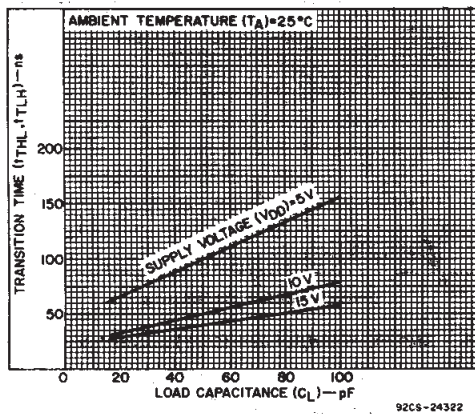


Fig. 12 - Typical transition time vs. load capacitance.

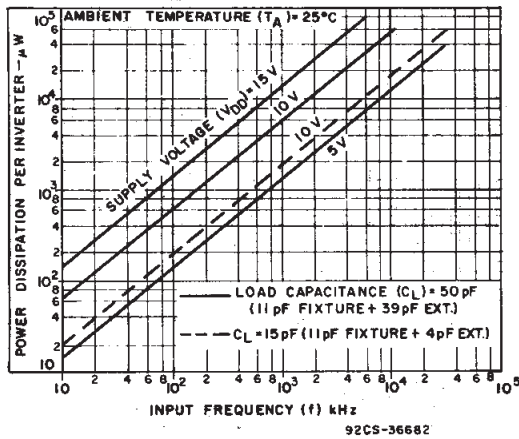


Fig. 14 - Typical dynamic power dissipation vs. frequency.

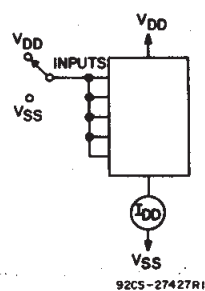


Fig. 16 - Quiescent device current test circuit.

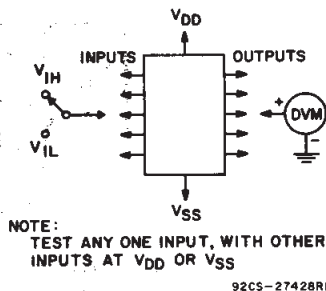


Fig. 17 - Noise immunity test circuit.

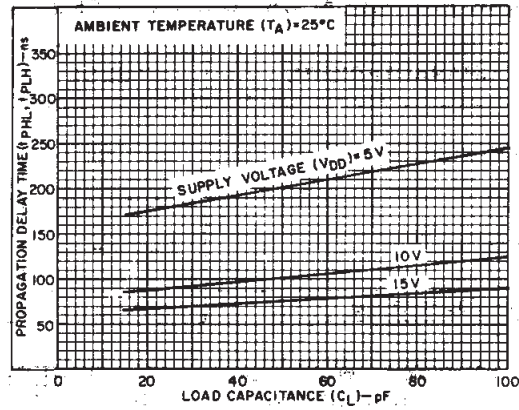


Fig. 11 - Typical propagation delay time as a function of load capacitance.

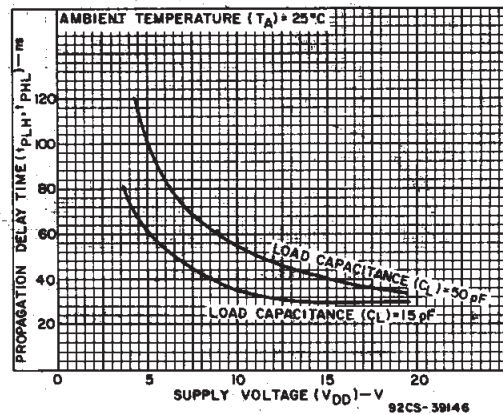


Fig. 13 - Typical propagation delay time vs. supply voltage.

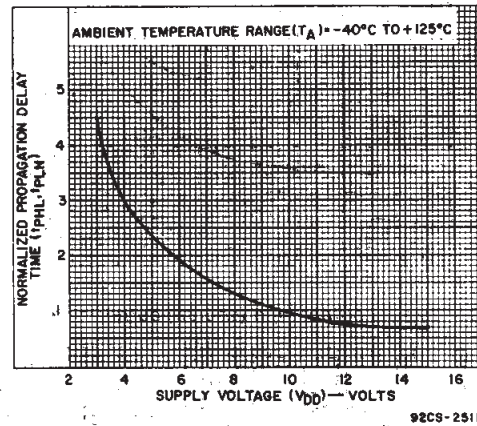


Fig. 15 - Variation of normalized propagation delay time ( $t_{PLH}$  and  $t_{PLH}$ ) with supply voltage.

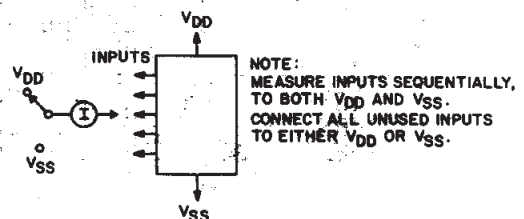


Fig. 18 - Input leakage current test circuit.

## CD4572UB Types

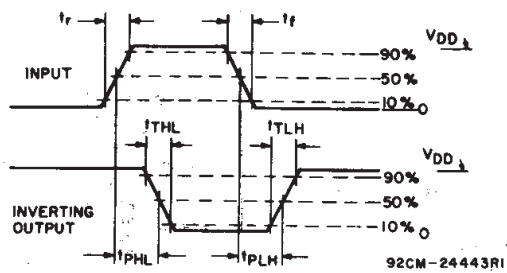
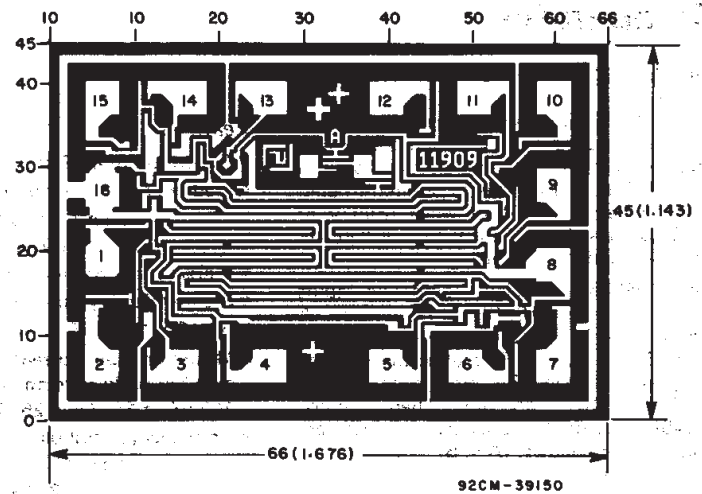


Fig. 19 - Transition times and propagation delay times, combination logic.

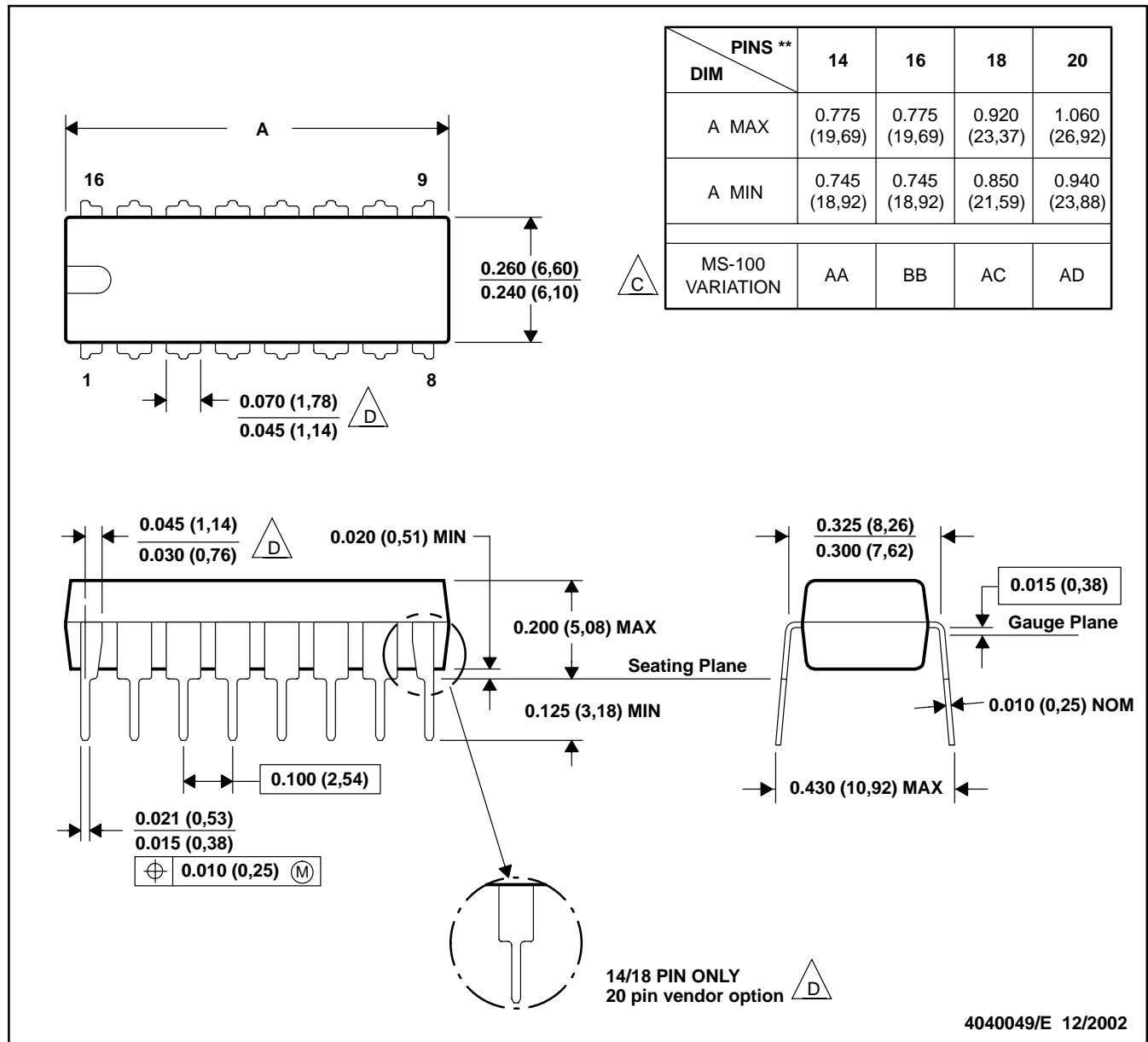


Dimensions and pad layout for CD4572UBH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**N (R-PDIP-T\*\*)**

16 PINS SHOWN

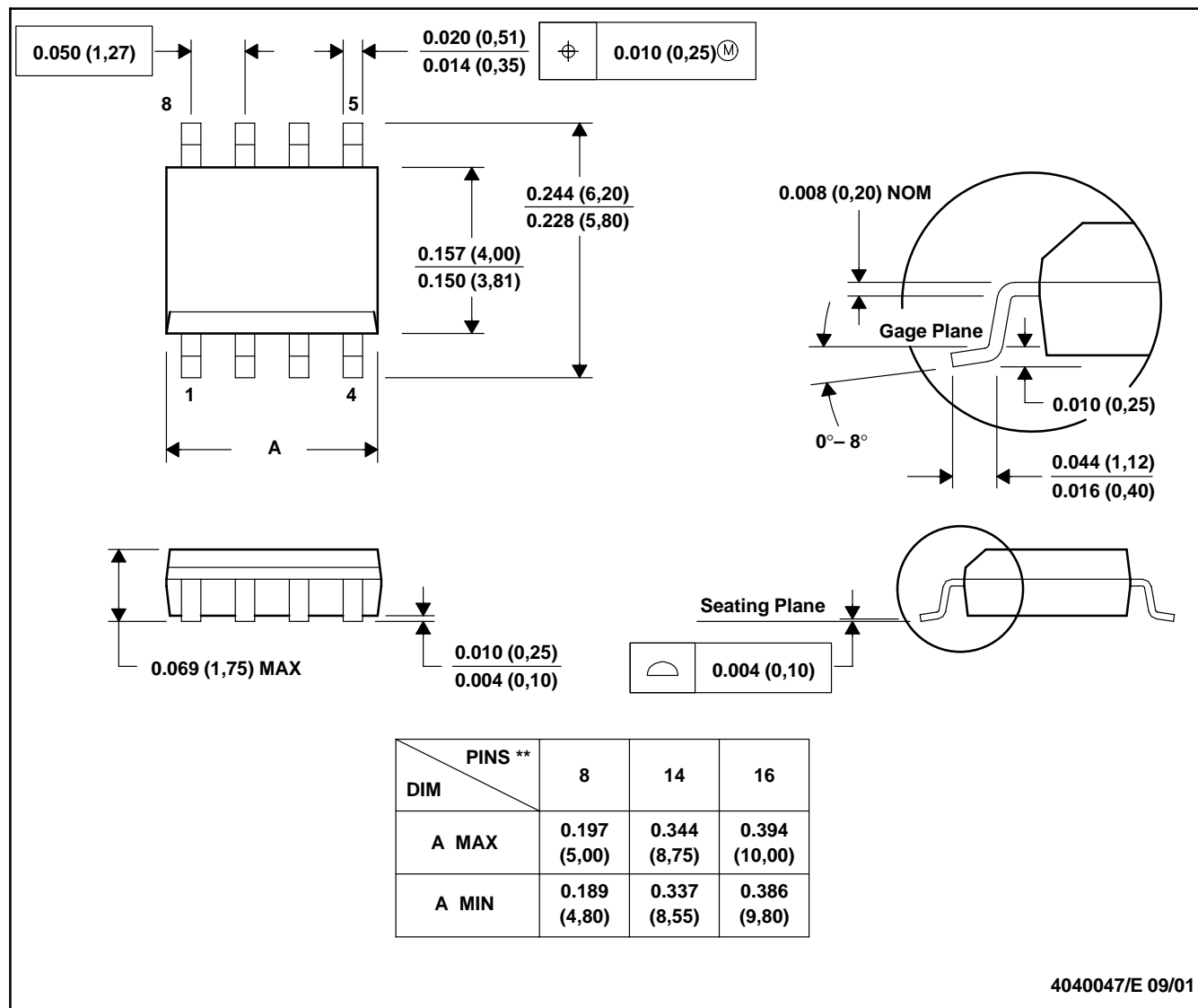
**PLASTIC DUAL-IN-LINE PACKAGE**

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

**D (R-PDSO-G\*\*)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

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