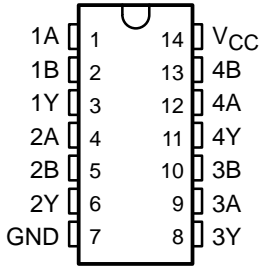


CD54ACT08, CD74ACT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCHS312B – JANUARY 2001 – REVISED JUNE 2002

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- Buffered Inputs
- ± 24 -mA Output Drive Current
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT08 . . . F PACKAGE
CD74ACT08 . . . E OR M PACKAGE
(TOP VIEW)



description

The 'ACT08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74ACT08E	CD74ACT08E
	SOIC – M	Tube	CD74ACT08M	ACT08M
		Tape and reel	CD74ACT08M96	
	CDIP – F	Tube	CD54ACT08F3A	CD54ACT08F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram, each gate (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CD54ACT08, CD74ACT08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCHS312B – JANUARY 2001 – REVISED JUNE 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	80°C/W
M package	86°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	$T_A = 25^\circ\text{C}$		–40°C TO 85°C		–55°C TO 125°C		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		2		V
V_{IL} Low-level input voltage		0.8		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–24		–24	mA
I_{OL} Low-level output current		24		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$		–40°C TO 85°C		–55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4		4.4		4.4		V
		$I_{OH} = -24\ \text{mA}$	4.5 V	3.94		3.8		3.7		
		$I_{OH} = -50\ \text{mA}^\ddagger$	5.5 V					3.85		
		$I_{OH} = -75\ \text{mA}^\ddagger$	5.5 V			3.85				
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 50\ \mu\text{A}$	4.5 V		0.1		0.1		0.1	V
		$I_{OL} = 24\ \text{mA}$	4.5 V		0.36		0.44		0.5	
		$I_{OL} = 50\ \text{mA}^\ddagger$	5.5 V						1.65	
		$I_{OL} = 75\ \text{mA}^\ddagger$	5.5 V				1.65			
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5 V		4		40		80	μA
ΔI_{CC}	$V_I = V_{CC} - 2.1\ \text{V}$		4.5 V to 5.5 V		2.4		2.8		3	mA
C_i					10		10		10	pF

[‡] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

CD54ACT08, CD74ACT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCHS312B – JANUARY 2001 – REVISED JUNE 2002

ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
A or B	0.3

Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C		–55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3.3	11.7	3.2	12.9	ns
t_{PHL}			3.3	11.7	3.2	12.9	

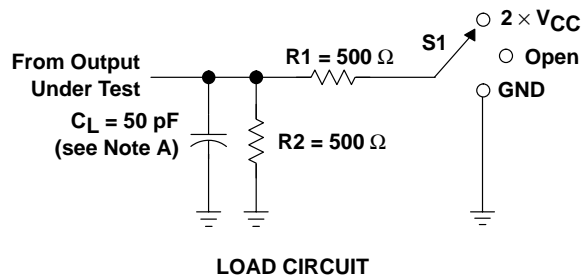
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	50	pF

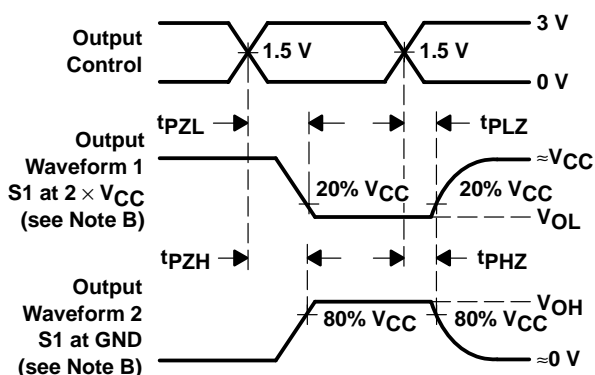
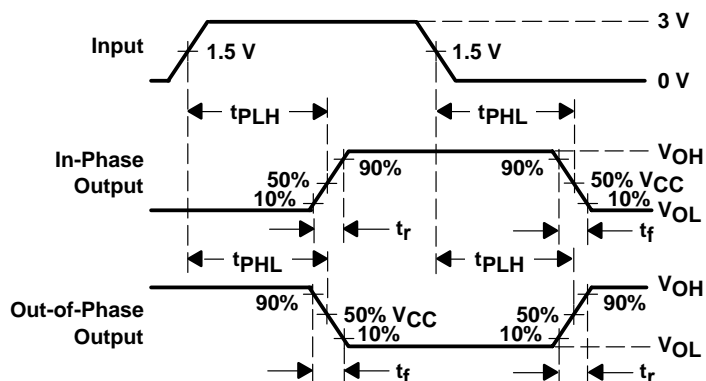
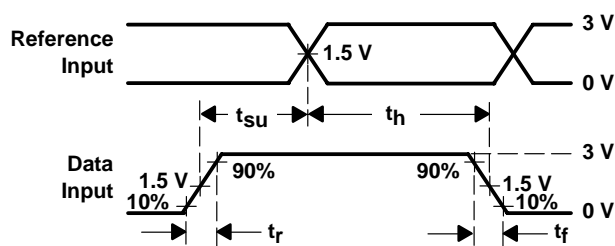
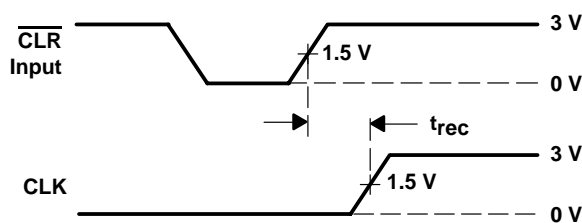
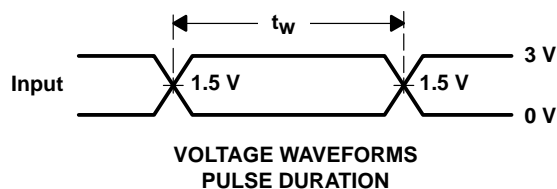
CD54ACT08, CD74ACT08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCHS312B – JANUARY 2001 – REVISED JUNE 2002

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265