

# CD54HC4538, CD74HC4538, CD74HCT4538

## High Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrator

### Features

- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of  $R_X$ ,  $C_X$
- Triggering from the Leading or Trailing Edge
- Q and  $\bar{Q}$  Buffered Outputs Available
- Separate Resets
- Wide Range of Output-Pulse Widths
- Schmitt Trigger Input on A and  $\bar{B}$  Inputs
- Retrigger Time is Independent of  $C_X$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD54HC4538, CD74HC4538 and CD74HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor ( $R_X$ ) and an external capacitor ( $C_X$ ) control the timing and the accuracy for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of  $R_X$  and  $C_X$ .

Leading-edge triggering (A) and trailing edge triggering ( $\bar{B}$ ) inputs are provided for triggering from either edge of the input pulse. An unused "A" input should be tied to GND and an unused  $\bar{B}$  should be tied to  $V_{CC}$ . On power up the IC is reset. Unused resets and sections must be terminated. In normal operation the circuit retriggers on the application of each new trigger pulse. To operate in the non-triggerable mode  $\bar{Q}$  is connected to  $\bar{B}$  when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering ( $\bar{B}$ ) is used. The period ( $\tau$ ) can be calculated from  $\tau = (0.7) R_X C_X$ ;  $R_{MIN}$  is 5k $\Omega$ .  $C_{MIN}$  is 0pF.

### Ordering Information

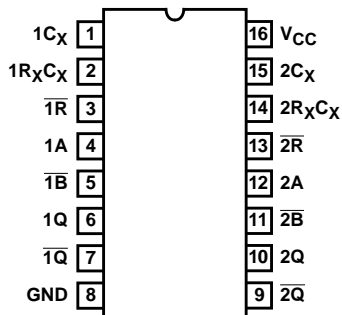
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54HC4538F	-55 to 125	16 Ld Cerdip	F16.3
CD74HC4538E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT4538E	-55 to 125	16 Ld PDIP	E16.3
CD74HC4538M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT4538M	-55 to 125	16 Ld SOIC	M16.15

#### NOTES:

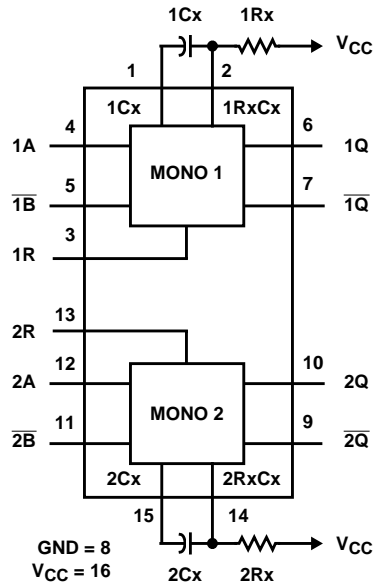
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout

CD54HC4538, CD74HC4538, CD74HCT4538  
(PDIP, SOIC, Cerdip)  
TOP VIEW



# Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS	
$\bar{R}$	A	$\bar{B}$	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	$\downarrow$	$\text{One High Level Pulse}$	$\text{One Low Level Pulse}$
H	$\uparrow$	H	$\text{One High Level Pulse}$	$\text{One Low Level Pulse}$

NOTE: H = High Level, L = Low Level,  $\uparrow$  = Transition from Low to High,  $\downarrow$  = Transition from High to Low,  $\text{One High Level Pulse}$ ,  $\text{One Low Level Pulse}$ , X = Irrelevant.

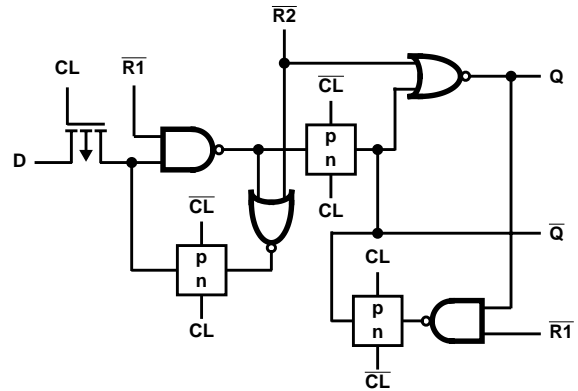


FIGURE 1. FF DETAIL

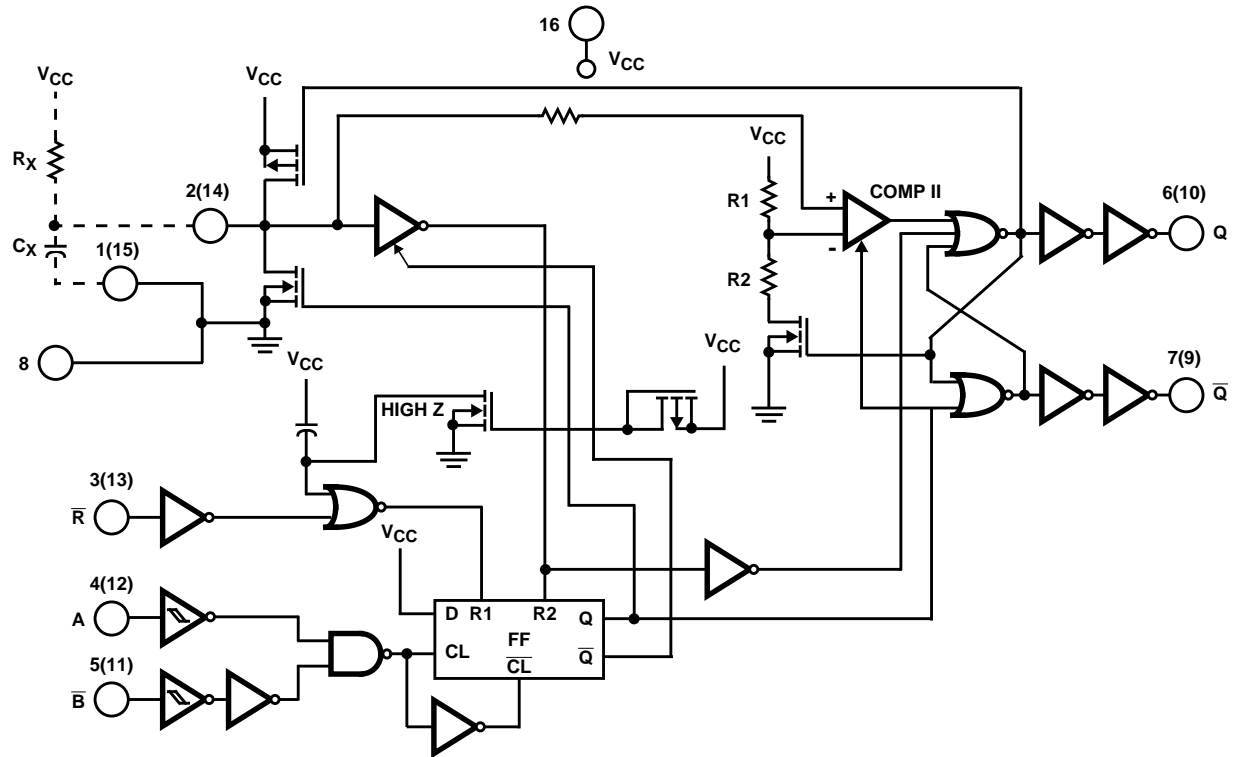


FIGURE 2. LOGIC DIAGRAM (1 MONO)

FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V <sub>CC</sub> TO TERMINAL NUMBER		GND TO TERMINAL NUMBER		INPUT PULSE TO TERMINAL NUMBER		OTHER CONNECTIONS	
	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:

- A retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T) after application of the last trigger pulse.
- A non-retriggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.



FIGURE 3. INPUT PULSE TRAIN

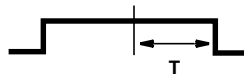


FIGURE 4. RETRIGGERABLE MODE  
PULSE WIDTH (A MODE)

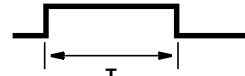


FIGURE 5. NON-RETRIGGERABLE MODE  
PULSE WIDTH  
(A MODE)

# CD54HC4538, CD74HC4538, CD74HCT4538

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 7)	$\theta_{JA}$ ( $^{\circ}C/W$ )	$\theta_{JC}$ ( $^{\circ}C/W$ )
PDIP Package . . . . .	90	N/A
SOIC Package . . . . .	160	N/A
CERDIP Package . . . . .	130	55
Maximum Junction Temperature . . . . .	150 $^{\circ}C$	
Maximum Storage Temperature Range . . . . .	-65 $^{\circ}C$ to 150 $^{\circ}C$	
Maximum Lead Temperature (Soldering 10s) . . . . .	300 $^{\circ}C$	
(SOIC - Lead Tips Only)		

## Operating Conditions

Temperature Range, $T_A$	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$ (Note 5)	
HC Types	.2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$	0V to $V_{CC}$
Input Rise and Fall Times, $t_r$ , $t_f$	
Reset Input:	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)
Trigger Inputs A or B:	
2V	Unlimited (Max)
4.5V	Unlimited (Max)
6V	Unlimited (Max)
External Timing Resistor, $R_X$ (Note 6)	.5k $\Omega$ (Min)
External Timing Capacitor, $C_X$ (Note 6)	0 (Min)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTES:

- Unless otherwise specified, all voltages are referenced to ground.
- The maximum allowable values of  $R_X$  and  $C_X$  are a function of leakage of capacitor  $C_X$ , the leakage of the HC4538, and leakage due to board layout and surface resistance. Values of  $R_X$  and  $C_X$  should be chosen so that the maximum current into pin 2 or pin 14 is 30mA. Susceptibility to externally induced noise signals may occur for  $R_X > 1M\Omega$ .
- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V

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**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current A, B, R	I <sub>I</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Input Leakage Current R <sub>X</sub> C <sub>X</sub> (Note 9)			-	6	-	-	±0.05	-	±0.5	-	±0.5	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
Active Device Current Q = High & Pins 2, 14 at V <sub>CC</sub> /4	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	0.6	-	0.8	-	1	mA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA
Input Leakage Current R <sub>X</sub> C <sub>X</sub> (Note 9)			-	5.5	-	-	±0.05	-	±0.5	-	±0.5	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Active Device Current Q = High & Pins 2, 14 at V <sub>CC</sub> /4	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	0.6	-	0.8	-	1	mA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 8)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

**NOTES:**

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.
- When testing I<sub>IL</sub> the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from V<sub>DD</sub> to the test pin will cause a current far exceeding the specification.

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**HCT Input Loading Table**

INPUT	UNIT LOADS
All	0.5

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Table, e.g. 360 $\mu$ A max at 25°C.

**Prerequisite for Switching Specifications**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Input Pulse Widths A, $\bar{B}$	t <sub>WH</sub> , t <sub>WL</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
$\bar{R}$	t <sub>WL</sub>	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Reset Recovery Time	t <sub>REC</sub>	2	5	-	-	5	-	-	5	-	-	ns
		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t <sub>rr</sub>	5	-	175	-	-	-	-	-	-	-	ns
HCT TYPES												
Input Pulse Widths A, $\bar{B}$	t <sub>WH</sub> , t <sub>WL</sub>	4.5	16	-	-	20	-	-	24	-	-	ns
		$\bar{R}$	t <sub>WL</sub>	4.5	20	-	-	25	-	-	30	-
Reset Recovery Time	t <sub>REC</sub>	4.5	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t <sub>rr</sub>	5	-	175	-	-	-	-	-	-	-	ns

**CD54HC4538, CD74HC4538, CD74HCT4538**

**Switching Specifications**  $C_L = 50\text{pF}$ , Input  $t_r, t_f = 6\text{ns}$ ,  $R_X = 10\text{k}\Omega$ ,  $C_X = 0$

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay A, $\overline{B}$ to Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C <sub>L</sub> = 15pF	5	-	21	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	43	-	54	-	64	ns
A, $\overline{B}$ to $\overline{Q}$	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C <sub>L</sub> = 15pF	5	-	21	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	43	-	54	-	64	ns
$\overline{R}$ to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C <sub>L</sub> = 15pF	5	-	21	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	43	-	54	-	64	ns
$\overline{R}$ to $\overline{Q}$	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C <sub>L</sub> = 15pF	5	-	21	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	43	-	54	-	64	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Pulse Width R <sub>X</sub> = 10k, C <sub>X</sub> = 0.1μF	τ	C <sub>L</sub> = 50pF	3	0.64	-	0.78	0.612	0.812	0.605	0.819	ms
			5	0.63	-	0.77	0.602	0.798	0.595	0.805	ms
Output Pulse Width Match, Same Package	-	-		-	±1	-	-	-	-	-	%
Power Dissipation Capacitance	C <sub>PD</sub>	C <sub>L</sub> = 15pF	5	-	136	-	-	-	-	-	pF
Input Capacitance	C <sub>I</sub>	C <sub>L</sub> = 50pF	-	10	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay A, $\overline{B}$ to Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	5	-	23	-	-	-	-	-	ns
A, $\overline{B}$ to $\overline{Q}$	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	5	-	23	-	-	-	-	-	ns
$\overline{R}$ to Q	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	40	-	50	-	60	ns
		C <sub>L</sub> = 15pF	5	-	17	-	-	-	-	-	ns

# **CD54HC4538, CD74HC4538, CD74HCT4538**

## **Switching Specifications** $C_L = 50\text{pF}$ , Input $t_r, t_f = 6\text{ns}$ , $R_X = 10\text{K}\Omega$ , $C_X = 0$ (Continued)

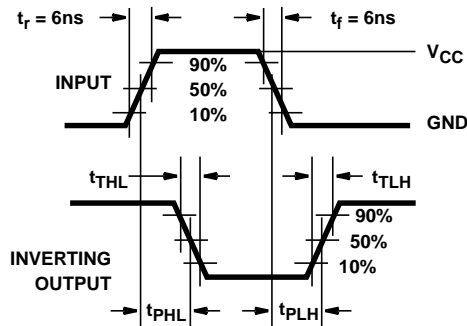
PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\bar{R}$ to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Output Pulse Width $R_X = 10\text{k}$ , $C_X = 0.1\mu\text{F}$	$\tau$	$C_L = 50\text{pF}$	5	0.63	-	0.77	0.602	0.798	0.595	0.805	ms
Output Pulse Width Match, Same Package	-	-	-	-	$\pm 1$	-	-	-	-	-	%
Power Dissipation Capacitance	$C_{PD}$	$C_L = 15\text{pF}$	5	-	134	-	-	-	-	-	pF
Input Capacitance	$C_I$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF

### NOTES:

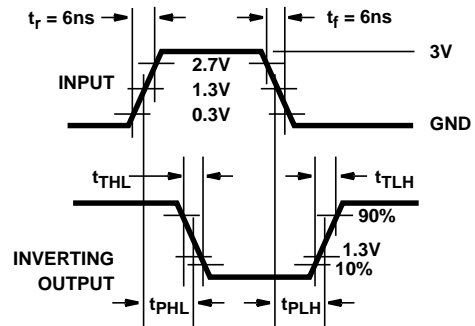
10.  $C_{PD}$  is used to determine the dynamic power consumption, per one shot.

11.  $P_D = (C_{PD} + C_X) V_{CC}^2 f_i \sum (C_L V_{CC}^2 f_O)$  where  $f_i$  = input frequency,  $f_O$  = output frequency,  $C_L$  = output load capacitance,  $C_X$  = external capacitance  $V_{CC}$  = supply voltage assuming  $f_i \ll \frac{1}{\tau}$

## **Test Circuits and Waveforms**



**FIGURE 6. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 7. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



# Typical Performance Curves

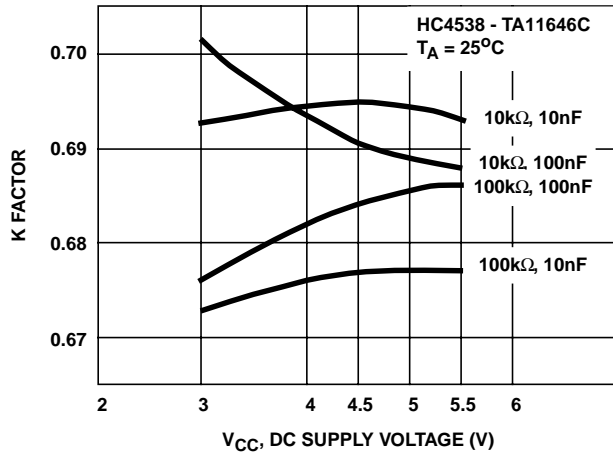


FIGURE 8. K FACTOR vs DC SUPPLY VOLTAGE ( $V_{CC}$ ) - V

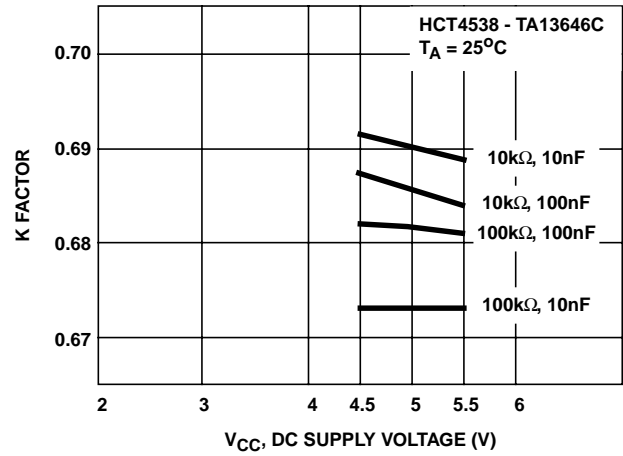


FIGURE 9. K FACTOR vs DC SUPPLY VOLTAGE ( $V_{CC}$ ) - V

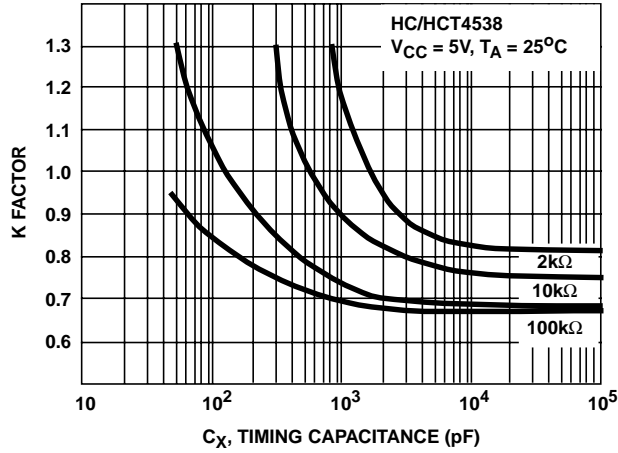


FIGURE 10. K FACTOR vs  $C_X$

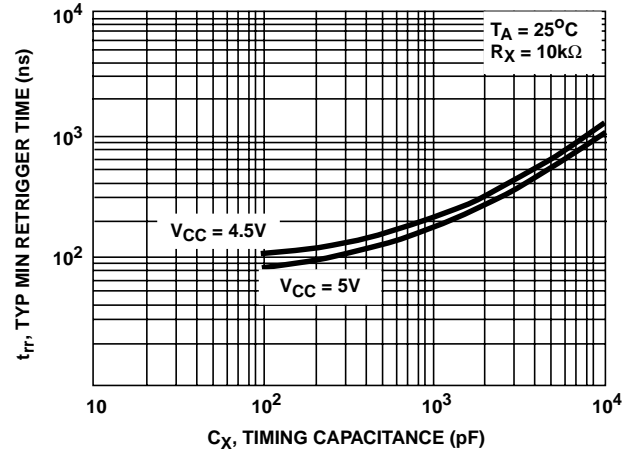


FIGURE 11. MINIMUM RETRIGGER TIME vs TIMING CAPACITANCE

## Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit with a poorly filtered power supply, the energy stored in  $C_X$  could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when  $C_X \geq 0.5\mu\text{F}$ , a protection diode with a 1 ampere or higher rating (1N5395 or equivalent) and a separate ground return for  $C_X$  should be provided as shown in Figure 12.

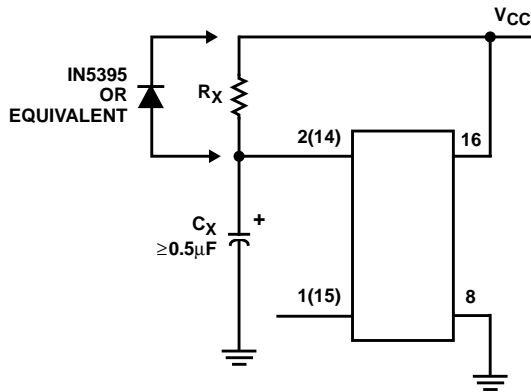


FIGURE 12. RAPID POWER-DOWN PROTECTION CIRCUIT

An alternate protection method is shown in Figure 13, where a  $51\Omega$  current-limiting resistor is inserted in series with  $C_X$ . Note that a small pulse width decrease will occur however, and  $R_X$  must be appropriately increased to obtain the originally desired pulse width.

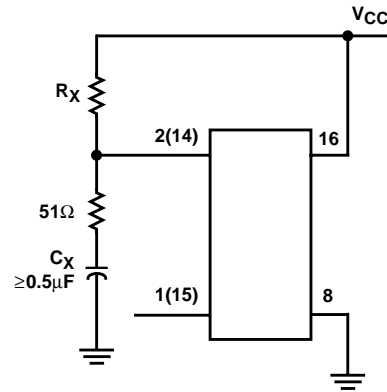


FIGURE 13. ALTERNATE RAPID POWER-DOWN PROTECTION CIRCUIT

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