

High-Speed CMOS Logic Hex Inverter

Features

- **Typical Propagation Delay:** 6ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$, Fastest Part in QMOS Line
- **Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HCU Types**
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 20\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}**

Description

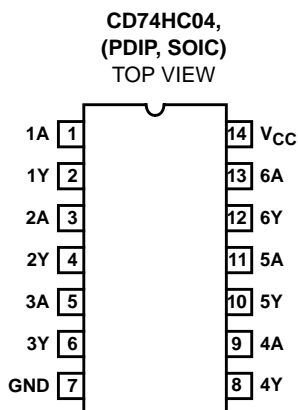
The CD74HCU04 unbuffered hex inverter utilizes silicon-gate CMOS technology to achieve operation speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. These devices are especially useful in crystal oscillator and analog applications.

Ordering Information

PART NUMBER	TEMP. RANGE ($^\circ C$)	PACKAGE
CD74HCU04E	-55 to 125	14 Ld PDIP
CD74HCU04M	-55 to 125	14 Ld SOIC
CD74HCU04MT	-55 to 125	14 Ld SOIC
CD74HCU04M96	-55 to 125	14 Ld SOIC

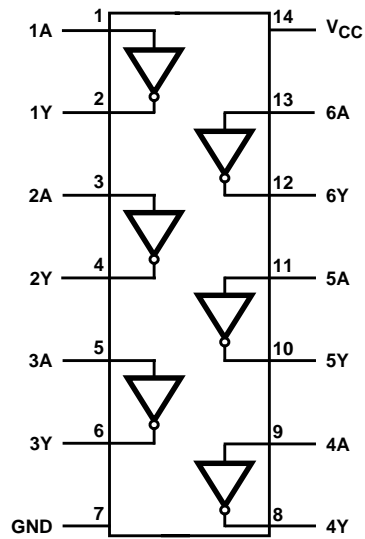
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

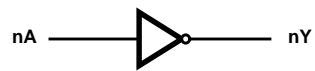


CD74HCU04

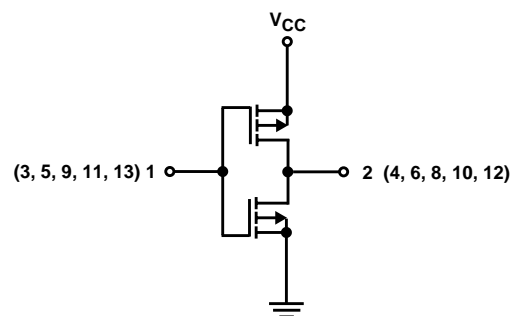
Functional Diagram



Logic Symbol



Schematic Diagram



CD74HCU04

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to +7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{\circ}C/W$)
E (PDIP) Package	80
M (SOIC) Package	.86
Maximum Junction Temperature (Hermetic Package or Die)	175 $^{\circ}C$
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	.2V to 6V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO +85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V _{IH}	-	-	2	1.7	-	1.7	-	1.7	-	V
				4.5	3.6	-	3.6	-	3.6	-	V
				6	4.8	-	4.8	-	4.8	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	0.3	-	0.3	-	0.3	V
				4.5	-	0.8	-	0.8	-	0.8	V
				6	-	1.1	-	1.1	-	1.1	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.8	-	1.8	-	1.8	-	V
			-0.02	4.5	4	-	4	-	4	-	V
			-0.02	6	5.5	-	5.5	-	5.5	-	V
High Level Output Voltage TTL Loads		V _{CC} or GND	-4	4.5	3.98	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads		V _{OL}	V _{IH} or V _{IL}	0.02	2	-	0.2	-	0.2	-	0.2
	0.02			4.5	-	0.5	-	0.5	-	0.5	V
	0.02			6	-	0.5	-	0.5	-	0.5	V
	Low Level Output Voltage TTL Loads		V _{CC} or GND	4	4.5	-	0.26	-	0.33	-	0.4
5.2		6		-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	2	-	20	-	40	μA

CD74HCU04

Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, Input to Output Y (Figure 1)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	70	-	90	-	105	ns
		$C_L = 50\text{pF}$	4.5	-	-	14	-	18	-	21	ns
		$C_L = 15\text{pF}$	5	-	5	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	12	-	15	-	18	ns
Transition Times (Figure 1)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	18	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	See Figure 3								pF
Power Dissipation Capacitance (Notes 2, 3)	C_{PD}	-	5	-	14	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per inverter.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

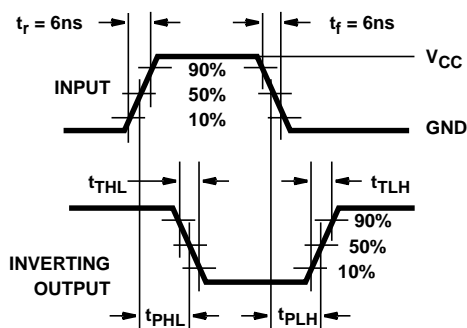


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Typical Performance Curves

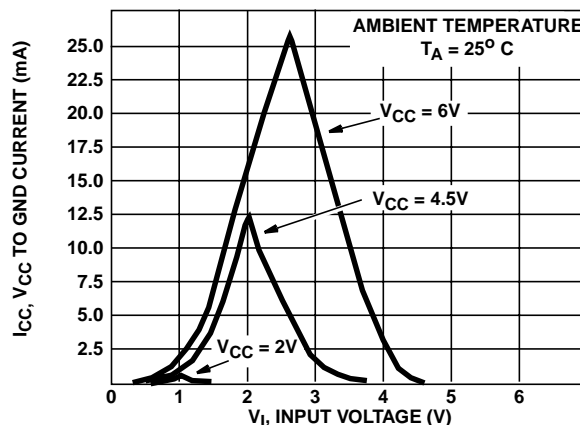


FIGURE 2. TYPICAL INVERTER SUPPLY CURRENT AS FUNCTION OF INPUT VOLTAGE

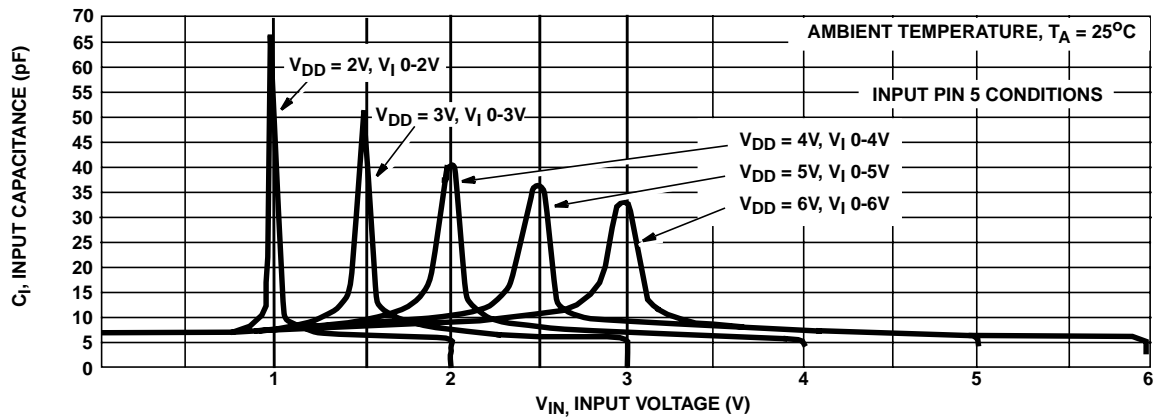
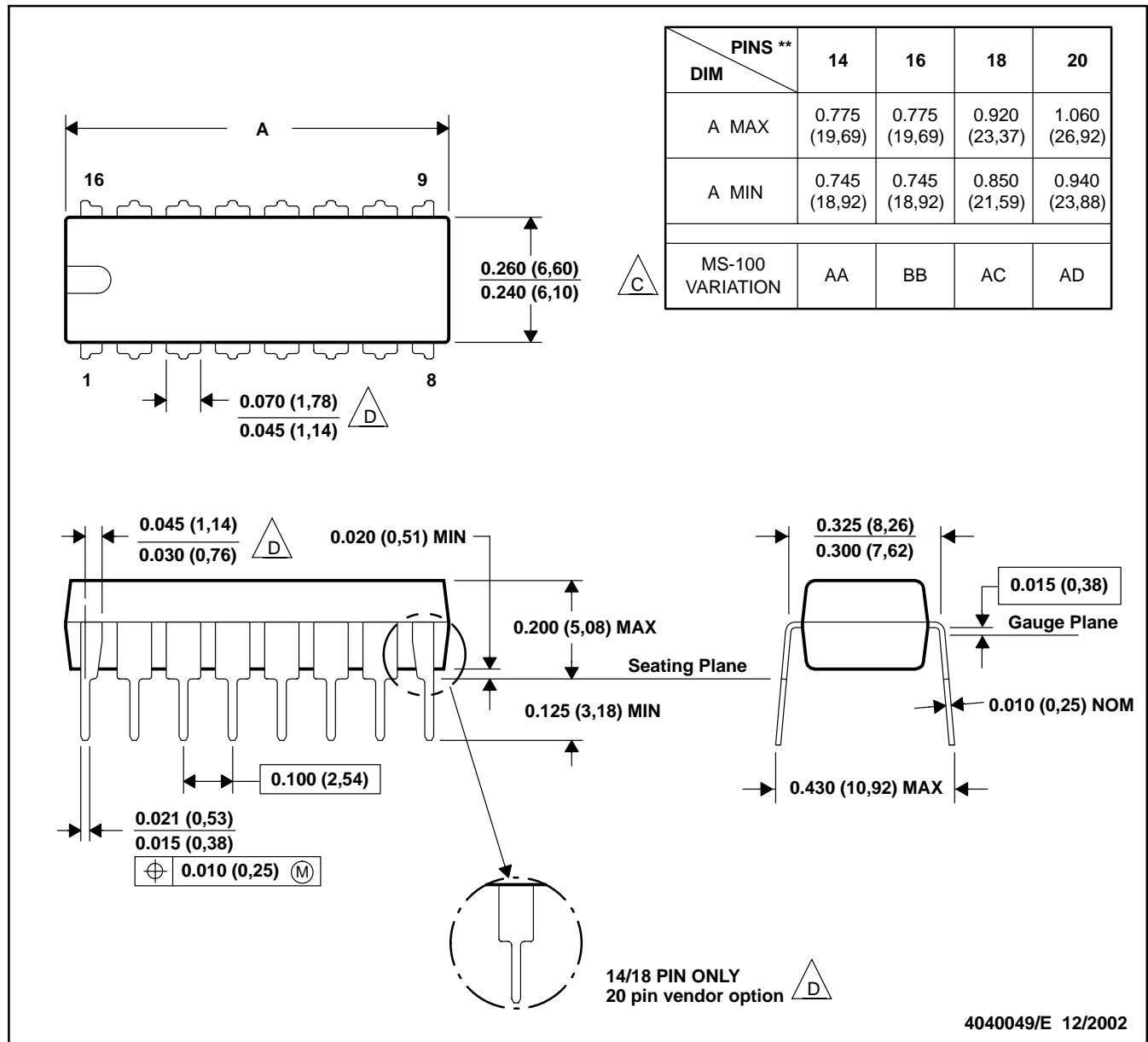
Typical Performance Curves (Continued)

FIGURE 3. INPUT CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE

N (R-PDIP-T)**

16 PINS SHOWN

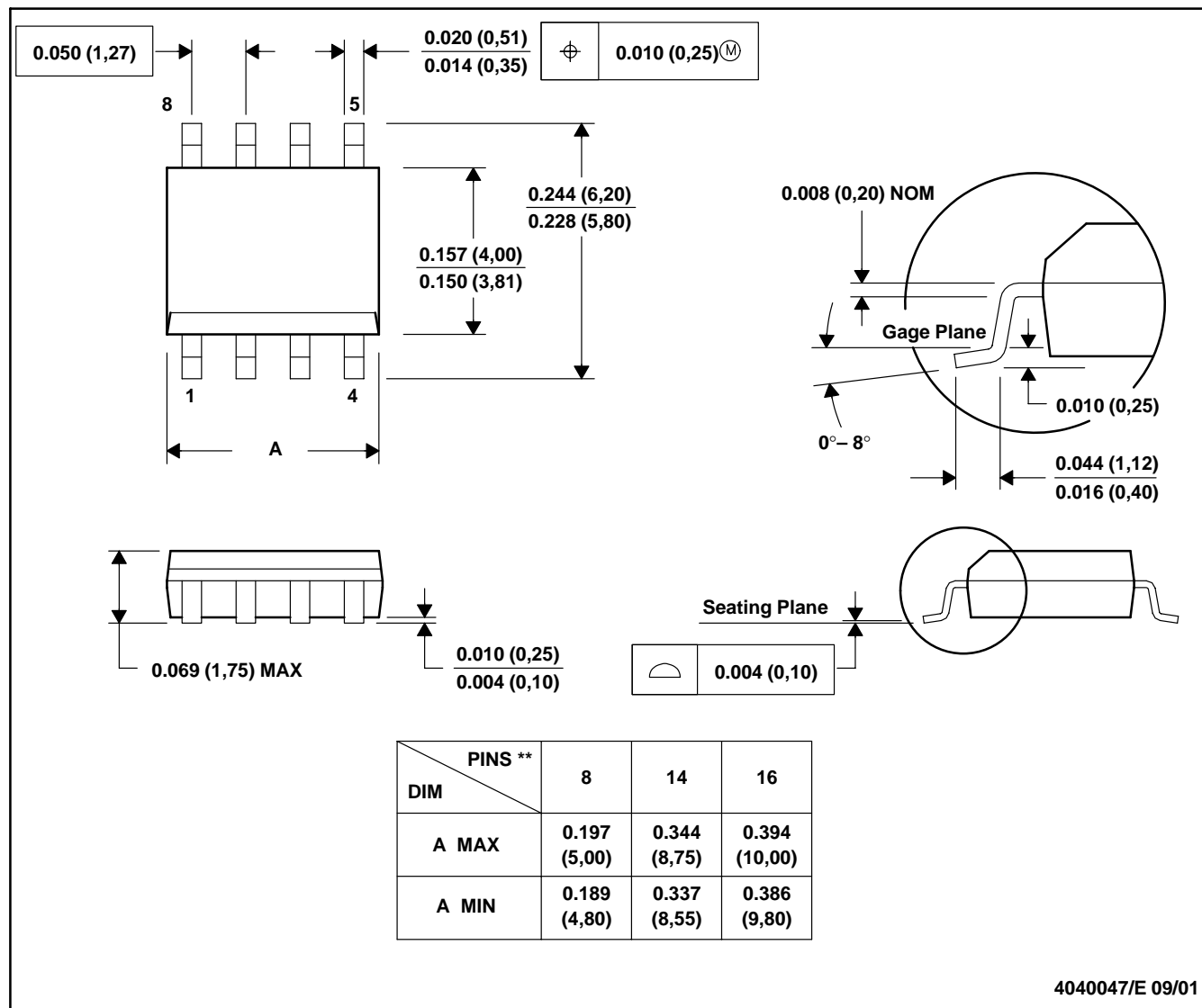
PLASTIC DUAL-IN-LINE PACKAGE

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

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