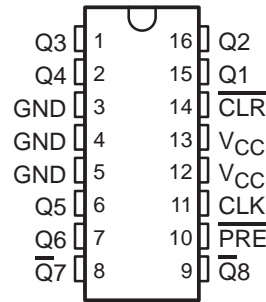


# CDC303 OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

SCAS323A – JULY 1990 – REVISED NOVEMBER 1995

- Replaces SN74AS303
- Maximum Output Skew Between Same Phase Outputs of 1 ns
- Maximum Pulse Skew of 1 ns
- TTL-Compatible Inputs and Outputs
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include Plastic Small-Outline (D) Package and Standard Plastic (N) 300-mil DIPs

D OR N PACKAGE  
(TOP VIEW)



## description

The CDC303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. Preset ( $\overline{PRE}$ ) and clear ( $\overline{CLR}$ ) inputs are provided to set the Q and  $\overline{Q}$  outputs high or low independent of the clock (CLK) input.

The CDC303 has output and pulse-skew parameters  $t_{sk(o)}$  and  $t_{sk(p)}$  to ensure performance as a clock driver when a divide-by-two function is required.

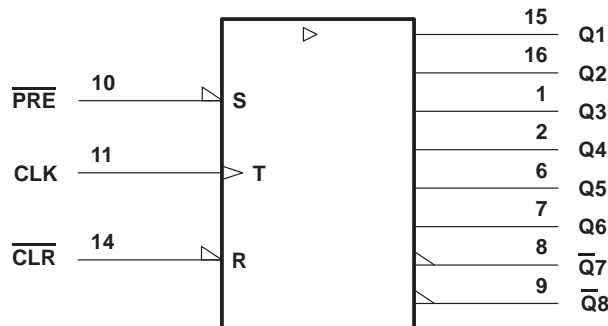
The CDC303 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q6	$\overline{Q7}$ – $\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L <sup>†</sup>	L <sup>†</sup>
H	H	↑	$\overline{Q}_0$	Q <sub>0</sub>
H	H	L	Q <sub>0</sub>	$\overline{Q}_0$

<sup>†</sup> This configuration does not persist when  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

## logic symbol<sup>‡</sup>



<sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

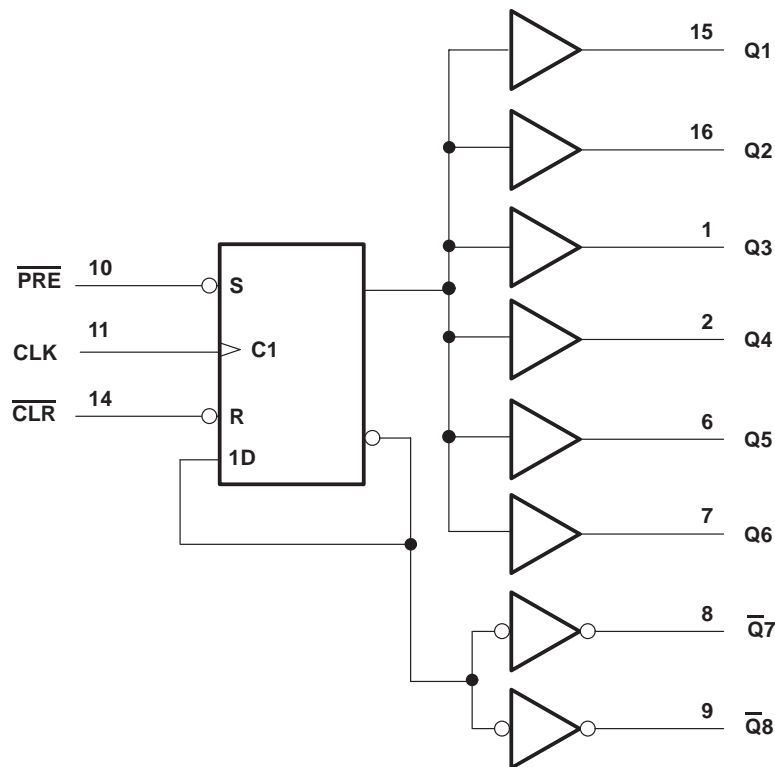
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CDC303  
OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Maximum power dissipation at $T_A = 55^{\circ}\text{C}$ (in still air) (see Note 1): D package	0.77 W
N package	1.2 W
Storage temperature range, $T_{stg}$	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of  $150^{\circ}\text{C}$  and a board trace length of 300 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			-24	mA
$I_{OL}$ Low-level output current			48	mA
$f_{clock}$ Input clock frequency			80	MHz
$T_A$ Operating free-air temperature	0		70	$^{\circ}\text{C}$

# CDC303

## OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ ,	$I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -24\text{ mA}$	2	2.8		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 48\text{ mA}$		0.3	0.5	V
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.5	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-50		-150	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ ,	See Note 2		40	70	mA

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 2:  $I_{CC}$  is measured with CLK and  $\overline{\text{PRE}}$  grounded, then with CLK and  $\overline{\text{CLR}}$  grounded.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

		MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency	0	80	MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ low	5	ns
		CLK high	4	
		CLK low	6	
$t_{su}$	Setup time before CLK <sup>†</sup>	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ inactive	6	ns

**switching characteristics over recommended operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$f_{\text{max}}^{\S}$				80		MHz
$t_{PLH}$	CLK	$Q, \overline{Q}$	$R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$	2	9	ns
$t_{PHL}$				2	9	
$t_{PLH}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	$Q, \overline{Q}$	$R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$	3	12	ns
$t_{PHL}$				3	12	
$t_{sk(o)}$	CLK	$Q$	$R_L = 500\ \Omega$ , $C_L = 10\text{ pF to } 30\text{ pF}$ , See Figure 2		1	ns
		$\overline{Q}$			1	
		$Q, \overline{Q}$			2	
$t_{sk(p)}$	CLK	$Q, \overline{Q}$	$R_L = 500\ \Omega$ , $C_L = 10\text{ pF to } 30\text{ pF}$		1	ns
$t_r$					4.5	ns
$t_f$					3.5	ns

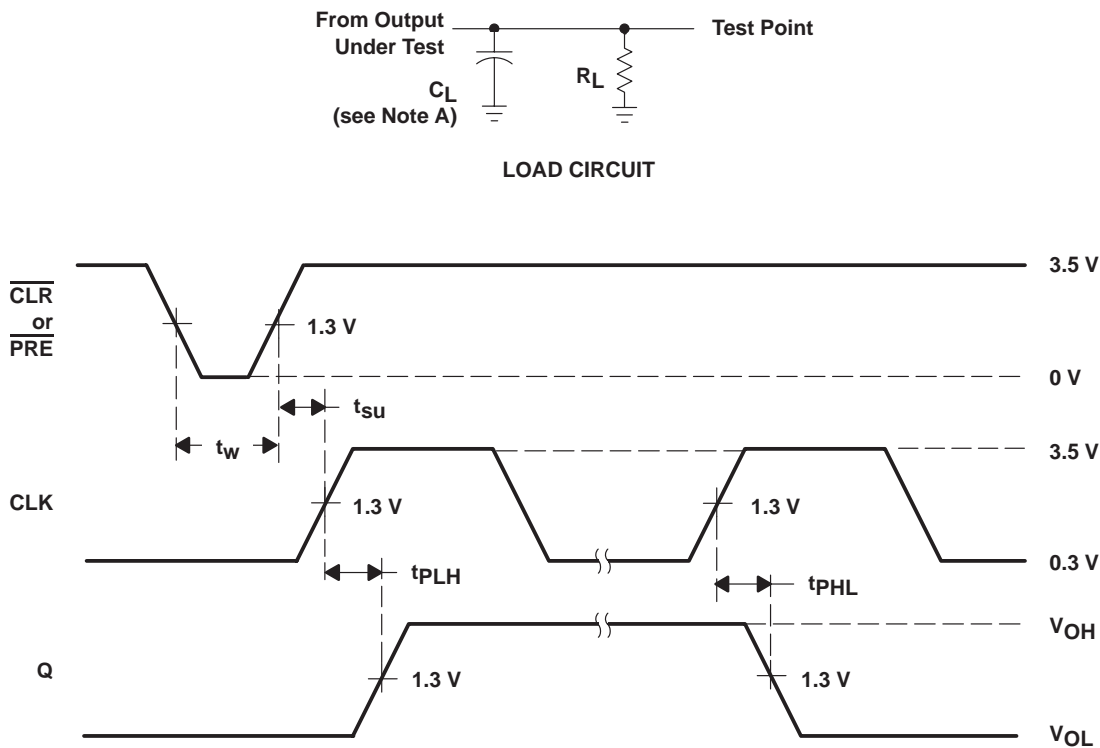
<sup>\S</sup>  $f_{\text{max}}$  minimum values are at  $C_L = 0\text{ to } 30\text{ pF}$ .



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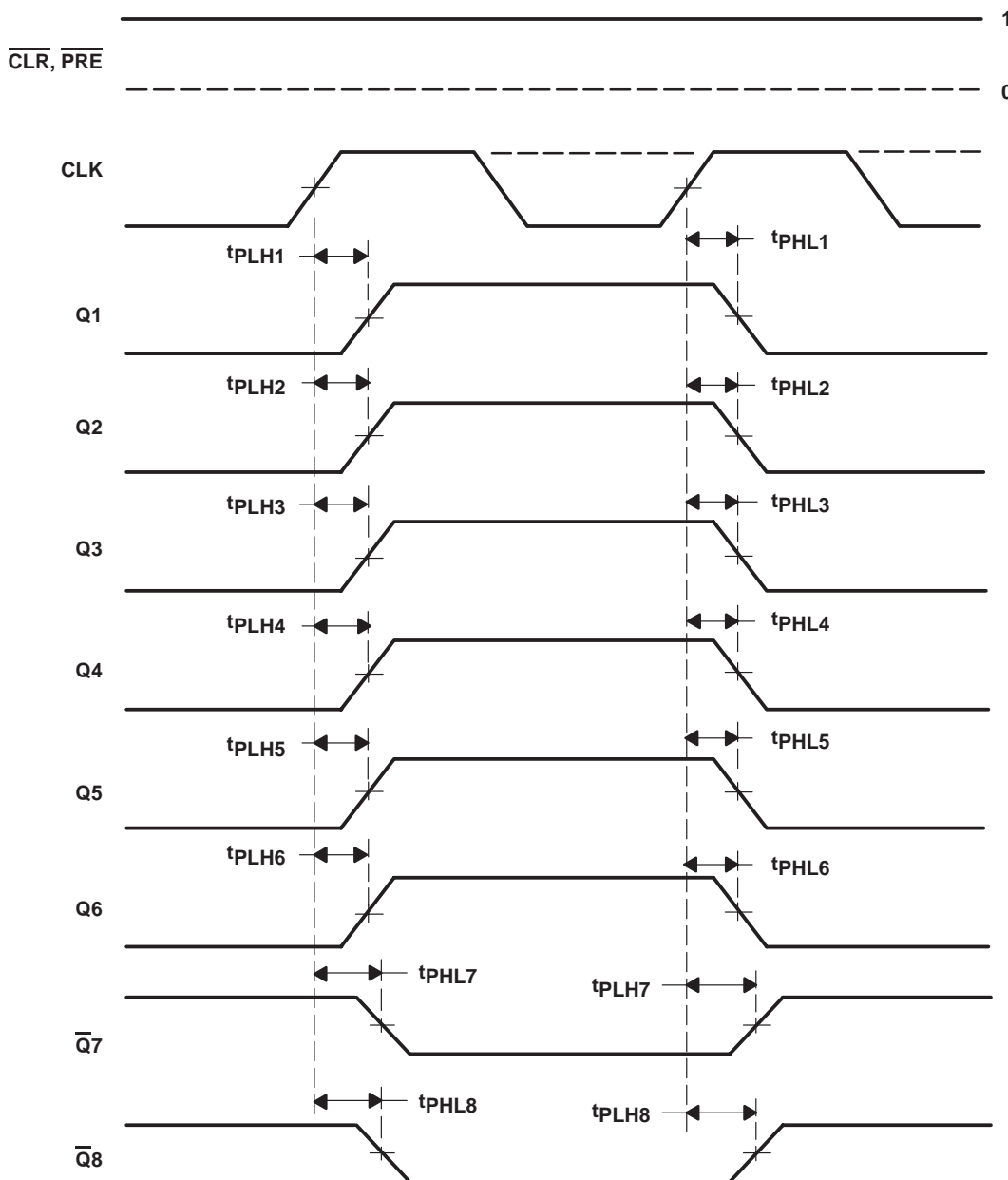
PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = 2.5$  ns,  $t_f = 2.5$  ns.

Figure 1. Load Circuit and Voltage Waveforms

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $t_{sk(o)}$ , CLK to Q, is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, 3, 4, 5, 6$ )
  - The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1, 2, 3, 4, 5, 6$ )
- B.  $t_{sk(o)}$ , CLK to  $\overline{Q}$ , is calculated as the greater of:  $|t_{PLH7} - t_{PLH8}|$  and  $|t_{PHL7} - t_{PHL8}|$ .
- C.  $t_{sk(o)}$ , CLK to Q and  $\overline{Q}$ , is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, 3, 4, 5, 6$ ),  $t_{PLH7}$ , and  $t_{PLH8}$
  - The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1, 2, 3, 4, 5, 6$ ),  $t_{PHL7}$ , and  $t_{PHL8}$
- D.  $t_{sk(p)}$  is calculated as the greater of  $|t_{PLHn} - t_{PHLn}|$  ( $n = 1, 2, 3, \dots, 8$ ).

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$  and  $t_{sk(p)}$**

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