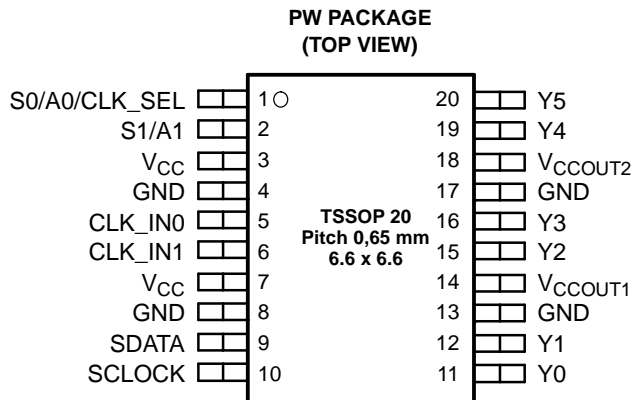


PROGRAMMABLE 3-PLL CLOCK SYNTHESIZER / MULTIPLIER / DIVIDER

FEATURES

- High Performance 2:6 PLL based Clock Synthesizer / Multiplier / Divider
- User Programmable PLL Frequencies using EEPROM Technology
- EEPROM Programming Without the Need to Apply High Programming Voltage
- Easy In-Circuit Programming via SMBus Data Interface
- Wide PLL Divider Ratio Allows 0-ppm Output Clock Error
- Clock Inputs Accept a Crystal or a Single-Ended LVCMOS or a Differential Input Signal
- Accepts Crystal Frequencies from 8 MHz up to 54 MHz
- Accepts LVCMOS or Differential Input Frequencies up to 200 MHz
- Two Programmable Control Inputs [S0/S1, A0/A1] for User Defined Control Signals
- Six LVCMOS Outputs with Output Frequencies up to 300 MHz
- LVCMOS Outputs can be Programmed for Complementary Signals (Pseudo Differential Outputs)
- Free Selectable Output Frequency via Programmable Output Switching Matrix [6x6] Including 7-Bit Post-Divider for Each Output
- PLL Loop Filter Components Integrated
- Low Period Jitter (Typ 60 ps)
- Features Spread Spectrum Clocking (SSC) for Lowering System EMI
- Programmable Output Slew-Rate Control (SRC) for Lowering System EMI
- Separate Power Supplies for Outputs (2.3 V to 3.6 V) Supports Mixed Power Supply Environments
- 3.3-V Device Power Supply
- Industrial Temperature Range –40°C to 85°C
- Development and Programming Kit for Ease PLL Design and Programming (TI Pro-Clock™)
- Packaged in 20-Pin TSSOP

TERMINAL ASSIGNMENT



PRODUCT PREVIEW

DESCRIPTION

The CDCE706 is one of the smallest and powerful PLL synthesizer / multiplier / divider available today. Despite its small physical outlines, the CDCE706 is the most flexible. It has the capability to produce an almost independent output frequency from a given input frequency.

The input frequency can be derived from a LVCMOS, differential input clock, or a single crystal. The appropriate input waveform can be selected via the SMBus data interface controller.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Pro-Clock is a trademark of Texas Instruments.

To achieve an independent output frequency the reference divider M and the feedback divider N for each PLL can be set to values from 1 up to 511 for the M-Divider and from 1 up to 4095 for the N-Divider. The PLL-VCO (voltage controlled oscillator) frequency then is routed to the free programmable output switching matrix to any of the six outputs. The switching matrix includes an additional 7-bit post-divider (1-to-127) and an inverting logic for each output. The individual selectable inverting logic allows two LVCMOS outputs to work as pseudo differential signal (0 degrees and 180 degree phase shift).

The deep M/N divider ratio allows the generation of zero ppm clocks from e.g., a 27-MHz reference input frequency.

The CDCE706 includes three PLLs of those one supports SSC (spread-spectrum clocking). PLL1, PLL2, and PLL3 are designed for frequencies up to 300 MHz and optimized for zero-ppm applications with wide divider factors.

PLL2 also supports center-spread and down-spread spectrum clocking (SSC) which effectively lower the energy for the selected frequency range. The electro-magnetic interference (EMI) will be significantly reduced. Also, the slew-rate controllable (SRC) output edges minimize EMI noise.

Based on the PLL frequency and the divider settings, the internal loop filter components will be automatically adjusted to achieve high stability and optimized jitter transfer characteristic of the PLL.

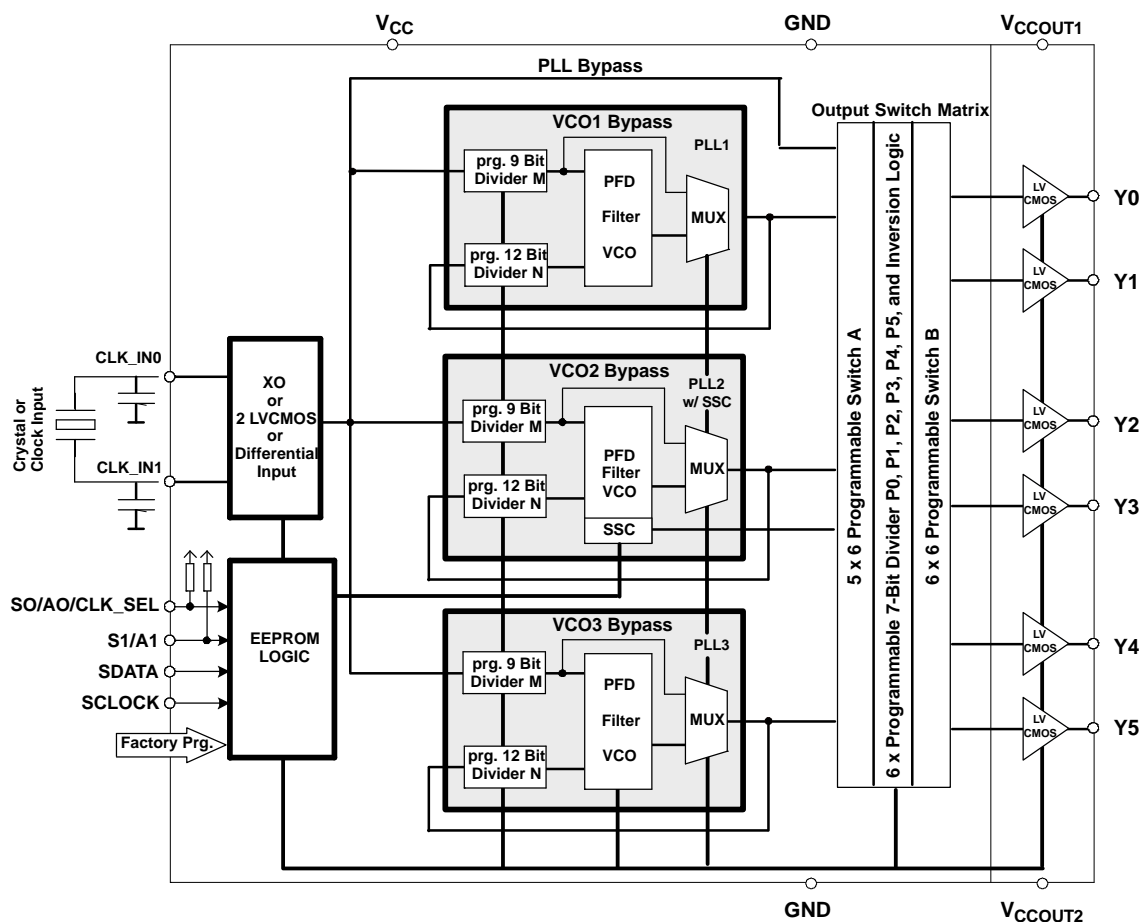
The device supports non-volatile EEPROM programming for ease-customized application. It is pre-programmed with a factory default configuration (see [Figure 8](#)) and can be re-programmed to a different application configuration before it goes onto the PCB or re-programmed by in-system programming. A different register setting is programmed via the serial SMBus Interface.

Two free programmable inputs, S0 and S1, can be used to control for each application the most demanding logic control settings (outputs disable to low, outputs 3-state, power down, PLL bypass, etc).

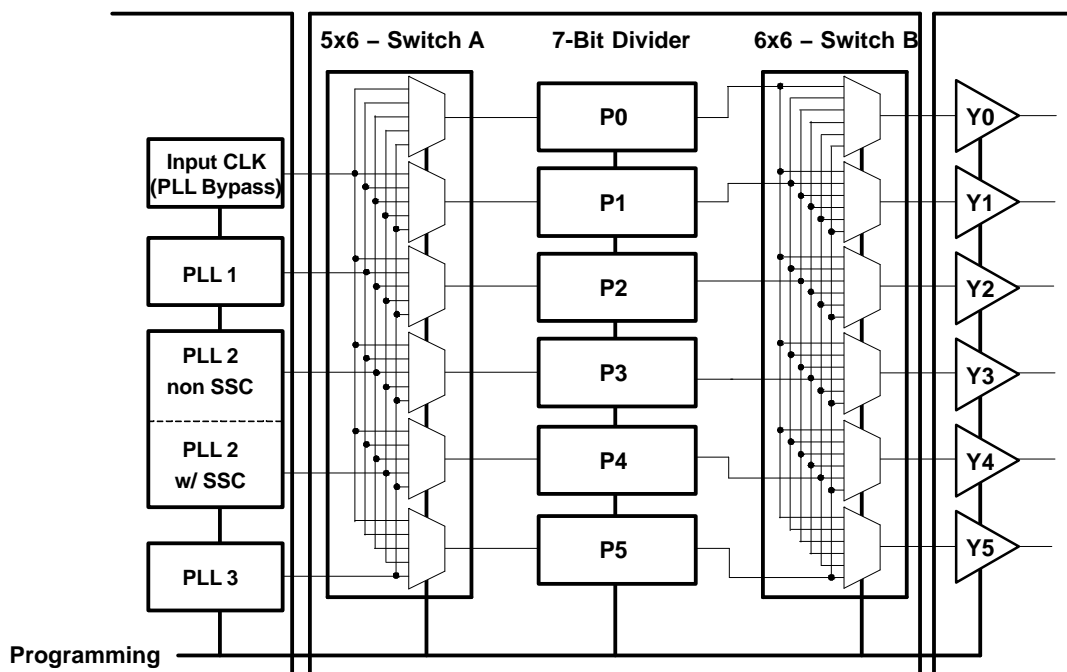
The CDCE706 has three power supply pins, V_{CC} , V_{CCOUT1} and V_{CCOUT2} . V_{CC} is the power supply for the device. It operates from a single 3.3-V supply voltage. V_{CCOUT1} and V_{CCOUT2} are the power supply pins for the outputs. V_{CCOUT1} supplies the outputs Y0 and Y1 and V_{CCOUT2} supplies the outputs Y2, Y3, Y4, and Y5. Both outputs supplies can be 2.3 V to 3.6 V.

The CDCE706 is characterized for operation from -40°C to 85°C .

FUNCTIONAL BLOCK DIAGRAM



OUTPUT SWITCH MATRIX



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	TSSOP20 NO.		
Y0 to Y5	11, 12, 15, 16, 19, 20	O	LVC MOS outputs
CLK_IN0	5	I	Dependent on SMBus settings, CLK_IN0 is the crystal oscillator input and can also be used as LVC MOS input or as positive differential signal inputs.
CLK_IN1	6	I/O	Dependent on SMBus settings, CLK_IN1 is serving as the crystal oscillator output or can be the second LVC MOS input or the negative differential signal input.
V _{CC}	3, 7	Power	3.3-V power supply for the device
V _{CCOUT1}	14	Power	Power 2.5-V to 3.3-V power supply for outputs Y0, Y1
V _{CCOUT2}	18	Power	Power 2.5-V to 3.3-V power supply for outputs Y2, Y3, Y4, Y5
GND	4, 8, 13, 17	Ground	Ground
S0, A0, CLK_SEL	1	I	User programmable control input S0 (PLL bypass or power-down mode) or AO (address bit 0), or CLK_SEL (selects one of two LVC MOS clock inputs), dependent on the SMBus settings; LVC MOS inputs; internal pullup 150 k Ω .
S1, A1	2	I	User programmable control input S1 (output enable/disable or all output low), A1 (address bit 1), dependent on the SMBus settings; LVC MOS inputs; internal pullup 150 k Ω
SDATA	9	I/O	Serial control data input/output for SMBus controller; LVC MOS input
SCLOCK	10	I	Serial control clock input for SMBus controller; LVC MOS input

ABSOLUTE MAXIMUM RATINGSover operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	VALUE	UNIT
V _{CC} Supply voltage range	–0.5 to 4.6	V
V _I Input voltage range ⁽²⁾	–0.5 to V _{CC} + 0.5	V
V _O Output voltage range ⁽²⁾	–0.5 to V _{CC} + 0.5	V
I _I Input current (V _I < 0, V _I > V _{CC})	±20	mA
I _O Continuous output current	±50	mA
T _{stg} Storage temperature range	–65 to 150	°C
T _J Maximum junction temperature	125	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PACKAGE THERMAL RESISTANCEfor TSSOP20 (PW) Package ⁽¹⁾

PARAMETER	AIRFLOW (lfm)	°C/W
θ_{JA} Thermal resistance junction-to-ambient	0	66.3
	150	59.3
	250	56.3
	500	51.9
θ_{JC} Thermal resistance junction-to-case		19.7

- (1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V _{CC} Device supply voltage	3	3.3	3.6	V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CCOUT1}	Output Y0,Y1 supply voltage	2.3		3.6	V
V _{CCOUT2}	Output Y2, Y3, Y4, Y5 supply voltage	2.3		3.6	V
V _{IL}	Low level input voltage LVCMOS			0.3 V _{CC}	V
V _{IH}	High level input voltage LVCMOS	0.7 V _{CC}			V
V _{Ithresh}	Input voltage threshold LVCMOS		0.5 V _{CC}		V
V _I	Input voltage range LVCMOS	0		3.6	V
V _{ID}	Differential input voltage	0.4			V
V _{IC}	Common-mode for differential input voltage	0.2		V _{CC} - 1	V
I _{OH}	High-level output current			–6	mA
I _{OL}	Low-level output current			6	mA
C _L	Output load LVCMOS			25	pF
T _A	Operating free-air temperature	–40		85	°C

RECOMMENDED CRYSTAL SPECIFICATIONS

		MIN	NOM	MAX	UNIT
f _{Xtal}	Crystal input frequency range (fundamental mode)	8	27	54	MHz
ESR	Effective series resistance ⁽¹⁾⁽²⁾	15		60	Ω
C _{IN}	Input capacitance CLK_IN0 and CLK_IN1		4		pF

(1) For crystal frequencies above 50 MHz the effective series resistor should not exceed 50 Ω to assure stable start-up condition.

(2) Maximum Power Handling (Drive Level) see [Figure 10](#).

EEPROM SPECIFICATION

		MIN	TYP	MAX	UNIT
EEcyc	Programming cycles of EEPROM	100	TBD		Cycles
EEret	Data retention		TBD		Years

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating-free air temperature

		MIN	NOM	MAX	UNIT
CLK_IN REQUIREMENTS					
f _{CLK_IN}	LVCMOS CLK_IN clock input frequency	PLL mode		1	MHz
		PLL bypass mode		0	
t _r / t _f	Rise and fall time CLK_IN signal (20% to 80%)			4	ns
duty _{REF}	Duty cycle CLK_IN at V _{CC} / 2	40%		60%	
SMBus TIMING REQUIREMENTS (see Figure 6)					
f _{SCLK}	SCLK frequency			100	kHz
t _h (START)	START hold time	4			μs
t _w (SCLL)	SCLK low-pulse duration	4.7			μs
t _w (SCLH)	SCLK high-pulse duration	4		50	μs
t _{su} (START)	START setup time	0.6			μs
t _h (SDATA)	SDATA hold time	0.3			μs
t _{su} (SDATA)	SDATA setup time	0.25			μs
t _r	SCLK / SDATA input rise time			1000	ns
t _f	SCLK / SDATA input fall time			300	ns
t _{su} (STOP)	STOP setup time	4			μs

TIMING REQUIREMENTS (continued)

over recommended ranges of supply voltage, load, and operating-free air temperature

		MIN	NOM	MAX	UNIT
t_{BUS}	Bus free time	4.7			μs
t_{POR}	Time in which the device must be operational after power-on reset			500	ms

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
OVERALL PARAMETER						
I _{CC}	Supply current	All PLLs on, all outputs on, f _{out} = 80 MHz, f _{CLK_IN} = 27 MHz, f _{VCO} = 160 MHz	90	115		mA
I _{CCPD}	Power down current. Every circuit powered down except SMBus	f _{IN} = 0 MHz, V _{CC} = 3.6 V	300			μA
V _{PUC}	Supply voltage V _{cc} threshold for power up control circuit		2.3			V
f _{VCO}	VCO frequency of internal PLL (any of three PLLs)	Normal speed-mode ⁽²⁾	80	167		MHz
		High-speed mode ⁽²⁾	150	300		
f _{OUT}	LVCMOS output frequency range	V _{CC} = 2.5 V		250		MHz
		V _{CC} = 3.3 V		300		
LVCMOS PARAMETER						
V _{IK}	LVCMOS input voltage	V _{CC} = 3 V; I _I = −18 mA			−1.2	V
I _I	LVCMOS input current	V _I = 0 V or V _{CC} , V _{CC} = 3.6 V		TBD		μA
I _{IH}	LVCMOS input current For S1/S0	V _I = V _{CC} , V _{CC} = 3.6 V		TBD		μA
I _{IL}	LVCMOS input current For S1/S0	V _I = 0 V, V _{CC} = 3.6 V		TBD		μA
C _I	Input capacitance at CLK_IN0 and CLK_IN1	V _I = 0 V or V _{CC}		3		pF

(1) All typical values are at respective nominal V_{CC} .(2) Normal-speed mode or high-speed mode must be selected by the VCO frequency selection bit in Byte 6, Bit [7:5]. The min f_{vco} can be lower but impacts jitter-performance.

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
LVCMOS PARAMETER FOR V _{ccout} = 3.3-V Mode						
V _{OH}	LVCMOS high-level output voltage	V _{ccout} = 3 V, I _{OH} = −0.1 mA	2.9			V
		V _{ccout} = 3 V, I _{OH} = −4 mA	2.4			
		V _{ccout} = 3 V, I _{OH} = −6 mA	2.1			
V _{OL}	LVCMOS low-level output voltage	V _{ccout} = 3 V, I _{OL} = 0.1 mA			0.1	V
		V _{ccout} = 3 V, I _{OL} = 4 mA			0.5	
		V _{ccout} = 3 V, I _{OL} = 6 mA			0.85	
t _{PLH} , t _{PHL}	Propagation delay	All PLL bypass	9			ns
		VCO bypass	11			
t _{r0} /t _{f0}	Rise and fall time for output slew rate 0	V _{ccout} = 3.3 V (20%–80%)	3.3			ns
t _{r1} /t _{f1}	Rise and fall time for output slew rate 1	V _{ccout} = 3.3 V (20%–80%)	2.5			ns
t _{r2} /t _{f2}	Rise and fall time for output slew rate 2	V _{ccout} = 3.3 V (20%–80%)	1.6			ns
t _{r3} /t _{f3}	Rise and fall time for output slew rate 3	V _{ccout} = 3.3 V (20%–80%)	0.6			ns
t _{jit(cc)}	Cycle-to-cycle jitter ⁽³⁾⁽⁴⁾	1 PLL, 1 Output	50		TBD	ps
		3 PLLs, 3 Outputs	120		TBD	
t _{jit(per)}	Peak-to-peak period jitter ⁽⁴⁾	1 PLL, 1 Output	60		TBD	
		3 PLLs, 3 Outputs	130		TBD	
t _{sk(o)}	Output skew (see ⁽⁵⁾ and Table 5)	1.6-ns rise/fall time (default) at f _{vco} = 150 MHz, Pdiv = 3			200	ps
odc	Output duty cycle ⁽⁶⁾	f _{vco} = 250 MHz, Pdiv = 1	45%			55%
		f _{vco} = 250 MHz, Pdiv = 25				
LVCMOS PARAMETER FOR V _{ccout} = 2.5-V Mode						
V _{OH}	LVCMOS high-level output voltage	V _{ccout} = 2.3 V, I _{OH} = 0.1 mA	2.2			V
		V _{ccout} = 2.3 V, I _{OH} = −3 mA	1.7			
		V _{ccout} = 2.3 V, I _{OH} = −4 mA	1.5			
V _{OL}	LVCMOS low-level output voltage	V _{ccout} = 2.3 V, I _{OL} = 0.1 mA			0.1	V
		V _{ccout} = 2.3 V, I _{OL} = 3 mA			0.5	
		V _{ccout} = 2.3 V, I _{OL} = 4 mA			0.85	
t _{PLH} , t _{PHL}	Propagation delay	All PLL bypass	9			ns
		VCO Bypass	11			
t _{r0} /t _{f0}	Rise and fall time for output slew rate 0	V _{ccout} = 2.5 V (20%–80%)	3.9			ns
t _{r1} /t _{f1}	Rise and fall time for output slew rate 1	V _{ccout} = 2.5 V (20%–80%)	2.9			ns
t _{r2} /t _{f2}	Rise and fall time for output slew rate 2	V _{ccout} = 2.5 V (20%–80%)	2.0			ns
t _{r3} /t _{f3}	Rise and fall time for output slew rate 3	V _{ccout} = 2.5 V (20%–80%)	0.8			ns
t _{jit(cc)}	Cycle-to-cycle jitter ⁽³⁾⁽⁴⁾	1 PLL, 1 Output	60		TBD	ps
		3 PLLs, 3 Outputs	130		TBD	
t _{jit(per)}	Peak-to-peak period jitter ⁽⁴⁾	1 PLL, 1 Output	60		TBD	ps
		3 PLLs, 3 Outputs	140		TBD	
t _{sk(o)}	Output skew (see ⁽⁵⁾ and Table 5)	2-ns rise/fall time (default) at fvco = 150 MHz, Pdiv = 3			250	ps

(3) 50000 cycles

(4) Jitter depends on configuration.

(5) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

(6) odc depends on output rise and fall time (t_r/t_f); above limits are for normal t_r/t_f , except for frequencies ranging from 167 MHz to 300 MHz, the fastest slew rate is used (0.6 ns at $V_{ccout} = 3.3\text{ V}$ or 0.8 ns at $V_{ccout} = 2.5\text{ V}$).

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
odc	Output duty cycle ⁽⁶⁾	fvco = 250 MHz, Pdiv = 1	45%		55%	
		fvco = 250 MHz, Pdiv = 25				
SMBus PARAMETER						
V _{IK}	SCLK and SDATA input clamp voltage	V _{CC} = 3 V, I _I = −18 mA			−1.2	V
I _{IH}	SCLK and SDATA input current	V _I = V _{CC} , V _{CC} = 3.6 V			5	μA
I _{IL}	SCLK and SDATA input current	V _I = 0 V, V _{CC} = 3.6 V	−15		−5	μA
V _{IH}	SCLK input high voltage		2.1			V
V _{IL}	SCLK input low voltage				0.8	V
V _{OL}	SDATA low-level output voltage	I _{OL} = 4 mA, V _{CC} = 3 V			0.4	V
C _{ISCLK}	Input capacitance at SCLK	V _I = 0 V or V _{CC}		4	10	pF
C _{ISDATA}	Input capacitance at SDATA	V _I = 0 V or V _{CC}		4	10	pF

PARAMETER MEASUREMENT INFORMATION

TBD

TYPICAL CHARACTERISTICS

TBD

APPLICATION INFORMATION

SMBus Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. It follows the SMBus specification Version 2.0, which is based upon the principals of operation of I2C. More details of the SMBus specification can be found at <http://www.smbus.org>.

Through the SMBus, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the SMBus data interface initialize to their default setting upon power-up, and therefore using this interface is optional. The clock device register changes are normally made upon system initialization, if any are required.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operations from the controller.

For Block Write/Read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individually addressed bytes.

Once a byte has been sent, it will be written into the internal register and effective immediately. This applies to each transferred byte, independent of whether this is a Byte Write or a Block Write sequence.

If the EEPROM write cycle is initiated, the data of the internal SMBus register is written into the EEPROM. During EEPROM write, no data is allowed to be sent to the device via the SMBus until the programming sequence is completed. Data, however, can be readout during the programming sequence (byte read or block read). The programming status can be monitored by EEPIP, byte 24 bit 7.

The offset of the indexed byte is encoded in the command code, as described in Table 1.

The Block Write and Block Read protocol is outlined in Figure 4 and Figure 5, while Figure 2 and Figure 3 outlines the corresponding Byte Write and Byte Read protocol.

Slave Receiver Address (7 bits)

A6	A5	A4	A3	A2	A1*	A0*	R/W
1	1	0	1	0	0	1	0

* Address bits A0 and A1 are programmable by the Configuration Inputs S0 and S1 (Byte 10 Bit [1:0] and Bit [3:2]. This allows addressing up to four devices connected to the same SMBus.

Table 1. Command Code Definition

Bit	Description
7	0 = Block Read or Block Write operation 1 = Byte Read or Byte Write operation
(6:0)	Byte Offset for Byte Read and Byte Write operation. For Block Read and Block Write operation, these bits have to be 000 0000.

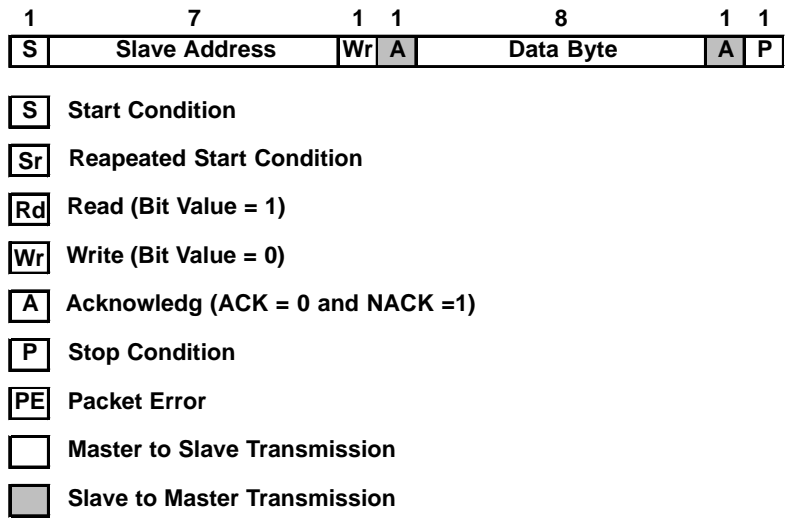


Figure 1. Generic Programming Sequence

Byte Write Programming Sequence

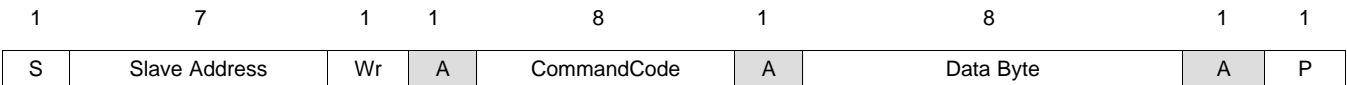


Figure 2. Byte Write Protocol

Byte Read Programming Sequence

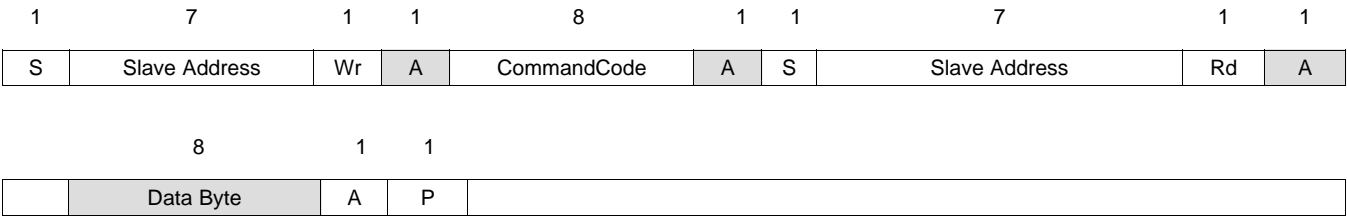
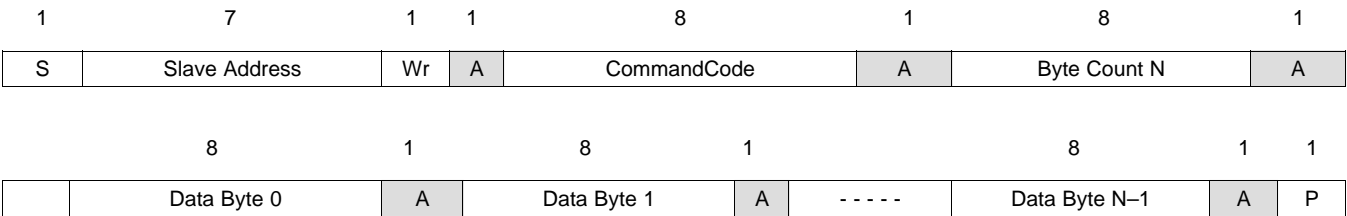


Figure 3. Byte Read Protocol

Block Write Programming Sequence⁽¹⁾



⁽¹⁾Data bit is reserved for revision code and vendor identification. However, this byte is used for internal test. Do not write into it other than 0000 0000.

Figure 4. Block Write Protocol

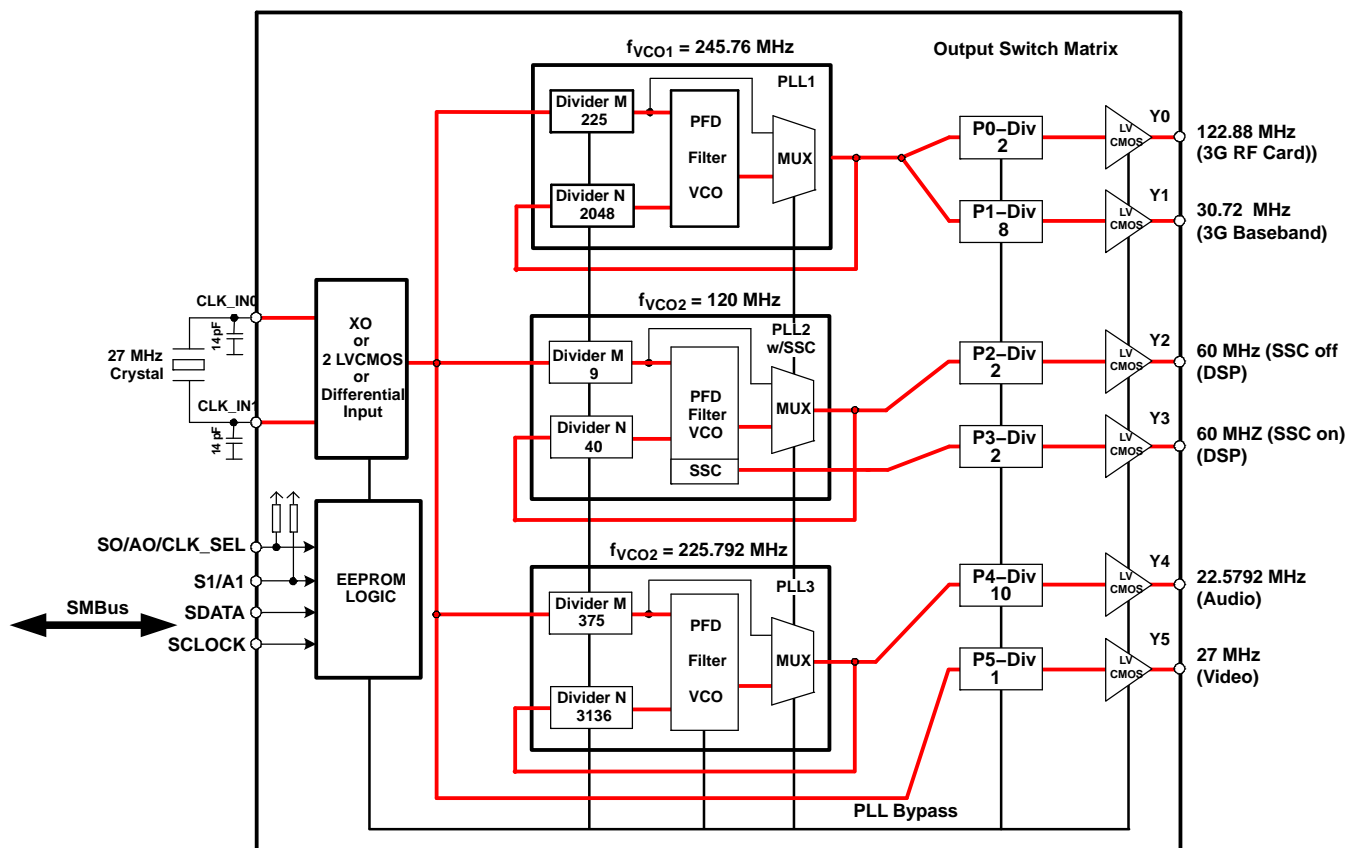
Table 2. Register Configuration Command Bitmap

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	Revision Code				Vendor Identification			
Byte 1	PLL1 Reference Divider M 9-Bit [7:0]							
Byte 2	PLL1 Feedback Divider N 12-Bit [7:0]							
Byte 3	PLL1 Mux	PLL2 Mux	PLL3 Mux	PLL1 Feedback Divider N 12-Bit [11:8]				PLL1 Ref Dev M [8]
Byte 4	PLL2 Reference Divider M 9-Bit [7:0]							
Byte 5	PLL2 Feedback Divider N 12-Bit [7:0]							
Byte 6	PLL1 fvco Selection	PLL2 fvco Selection	PLL3 fvco Selection	PLL2 Feedback Divider N 12-Bit [11:8]				PLL2 Ref Dev M [8]
Byte 7	PLL3 Reference Divider 9-Bit M [7:0]							
Byte 8	PLL3 Feedback Divider N [12-Bit 7:0]							
Byte 9	PLL Selection for P0 (Switch A)			PLL3 Feedback Divider N 12-Bit [11:8]				PLL3 Ref Dev M [8]
Byte 10	PLL Selection for P1 (Switch A)			Inp. Clock Selection	Configuration Inputs S1		Configuration Inputs S0	
Byte 11	Input Signal Source		PLL Selection for P3 (Switch A)			PLL Selection for P2 (Switch A)		
Byte 12	Reserved	Power Down	PLL Selection for P5 (Switch A)			PLL Selection for P4 (Switch A)		
Byte 13	Reserved	7-Bit Divider P0 [6:0]						
Byte 14	Reserved	7-Bit Divider P1 [6:0]						
Byte 15	Reserved	7-Bit Divider P2 [6:0]						
Byte 16	Reserved	7-Bit Divider P3 [6:0]						
Byte 17	Reserved	7-Bit Divider P4 [6:0]						
Byte 18	Reserved	7-Bit Divider P5 [6:0]						
Byte 19	Reserved	Y0 Inv. or Non-Inv	Y0 Slew-Rate Control		Y0 Enable or Low	Y0 Divider Selection (Switch B)		
Byte 20	Reserved	Y1 Inv. or Non-Inv	Y1 Slew-Rate Control		Y1 Enable or Low	Y1 Divider Selection (Switch B)		
Byte 21	Reserved	Y2 Inv. or Non-Inv	Y2 Slew-Rate Control		Y2 Enable or Low	Y2 Divider Selection (Switch B)		
Byte 22	Reserved	Y3 Inv. or Non-Inv	Y3 Slew-Rate Control		Y3 Enable or Low	Y3 Divider Selection (Switch B)		
Byte 23	Reserved	Y4 Inv. or Non-Inv	Y4 Slew-Rate Control		Y4 Enable or Low	Y4 Divider Selection (Switch B)		
Byte 24	EEPIP [read only]	Y5 Inv or Non-Inv	Y5 Slew-Rate Control		Y5 Enable or Low	Y5 Divider Selection (Switch B)		
Byte 25	EELOCK	Spread Spectrum (SSC) Modulation Selection			Frequency Selection for SSC			
Byte 26	EEWRITE	7-Bit Byte Count						

Default Device Setting

The internal EEPROM of CDCE706 is pre-programmed with a factory default configuration as shown below. This puts the device in an operating mode without the need to program it first. The default setting appears after power is switched on or after a power-down/up sequence until it is re-programmed by the user to a different application configuration. A new register setting is programmed via the serial SMBUS Interface.

A different default setting can be programmed upon customer request. Contact a Texas Instruments sales or marketing representative for more information.



NOTE: All outputs are enabled and in non-inverting mode. S0, S1, and SSC comply according the default setting described in Byte 10 and Byte 25 respectively.

Figure 8. Default Device Setting

The output frequency can be calculated:

$$f_{out} = \frac{f_{in} \times N}{M \times P}, \text{ i.e. } f_{out} = \frac{27 \text{ MHz} \times 3136}{(375 \times 10)} = 22.5792 \text{ MHz}$$

(1)

PRODUCT PREVIEW

Functional Description of the Logic

All Bytes are read-/write-able, unless otherwise expressly mentioned.

Byte 0 (read only): Vendor Identification Bits [3:0]; Revision Code Bit [7:4]								
Revision Code				Vendor Identification				
0	0	0	0	0	0	0	1	

Byte 1 to 9: Reference Divider M of PLL1, PLL2, PLL3 ⁽¹⁾										
M8	M7	M6	M5	M4	M3	M2	M1	M0	Div by	Default ⁽²⁾⁽³⁾
0	0	0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	0	1	0	2	
0	0	0	0	0	0	0	1	1	3	
				•						
				•						
				•						
1	1	1	1	1	1	1	0	1	509	
1	1	1	1	1	1	1	1	0	510	
1	1	1	1	1	1	1	1	1	511	

- (1) By selecting the PLL divider factors, $M \leq N$ and $80 \text{ MHz} \leq f_{vco} \leq 300 \text{ MHz}$.
 (2) Unless customer specific setting.
 (3) Default setting of divider M for PLL1 = 225, for PLL2 = 9 and for PLL3 = 375.

Byte 1 to 9: Feedback Divider N of PLL1, PLL2, PLL3 ⁽¹⁾													
N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	Div by	Default ⁽²⁾⁽³⁾
0	0	0	0	0	0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	0	0	0	0	0	1	1	
0	0	0	0	0	0	0	0	0	0	1	0	2	
0	0	0	0	0	0	0	0	0	0	1	1	3	
							•						
							•						
							•						
1	1	1	1	1	1	1	1	1	1	0	1	4093	
1	1	1	1	1	1	1	1	1	1	1	0	4094	
1	1	1	1	1	1	1	1	1	1	1	1	4095	

- (1) By selecting the PLL divider factors, $M \leq N$ and $80 \text{ MHz} \leq f_{vco} \leq 300 \text{ MHz}$.
 (2) Unless customer specific setting.
 (3) Default setting of divider N for PLL1 = 1024, for PLL2 = 40 and for PLL3 = 1568.

Byte 3 Bit [7:5]: PLL (VCO) Bypass Multiplexer		
PLLxMUX	PLL (VCO) MUX Output	Default ⁽¹⁾
0	PLLx	Yes
1	VCO bypass	

- (1) Unless customer specific setting.

Byte 6 Bit [7:5]: VCO Frequency Selection Mode for each PLL ⁽¹⁾		
PLLxFVCO	VCO Frequency Range	Default ⁽²⁾
0	80-200 MHz	Yes
1	180-300 MHz	

- (1) This bit selects the normal-speed mode or the high-speed mode for the dedicated VCO in PLL1, PLL2 or PLL3. At power-up the normal-speed mode is selected, f_{vco} is 80-200 MHz. In case of higher f_{vco} , this bit has to be set to [1].
 (2) Unless customer specific setting.

Byte 9 to 12: Outputs Switch Matrix (5x6 Switch A) PLL Selection for P-Divider P0-P5				
SWAPx2	SWAPx1	SWAPx0	Any Output Px	Default ⁽¹⁾
0	0	0	PLL bypass (input clock)	P5
0	0	1	PLL1	P0, P1
0	1	0	PLL2 non-SSC	P2
0	1	1	PLL2 w/ SSC ⁽²⁾	P3
1	0	0	PLL3	P4
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

(1) Unless customer specific setting.

(2) PLL2 has a SSC output and non-SSC output. If SSC bypass is selected (see Byte 25, Bit [6:4]), the SSC circuitry of PLL2 is powered-down and the SSC output is reset to logic low. The non-SSC output of PLL2 is not affected by this mode and can still be used.

Byte 10, Bit [1:0]: Configuration Settings of Input S0/A0/CLK_SEL			
S01	S00	Function	Default ⁽¹⁾
0	0	If S0 is low, the PLLs and the clock-input stage are going into power-down mode, outputs are in 3-state, all actual register settings will be maintained, SMBus stays active ⁽²⁾	Yes
0	1	If S0 is low, the PLL and all dividers (M-Div and P-Div) are bypassed and PLL is in power-down, all outputs are active (inv. or non-inv.), actual register settings will be maintained, SMBus stays active; this mode is useful for production test;	
1	0	CLK_SEL (input clock selection — overwrites the CLK_SEL setting in Byte 10, Bit [4]) ⁽³⁾ — CLK_SEL is set low selects CLK_IN_IN0 — CLK_SEL is set high selects CLK_IN_IN1	
1	1	In this mode, the control input S0 is interpreted as address bit A0 of the slave receiver address byte ⁽⁴⁾	

(1) Unless customer specific setting.

(2) Power-down mode overwrites 3-state or low-state of S1 setting in Byte 10, Bit [3:2].

(3) If the clock input (CLK_IN0/CLK_IN1) is selected as crystal input or differential clock input (Byte 11, Bit [7:6]) then this setting is not relevant.

(4) To use this pin as Slave Receiver Address Bit A0, an Initialization pattern needs to be sent to CDCE706. When S00/S01 is set to be 1, the S0 input pin will be interpreted in the next read or write cycle as the Address Bit A0 of the Slave Receiver Address Byte. Note that right after the Byte 10 (S00/S01) has been written, A0 (via S0-pin) will immediately be active (also when Byte 10 is sent within a block write sequence). After the Initialization each CDCE706 has its own S0 dependent Slave Receiver Address and can be addressed accordingly to their new valid address.

Byte 10, Bit [3:2]: Configuration Settings of Input S1/A1			
S11	S10	Function	Default ⁽¹⁾
0	0	If S1 is set low, all outputs are switched to a low-state (non-inv.) or high-state (inv.);	Yes
0	1	If S1 is set low, all outputs are switched to a 3-state	
1	0	Reserved	
1	1	In this mode, the control input S1 is interpreted as Address Bit A1 of the Slave Receiver Address Byte ⁽²⁾	

(1) Unless customer specific setting.

(2) To use this pin as Slave Receiver Address Bit A1, an Initialization pattern needs to be sent to CDCE706. When S10/S11 is set to be 1, the S1 input pin will be interpreted in the next read or write cycle as the Address Bit A1 of the Slave Receiver Address Byte. Note that right after the Byte 10 (S10/S11) has been written, A1 (via S1-pin) will immediately be active (also when Byte 10 is sent within a block write sequence). After the Initialization each CDCE706 has its own S1 dependent Slave Receiver Address and can be addressed accordingly to their new valid address.

Byte 10, Bit [4]: Input Clock Selection ⁽¹⁾		
CLKSEL	Input Clock	Default ⁽²⁾
0	CLK_IN0	Yes
1	CLK_IN1	

(1) This bit is not relevant, if crystal input or differential clock input is selected, Byte 11, Bit [7:6].

(2) Unless customer specific setting.

Byte 11, Bit [7:6]: Input Signal Source ⁽¹⁾			
IS1	IS0	Function	Default ⁽²⁾
0	0	CLK_IN0 is Crystal Oscillator Input and CLK_IN1 is serving as Crystal Oscillator Output.	Yes
0	1	CLK_IN0 and CLK_IN1 are two LVCMOS Inputs. CLK_IN0 or CLK_IN1 are selectable via CLK_SEL control pin.	
1	0	CLK_IN0 and CLK_IN1 serve as differential signal inputs.	
1	1	Reserved	

(1) In case the crystal input or differential clock input is selected, the input clock selection, Byte 10, Bit [4], is not relevant.

(2) Unless customer specific setting.

Byte 12, Bit [6]: Power-Down Mode (except SMBus)		
PD	Power-Down Mode	Default ⁽¹⁾
0	Normal Device Operation	Yes
1	Power Down ⁽²⁾	

(1) Unless customer specific setting.

(2) In power down, all PLLs and the Clock-Input-Stage are going into power-down mode, all outputs are in 3-State, all actual register settings will be maintained and SMBus stays active. Power-Down Mode overwrites 3-State or Low-State of S0 and S1 setting in Byte 10.

Byte 13 to 18, Bit [6:0]: Outputs Switch Matrix - 6x7-Bit Divider P0-P5								
DIVYx6	DIVYx5	DIVYx4	DIVYx3	DIVYx2	DIVYx1	DIVYx0	Div by	Default ⁽¹⁾⁽²⁾
0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	1	1	
0	0	0	0	0	1	0	2	
		⋮						
1	1	1	1	1	0	1	125	
1	1	1	1	1	1	0	126	
1	1	1	1	1	1	1	127	

(1) Unless customer specific setting.

(2) Default setting of divider P0 = 1, P1 = 4, P2 = 2, P3 = 2, P4 = 5, and P5 = 1

Byte 19 to 24, Bit [5:4]: LVCMOS Output Rise/Fall Time Setting at Y0-Y5			
SRCYx1	SRCYx0	Yx	Default ⁽¹⁾
0	0	Nominal +2 ns (t_{r0}/t_{f0})	
0	1	Nominal +1 ns (t_{r1}/t_{f1})	
1	0	Nominal (t_{r2}/t_{f2})	Yes
1	1	Nominal –1 ns (t_{r3}/t_{f3})	

(1) Unless customer specific setting.

Byte 19 to 24, Bit [2:0]: Outputs Switch Matrix (6 x 6 Switch B) Divider (P0-P5) Selection for Outputs Y0-Y5				
SWBYx2	SWBYx1	SWBYx0	Any Output Yx	Default ⁽¹⁾
0	0	0	Divider P0	Y0
0	0	1	Divider P1	Y1
0	1	0	Divider P2	Y2
0	1	1	Divider P3	Y3
1	0	0	Divider P4	Y4
1	0	1	Divider P5	Y5
1	1	0	Reserved	
1	1	1	Reserved	

(1) Unless customer specific setting.

Byte 19 to 24, Bit [3]: Output Y0-Y5 Enable or Low-State		
ENDISYx	Output Yx	Default ⁽¹⁾
0	Disable to low	
1	Enable	Yes

(1) Unless customer specific setting.

Byte 19 to 24, Bit [6]: Output Y0-Y5 Non-Inverting/Inverting		
INVYx	Output Yx Status	Default ⁽¹⁾
0	Non-inverting	Yes
1	Inverting	

(1) Unless customer specific setting.

Byte 24, Bit [7] (read only): EEPROM Programming In Process Status ⁽¹⁾		
EEPIP	Indicate EEPROM Write Process	Default
0	No programming	
1	Programming in process	

(1) This *read only* Bit indicates an EEPROM write process. It is set to high if programming starts and resets to low if programming is completed. Any data written to the EEPIP-Bit will be ignored. During programming, no data are allowed to be sent to the device via the SMBus until the programming sequence is completed. Data, however, can be readout during the programming sequence (Byte Read or Block Read).

Byte 25, Bit [3:0]: SSC Modulation Frequency Selection in the Range of 30 kHz 60 kHz ⁽¹⁾														
FSSC3	FSSC2	FSSC1	FSSC0	Modulation Factor		f _{vco} [MHz]								Default ⁽²⁾
						100	110	120	130	140	150	160	167	
0	0	0	0	5680	f _{mod} [kHz]	17.6	19.4	21.1	22.9	24.6	26.4	28.2	29.4	
0	0	0	1	5412		18.5	20.3	22.2	24.0	25.9	27.7	29.6	30.9	
0	0	1	0	5144		19.4	21.4	23.3	25.3	27.2	29.2	31.1	32.5	
0	0	1	1	4876		20.5	22.6	24.6	26.7	28.7	30.8	32.8	34.2	
0	1	0	0	4608		21.7	23.9	26.0	28.2	30.4	32.6	34.7	36.2	
0	1	0	1	4340		23.0	25.3	27.6	30.0	32.3	34.6	36.9	38.5	
0	1	1	0	4072		24.6	27.0	29.5	31.9	34.4	36.8	39.3	41.0	
0	1	1	1	3804		26.3	28.9	31.5	34.2	36.8	39.4	42.1	43.9	
1	0	0	0	3536		28.3	31.1	33.9	36.8	39.6	42.4	45.2	47.2	
1	0	0	1	3286		30.4	33.5	36.5	39.6	42.6	45.6	48.7	50.8	Yes
1	0	1	0	3000		33.3	36.7	40.0	43.3	46.7	50.0	53.3	55.7	
1	0	1	1	2732		36.6	40.3	43.9	47.6	51.2	54.9	58.6	61.1	
1	1	0	0	2464		40.6	44.6	48.7	52.8	56.8	60.9	64.9	67.8	
1	1	0	1	2196		45.5	50.1	54.6	59.2	63.8	68.3	72.9	76.0	
1	1	1	0	1928		51.9	57.1	62.2	67.4	72.6	77.8	83.0	86.6	
1	1	1	1	1660		60.2	66.3	72.3	78.3	84.3	90.4	96.4	100.6	

(1) The PLL has to be bypassed (turned off) when changing *SSC Modulation Frequency Factor* on-the-fly. This can be done by following programming sequence: bypass PLL2 (Byte 3, Bit 6 = 1); write new *Modulation Factor* (Byte 25); re-activate PLL2 (Byte 3, Bit 6 = 0).

(2) Unless customer specific setting.

Byte 25, Bit [6:4]: SSC Modulation Amount ⁽¹⁾				
SSC2	SSC1	SSC0	Function	Default ⁽²⁾
0	0	0	SSC Modulation Amount 0% = SSC bypass for PLL ⁽³⁾	
0	0	1	SSC Modulation Amount $\pm 0.1\%$ (center spread)	
0	1	0	SSC Modulation Amount $\pm 0.25\%$ (center spread)	
0	1	1	SSC Modulation Amount $\pm 0.4\%$ (center spread)	
1	0	0	SSC Modulation Amount 1% (down spread)	Yes

(1) The PLL has to be bypassed (turned off) when changing *SSC Modulation Amount* on-the-fly. This can be done by following programming sequence: bypass PLL2 (Byte 3, Bit 6 = 1); write new *Modulation Amount* (Byte 25); re-activate PLL2 (Byte 3, Bit 6 = 0).

(2) Unless customer specific setting.

(3) If SSC bypass is selected, SSC circuitry of PLL2 is powered-down and the SSC output is reset to logic low. The non-SSC output of PLL2 is not affected by this mode and can still be used.

Byte 25, Bit [6:4]: SSC Modulation Amount ⁽¹⁾				
SSC2	SSC1	SSC0	Function	Default ⁽²⁾
1	0	1	SSC Modulation Amount 1.5% (down spread)	
1	1	0	SSC Modulation Amount 2% (down spread)	
1	1	1	SSC Modulation Amount 3% (down spread)	

Byte 25, Bit [7]: Permanently Lock EEPROM-Data		
EELOCK	Permanently Lock EEPROM ⁽¹⁾	Default ⁽²⁾
0	No	Yes
1	Yes	

- (1) If this bit is set, the actual data in the EEPROM will be permanently locked. There is no further programming possible, even this bit is set low. Data, however can still be written via SMBUS to the internal register to change device function on the fly. But new data no longer can be stored into the EEPROM.
- (2) Unless customer specific setting.

Byte 26, Bit [6:0]: Byte Count ⁽¹⁾								
BC6	BC5	BC4	BC3	BC2	BC1	BC0	No. of Bytes	Default ⁽²⁾
0	0	0	0	0	0	0	Not allowed	
0	0	0	0	0	0	1	1	
0	0	0	0	0	1	0	2	
0	0	0	0	0	1	1	3	
			• • •					
0	0	1	1	0	1	1	27	Yes
			• • •					
1	1	1	1	1	0	1	125	
1	1	1	1	1	1	0	126	
1	1	1	1	1	1	1	127	

- (1) Defines the number of Bytes, which will be sent from this device at the next Block Read protocol.
- (2) Unless customer specific setting.

Byte 26, Bit [7]: Initiate EEPROM Write Cycle ⁽¹⁾		
EEWRITE	Starts EEPROM Write Cycle	Default ⁽²⁾
0	No	Yes
1	Yes	

- (1) The EEPROM WRITE cycle is initiated with the rising edge of the EEWRITE-Bit. A static level high does not trigger an EEPROM WRITE cycle. This bit stays high until the user reset it to low (it will not automatically be reset after the programming has been completed). Therefore, to initiate an EEPROM WRITE cycle, it is recommended to send a zero-one sequence to the EEWRITE bit in Byte 26. During EEPROM programming, no data are allowed to be sent to the device via the SMBus until the programming sequence has been completed. Data, however, can be readout during the programming sequence (Byte Read or Block Read). The programming status can be monitored by readout EEPIP, Byte 24–Bit 7. If EELOCK is set, no EEPROM programming will be possible.
- (2) Unless customer specific setting.

FUNCTIONAL DESCRIPTION

Clock Inputs (CLK_IN0 and CLK_IN1)

The CDCE706 features two clock inputs which can be used as:

- Crystal oscillator input (default setting)
- Two independent single-ended LVCMOS inputs
- Differential signal input

The dedicated clock input can be selected by the *input signal source* Bit [7:6] of Byte 11.

Crystal Oscillator Inputs

The input frequency range in crystal mode is 8 MHz to 54 MHz. The CDCE706 uses a Pierce-type oscillator circuitry with included feedback resistance for the inverting amplifier. The user, however, has to add external capacitors (C_{X0} , C_{X1}) to match the input load capacitor from the crystal (see Figure 9). The required values can be calculated:

$$C_{X0} = C_{X1} = 2 \times C_L - C_{ICB},$$

where C_L is the crystal load capacitor as specified for the crystal unit and C_{ICB} is the input capacitance of the device including the board capacitance (stray capacitance of PCB).

For example, for a fundamental 27-MHz crystal with C_L of 9 pF and C_{ICB} of 4 pF,

$$C_{X0} = C_{X1} = (2 \times 9 \text{ pF}) - 4 \text{ pF} = 14 \text{ pF}.$$

It is important to use a short PCB trace from the device to the crystal unit to keep the stray capacitance of the oscillator loop to a minimum.

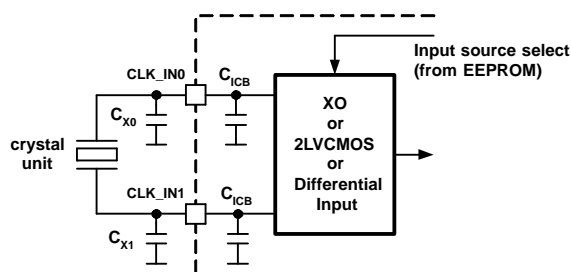


Figure 9. Crystal Input Circuitry

In order to ensure a stable oscillating, a certain drive power must be applied. The CDCE706 features an input oscillator with adaptive gain control which relieves the user to manually program the gain. The drive level is the amount of power dissipated by the oscillating crystal unit and is usually specified in terms of power dissipated by the resonator (equivalent series resistance (ESR)). Figure 10 gives the resulting drive level vs crystal frequency and ESR.

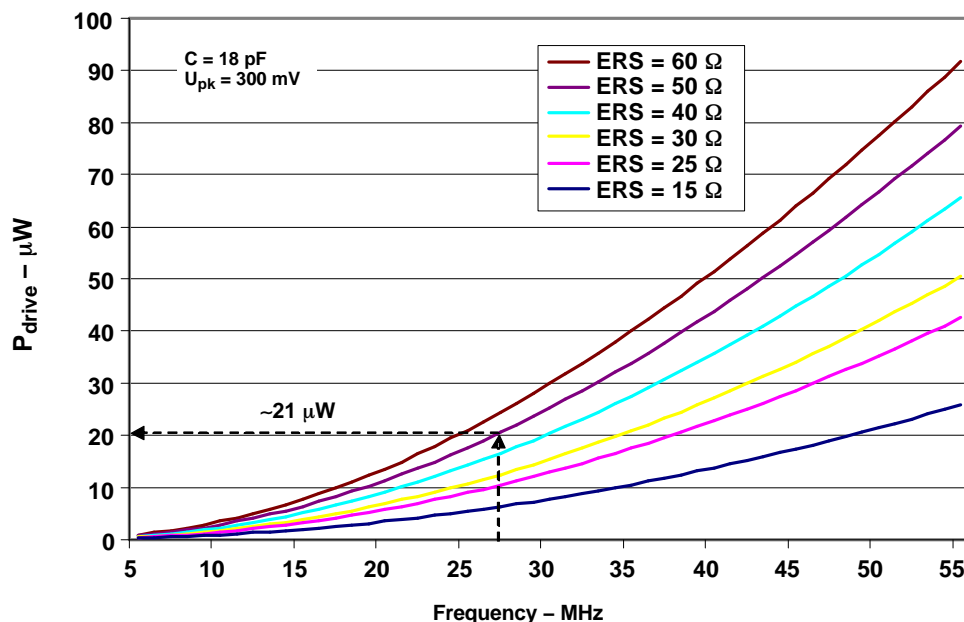


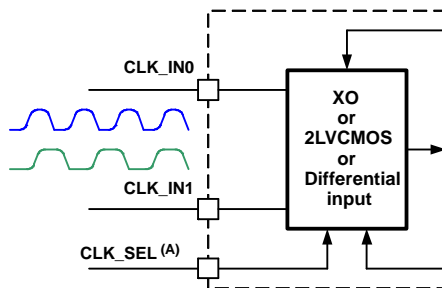
Figure 10. Crystal Drive Power

For example, if a 27-MHz crystal with ESR of $50\ \Omega$ is used and $2 \times C_L$ is 18 pF, the drive power is 21 μ W. Drive level should be held to a minimum to avoid over driving the crystal. The maximum power dissipation is specified for each type of crystal in the oscillator specifications, i.e., 100 μ W for the example above.

Single-Ended LVCMOS Clock Inputs

When selecting the LVCMOS clock mode, CLK_IN0 and CLK_IN1 act as regular clock inputs pins and can be driven up to 200 MHz. Both clock inputs circuitry are equal in design and can be used independently to each other (see Figure 11). The internal clock select bit, Byte 10, Bit [4], selects one of the two input clocks. CLK_IN0 is the default selection. There is also the option to program the external control pin S0/A0/CLK_SEL as clock select pin, Byte 10, Bit [1:0].

The two clock inputs can be used for redundancy switching, i.e. to switch between a primary clock and secondary clock. Note a phase difference between the clock inputs may require PLL correction. Also in case of different frequencies between the primary and secondary clock, the PLL has to re-lock to the new frequency.



A. CLK_SEL is optional and can be configured by EEPROM setting.

Figure 11. LVCMOS Clock Input Circuitry

Differential Clock Inputs

The CDCE706 supports differential signaling as well. In this mode, CLK_IN0 and CLK_IN1 pin serve as differential signal inputs and can be driven up to 200 MHz.

The minimum magnitude of the differential input voltage is 400mV over a differential common-mode input voltage range of 300 mV to $V_{CC} - 1$. If LVDS or LVPECL signal levels are applied, ac-coupling and a biasing structure is recommended to adjust the different physical layers (see Figure 12). The capacitor removes the dc component of the signal (common-mode voltage), while the ac component (voltage swing) is passed on. A resistor pull-up and/or pull-down network represents the biasing structure used to set the common-mode voltage on the receiver side of the ac-coupling capacitor.

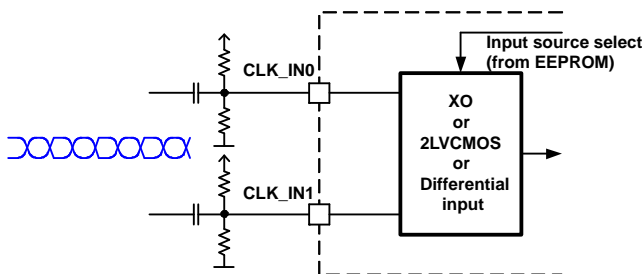


Figure 12. Differential Clock Input Circuitry

PLL Configuration and Setting

The CDCE706 includes three PLLs which are equal in function and performance. Except PLL2 which in addition supports spread spectrum clocking (SSC) generation. Figure 13 shows the block diagram of the PLL.

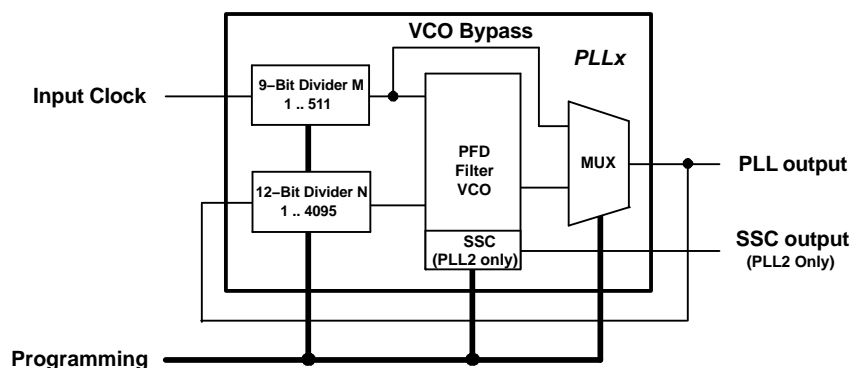


Figure 13. PLL Architecture

All three PLLs are designed for easiest configuration. The user just has to define the input and output frequencies or the divider (M, N, P) setting respectively. All other parameters, such as charge-pump current, filter components, phase margin, or loop bandwidth are controlled and set by the device itself. This assures optimized jitter attenuation and loop stability.

The PLL support normal-speed mode ($80 \text{ MHz} \leq f_{\text{VCO}} \leq 167 \text{ MHz}$) and high-speed mode ($150 \text{ MHz} \leq f_{\text{VCO}} \leq 300 \text{ MHz}$) which can be selected by PLLxFVCO (Bit [7:5] of Byte 6). The respective speed option assures stable operation and lowest jitter.

The divider M and divider N operates internally as fractional divider for f_{VCO} up to 250 MHz. This allows fractional divider ratio for zero ppm output clock error.

In case of $f_{\text{VCO}} > 250 \text{ MHz}$, it is recommended that integer factors of N/M are used only.

For optimized jitter performance, keep divider M as small as possible. Also, the fractional divider concept requires a PPL divider configuration, $M \leq N$ (or $N/M \geq 1$).

Additionally, each PLL supports two bypass options:

- PLL Bypass and
- VCO Bypass

In PLL bypass mode, the PLL completely is bypassed, so that the input clock is switched directly to the Output-Switch-A (SWAPxx of Byte 9 to 12). In the VCO bypass mode, only the VCO of the respective PLL is bypassed by setting PLLxMUX to 1 (Bit [7:5] of Byte 3). But the divider M still is useable and expands the output divider by additional 9-bits. This gives a total divider range of $M \times P = 511 \times 127 = 64897$. In VCO bypass mode the respective PLL block is powered down and minimizes current consumption.

Table 3. Example for Divide, Multiplication, and Bypass Operation

Function	Equation ⁽¹⁾	f_{IN} [MHz]	$f_{\text{OUT-desired}}$ [MHz]	$f_{\text{OUT-actual}}$ [MHz]	Divider				f_{VCO} [MHz]
					M	N	P	N/M	
Fractional ⁽²⁾	$f_{\text{OUT}} = f_{\text{IN}} \times (N/M)/P$	30.72	155.52	155.52	16	81	1	5.0625	155.52
Integer Factor ⁽³⁾	$f_{\text{OUT}} = f_{\text{IN}} \times (N/M)/P$	27	270	270	1	10	1	10	270
VCO bypass	$f_{\text{OUT}} = f_{\text{IN}}/(M \times P)$	30.72	0.06	0.06	8	—	64	—	—

(1) P-divider of Output-Switch-Matrix is included in the calculation.

(2) Fractional operation for $f_{\text{VCO}} \leq 250 \text{ MHz}$.

(3) Integer operation for $f_{\text{VCO}} > 250 \text{ MHz}$.

Spread Spectrum Clocking and EMI Reduction

In addition to the basic PLL function, PLL2 supports spread spectrum clocking (SSC) as well. Thus, PLL 2 features two outputs, a SSC output and a non-SSC output. Both outputs can be used in parallel. The mean phase of the Center Spread SSC modulated signal is equal to the phase of the non-modulated input frequency. SSC is selected by Output-Switch-A (SWAPxx of Byte 9 to 12).

SSC also is bypass-able (Byte 25, Bit [6:4]), which powers-down the SSC output and set it to logic low state. The non-SSC output of PLL2 is not affected by this mode and can still be used.

SSC is an effective method to reduce electro-magnetic interference (EMI) noise in high-speed applications. It reduces the RF energy peak of the clock signal by modulating the frequency and spread the energy of the signal to a broader frequency range. Because the energy of the clock signal remains constant, a varying frequency that broadens the overtones necessarily lowers their amplitudes. Figure 14 shows the effect of SSC on a 54-MHz clock signal for DSP

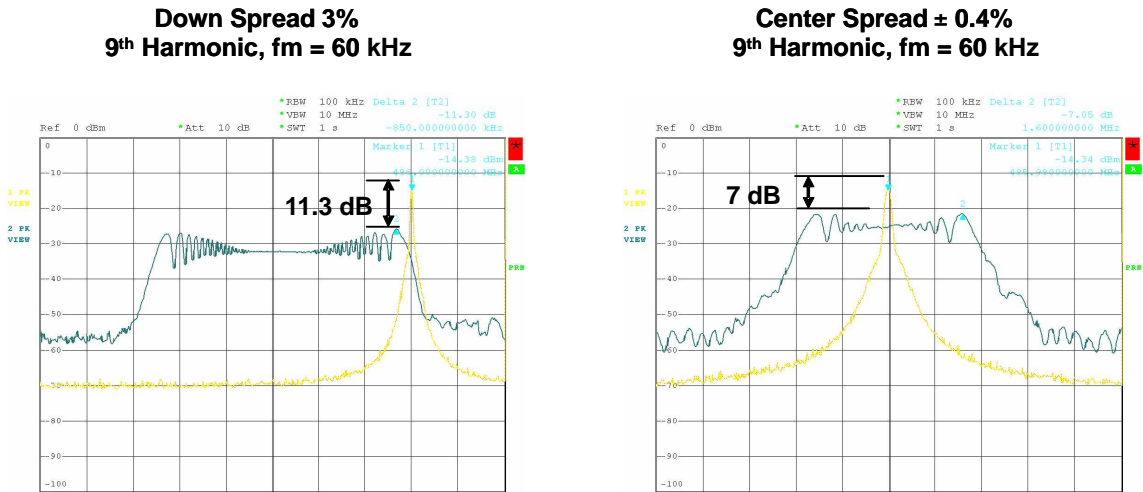


Figure 14. Spread Spectrum Clocking With Center Spread and Down Spread

The peak amplitude of the modulated clock is 11.3 dB lower than the non-modulated carrier frequency for down spread and radiated less electro-magnetic energy.

In SSC mode, the user can select the SSC modulation amount and SSC modulation frequency. The modulation amount is the frequency deviation based to the carrier (min/max frequency), whereas the modulation frequency determines the speed of the frequency variation. In SSC mode, the maximum VCO frequency is limited to 167 MHz.

SSC Modulation Amount

The CDCE706 supports center spread modulation and down spread modulation. In center spread, the clock is symmetrically shifted around the carrier frequency and can be $\pm 0.1\%$, $\pm 0.25\%$, and $\pm 0.4\%$. At down spread, the clock frequency is always lower than the carrier frequency and can be 1%, 1.5%, 2%, and 3%. The down spread is preferred if a system can not tolerate an operating frequency higher than the nominal frequency (over-clocking problem).

Example:

	Modulation Type	Minimum Frequency	Center Frequency	Maximum Frequency
A	$\pm 0.25\%$ center spread	53.865 MHz	54 MHz	54.135 MHz
B	1% down spread	53.46 MHz	—	54 MHz
C	0.5% down spread ⁽¹⁾	53.73 MHz	53.865 MHz	54 MHz

(1) A down spread of 0.5% of a 54-MHz carrier is equivalent to 53.865 MHz at a center spread of $\pm 0.25\%$.

SSC Modulation Frequency

The modulation frequency (sweep rate) can be selected between 30 kHz and 60 kHz. It also based on the VCO frequency as shown in the *SSC Modulation Frequency Selection* as shown on page 17. As shown in Figure 15, the damping increases with higher modulation frequencies. It may be limited by the tracking skew of a downstream PLL. The CDCE706 uses a triangle modulation profile which is one of the common profiles for SSC.

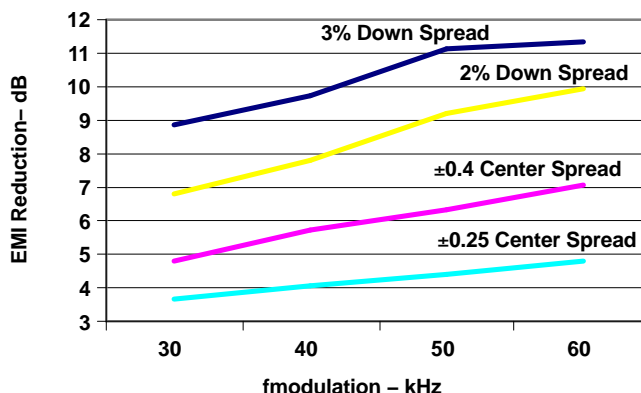


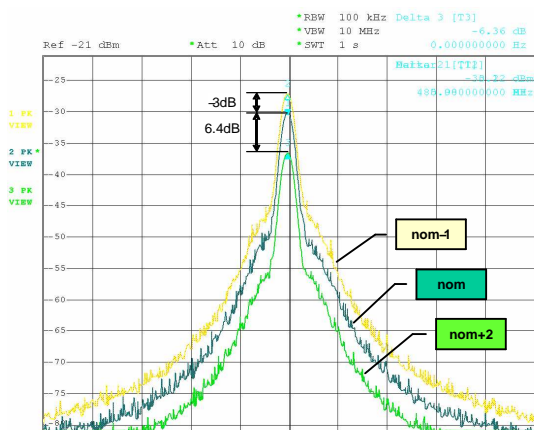
Figure 15. EMI Reduction vs $f_{\text{Modulation}}$ and f_{Amount}

Further EMI Reduction

The optimum damping is a combination of modulation amount, modulation frequency and the harmonics which are considered. Note that higher order harmonic frequencies results in stronger EMI reduction because of respective higher frequency deviation.

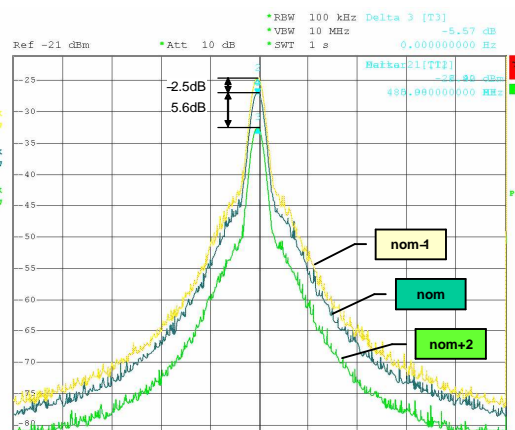
As seen in Figure 16 and Figure 17, a slower output slew rate and/or smaller output signal amplitude helps to reduce EMI emission even more. Both measures reduce the RF energy of clock harmonics. The CDCE706 allows slew rate control in four steps between 0.6 ns and 3.3 ns (Byte 19-24, Bit [5:4]). The output amplitude is set by the two independent output supply voltage pins, V_{CCOUT1} and V_{CCOUT2} , and can vary from 2.3 V to 3.6 V. Even a lower output supply voltage down to 1.8 V works, but the maximum frequency has to be considered.

Slew-Rate for $V_{\text{ccout}} = 2.5 \text{ V}$



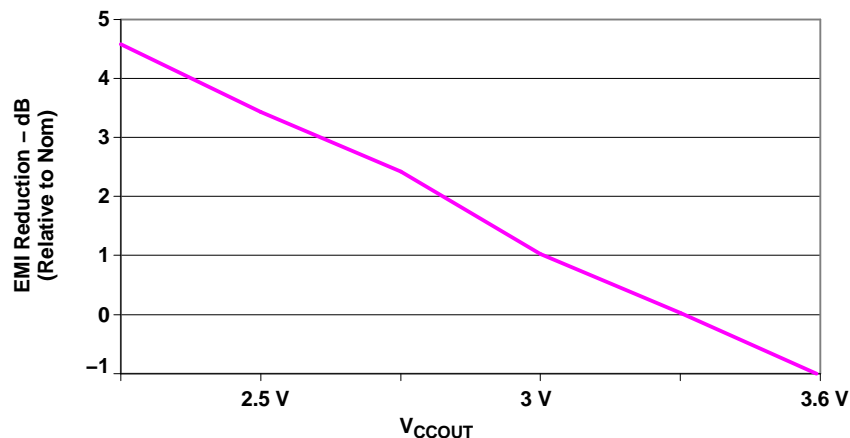
Date: 9.AUG.2005 14:19:49

Slew-Rate for $V_{\text{ccout}} = 3.3 \text{ V}$



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Figure 16. EMI Reduction vs Slew-Rate and V_{ccout}

Figure 17. EMI Reduction vs V_{CCOUT}

Multi-Function Control Inputs S0 and S1

The CDCE706 features two user definable inputs pins which can be used as external control pins or address pins. When programmed as control pins, they can function as clock select pin, enable/disable pin or device power-down pin. If both pins used as address-bits, up to four devices can be connected to the same SMBus. The respective function is set in Byte 10; Bit [3:0]. Table 4 shows the possible setting for the different output conditions, clock select and device addresses.

Table 4. Configuration Setting of Control Inputs

Configuration Bits				External Control Pins		Device Function			
Byte 10, Bit [3:2]		Byte 10, Bit [1:0]		S1 (Pin 2)	S0 (Pin 1)	Yx Outputs	Power Down	Pin 2	Pin 1
S11	S10	S01	S00						
0	X	0	X	1	1	Active	No	Output ctrl	Output ctrl
0	0	0	X	0	1	Low/High ⁽¹⁾	No	Output ctrl	Output ctrl
0	1	0	X	0	1	3-State	Outputs only	Output ctrl	Output ctrl
0	X	0	0	X	0	3-State	PLL, inputs and outputs	Output ctrl	Output ctrl and pd
0	X	0	1	0	0	S10=0: low/high ⁽¹⁾ S10=1: 3-State	PLL only	Output ctrl	PLL and Div bypass
0	X	0	1	1	0	Active	PLL only	Output ctrl	PLL and Div bypass
0	X	1	0	0	0/1 ⁽²⁾	S10=0: Low/High ⁽¹⁾ S10=1: 3-State	No	Output ctrl	CLK_SEL
0	X	1	0	1	0/1 ⁽²⁾	Active	No	Output ctrl	CLK_SEL
1	1	1	1	X	X	Active	No	A1 ⁽³⁾	A0 ⁽³⁾

(1) A non-inverting output will be set to low and an inverting output will be set to high.

(2) If S0 is 0, CLK_IN0 is selected; if S0 is 1, CLK_IN1 is selected.

(3) S0 and S1 are interpreted as Address Bit A0 and A1 of the Slave Receiver Address Byte.

As shown in Table 4, there is a specific order of the different output condition: Power-down mode overwrites 3-state, 3-state overwrites low-state, and low-state overwrites active-state.

Output Switching Matrix

The flexible architecture of the output switch matrix allows the user to switch any of the internal clock signal sources via a free-selectable post-divider to any of the six outputs.

As shown in Figure 18, the CDCE706 is based on two banks of switches and six post-dividers. Switch A comprises six 5-Input-Muxes which selects one of the four PLL clock outputs or directly selects the input clock and feed it to one of the 7-bit post-divider (P-Divider). Switch B is made up of six 6-Input-Muxes which takes any post-divider and feeds it to one of the six outputs, Yx.

Switch B was added to the output switch matrix to ensure that outputs frequencies derive from one P-divider are 100% phase aligned. Also, the P-divider is built in a way that every divide factor is automatically duty-cycle corrected. Changing the divider value on the fly may cause a glitch on the output.

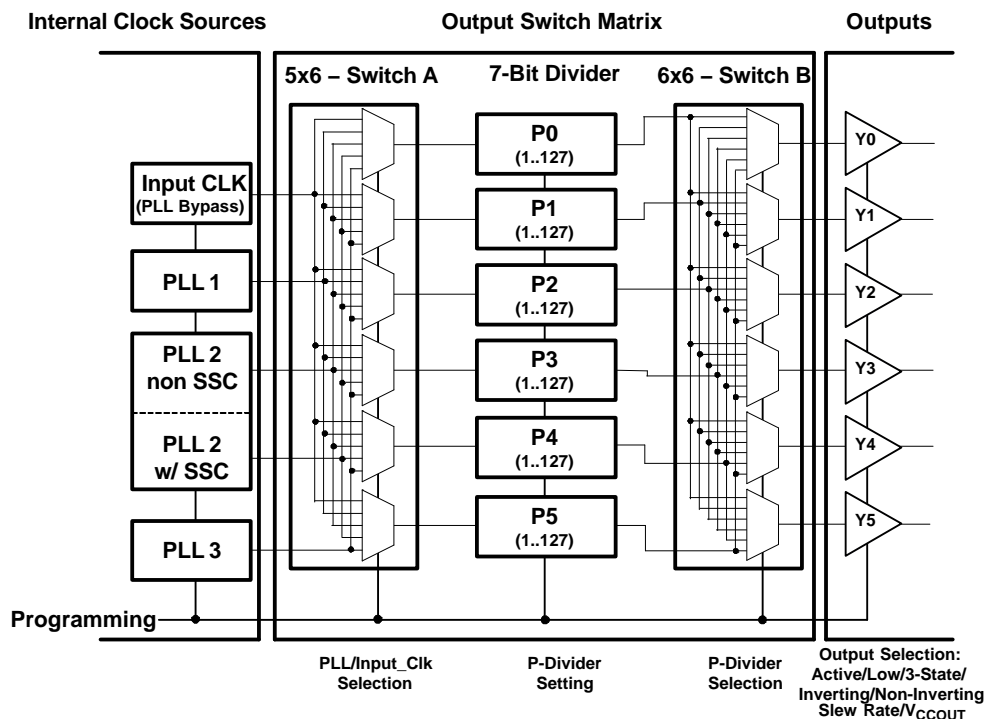


Figure 18. CDCE706 Output Switch Matrix

In addition, the outputs can be switched active, low or 3-state and/or 180 degree phase shifted. Also the outputs slew-rate and the output-voltage is user selectable.

LVCMOS Output Configuration

The output stage of the CDCE706 supports all common output setting, such as enable, disable, low-state and signal inversion (180 degree phase shift). It further features slew-rate control (0.6 ns to 3.3 ns) and variable output supply voltage (2.3 V to 3.6 V).

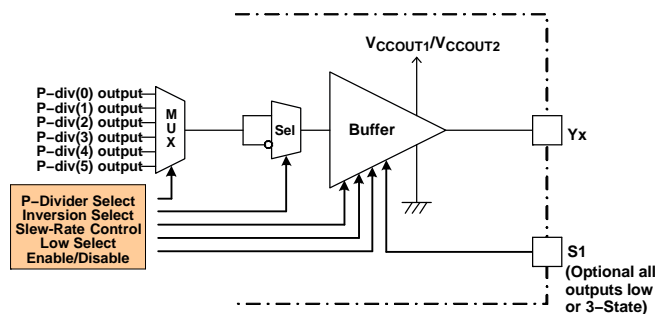


Figure 19. Block Diagram of Output Architecture

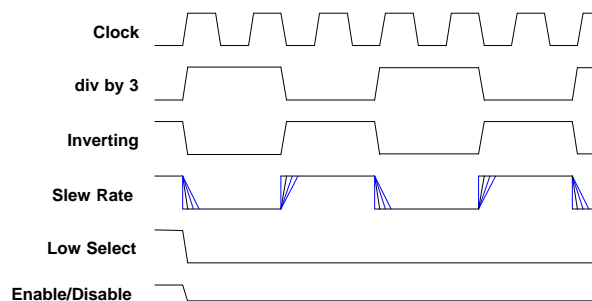


Figure 20. Example for Output Waveforms

All output settings are programmable via SMBus:

- enable, disable, low-state via external control pins S0 and S1 → Byte 10, Bit[3:0]
- enable or disable-to-low → Byte 19 to 24, Bit[3]
- inverting/non-inverting → Byte 19 to 24, Bit[6]
- slew-rate control → Byte 19 to 24, Bit[5:4]
- output swing → external pins V_{CCOUT1} (Pin 14) and V_{CCOUT2} (Pin 18)

Performance Data: Output Skew, Jitter, Cross Coupling, Noise Rejection (Spur-Suppression), and Phase Noise

Output Skew

Skew is an important parameter for clock distribution circuits. It is defined as the time difference between outputs that are driven by the same input clock. Table 5 shows the output skew ($t_{sk(o)}$) of the CDCE706 for high-to-low and low-to-high transitions over the entire range of supply voltages, operating temperature and output voltage swing.

Table 5. Output Skew

PARAMETER	V_{ccout}	TYP	MAX	UNIT
$t_{sk(o)}$	2.5 V	130	250	ps
	3.3 V	130	200	ps

Jitter Performance

Jitter is a major parameter for PLL-based clock driver circuits. This becomes important as speed increases and timing budget decreases. The PLL and internal circuits of CDCE706 are designed for lowest jitter. The peak-to-peak period jitter is only 60 ps (typical). Table 6 gives the peak-to-peak and rms deviation of cycle-to-cycle jitter, period jitter and phase jitter as taken during characterization.

Table 6. Jitter Performance of CDCE706

PARAMETER	f_{out}	TYP ⁽¹⁾		MAX ⁽¹⁾		UNIT
		Peak-Peak	rms (one sigma)	Peak-Peak	rms (one sigma)	
$t_{jit(cc)}$	50 MHz	55	–	75	–	ps
	133 MHz	50	–	85	–	
	245.76 MHz	45	–	60	–	
$t_{jit(per)}$	50 MHz	60	4	76	7	ps
	133 MHz	55	5	84	11	
	245.76 MHz	50	4	72	8	
$t_{jit(phase)}$	50 MHz	730	90	840	115	ps
	133 MHz	930	130	1310	175	
	245.76 MHz	720	90	930	125	

(1) All typical and maximum values are at $V_{CC} = 3.3$ V, temperature = 25°C, $V_{ccout} = 3.3$ V; one output is switching, data taken over several 10000 cycles.

Figure 21, Figure 22, and Figure 23 show the relationship between cycle-to-cycle jitter, period jitter, and phase jitter over 10000 samples. The jitter varies with a smaller or wider sample window. The cycle-to-cycle jitter and period jitter show the measured value whereas the phase jitter is the accumulated period jitter.

Cycle-to-Cycle jitter ($t_{jit(cc)}$) is the variation in cycle time of a clock signal between adjacent cycles, over a random sample of adjacent cycle pairs. Cycle-to-cycle jitter will never be greater than the period jitter. It is also known as adjacent cycle jitter.

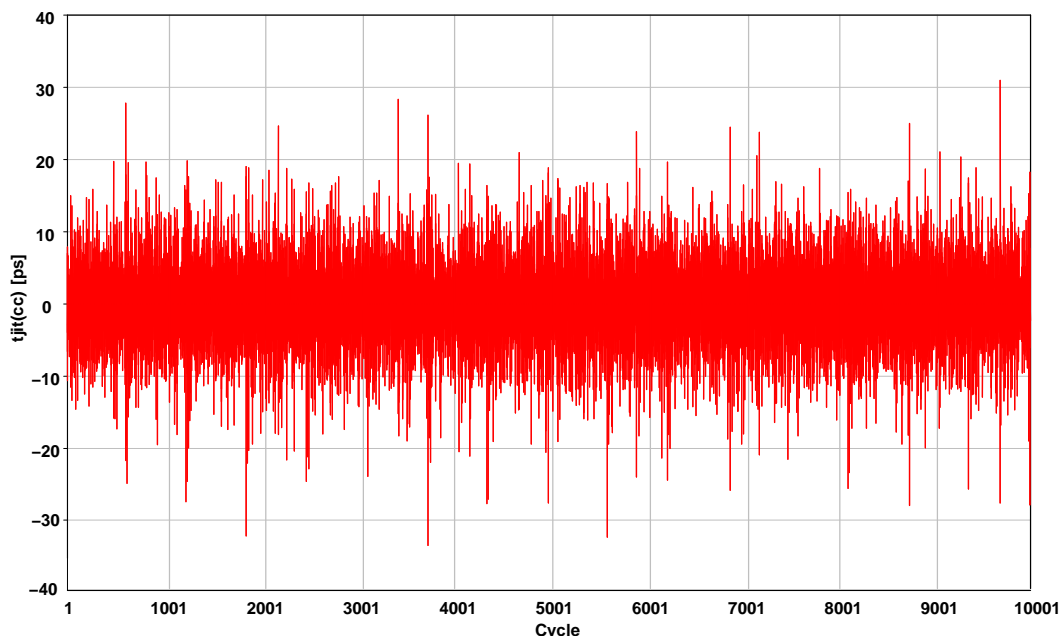


Figure 21. Snapshot of Cycle-to-Cycle Jitter

Period jitter ($t_{jit(per)}$) is the deviation in cycle time of a clock signal with respect to the ideal period ($1/f_0$) over a random sample of cycles. In reference to a PLL, period jitter is the worst-case period deviation from the ideal that would ever occur on the PLLs outputs. This is also referred to as short-term jitter.

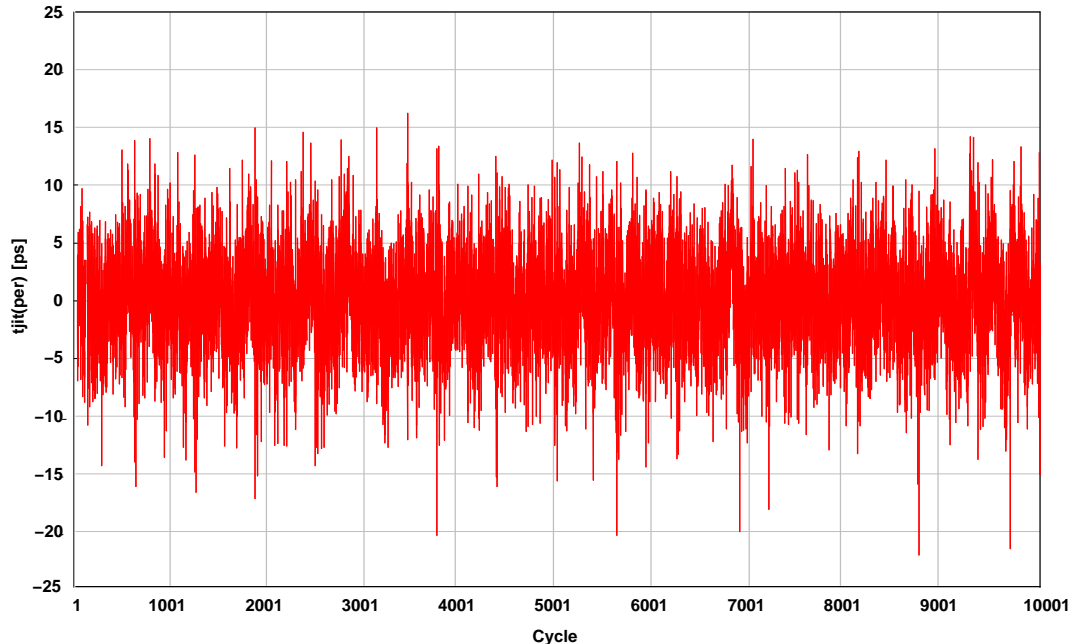


Figure 22. Snapshot of Period Jitter

Phase jitter ($t_{jit(phase)}$) is the long-term variation of the clock signal. It is the cumulative deviation in $t(\Theta)$ for a

controlled edge with respect to a $t(\Theta)$ mean in a random sample of cycles. Phase jitter, Time Interval Error (TIE), or Wander are used in literature to describe long-term variation in frequency. As of ITU-T: G.810, wander is defined as phase variation at rates less than 10 Hz while jitter is defined as phase variation greater than 10 Hz. The measurement interval must be long enough to gain a meaningful result. Wander can be caused by temperature drift, aging, supply voltage drift, etc.

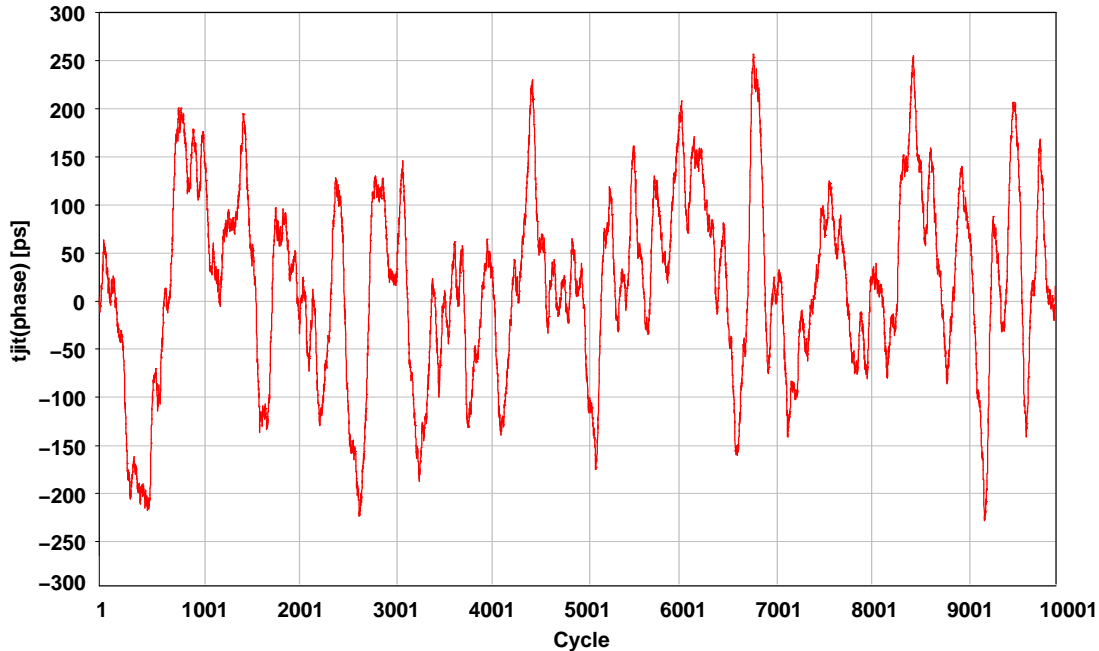


Figure 23. Snapshot of Phase Jitter

Cross Coupling, Spur Suppression and Noise Rejection

Cross-Coupling in ICs occurs through interactions between several parts of the chip such as between output stages, metal lines, bond wires, substrate, etc. The coupling can be capacitive, inductive and resistive (ohmic) induced by output switching, leakage current, ground bouncing, power supply transients, etc.

The CDCE706 is designed in BiCMOS process technology incorporating silicon-germanium (SiGe) technology. This process gives excellent performance in linearity, low power consumption, best-in-class noise performance and very good isolation characteristic between the on-chip components.

The good isolation was a major criteria to use BiCMOS process as it minimizes the coupling effect. Even if all three PLLs are active and all outputs are on, the noise suppression is clearly above 50 dB. [Figure 24](#) and [Figure 25](#) show an example of noise coupling, spur-suppression, and power supply noise rejection of CDCE706. Die respective measurement conditions are shown in [Figure 24](#) and [Figure 25](#).

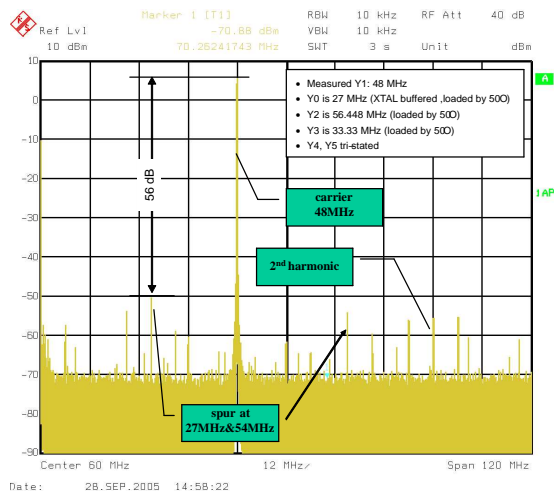


Figure 24. Noise Coupling and Spur Suppression

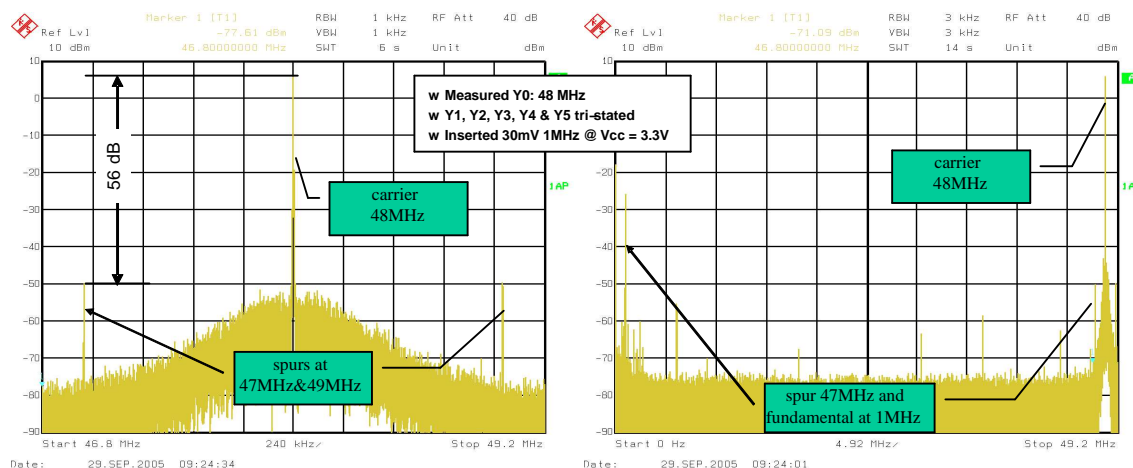


Figure 25. Power Supply Noise Rejection

Phase Noise Characteristic

In high-speed communication systems, the phase noise characteristic of the PLL frequency synthesizer is of high interest. Phase noise describes the stability of the clock signal in the frequency domain, similar to the jitter specification in the time domain.

Phase noise is a result of random and discrete noise causing a broad slope and spurious peaks. The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to phase noise. It can be the result of thermal noise, shot noise and/or flicker noise in active and passive devices.

Important factor for PLL synthesizer is the loop bandwidth (–3 dB cut-off frequency) — large LBW results in fast transient response but have less reference spur attenuation. The LBW of the CDCE706 is about 100 kHz to 150 kHz, dependent on selected PLL parameter.

For the CDCE706, two phase noise characteristics are of interest: The phase noise of the crystal-input stage and the phase noise of the internal PLL (VCO). The following Figure shows the respective phase noise characteristic.

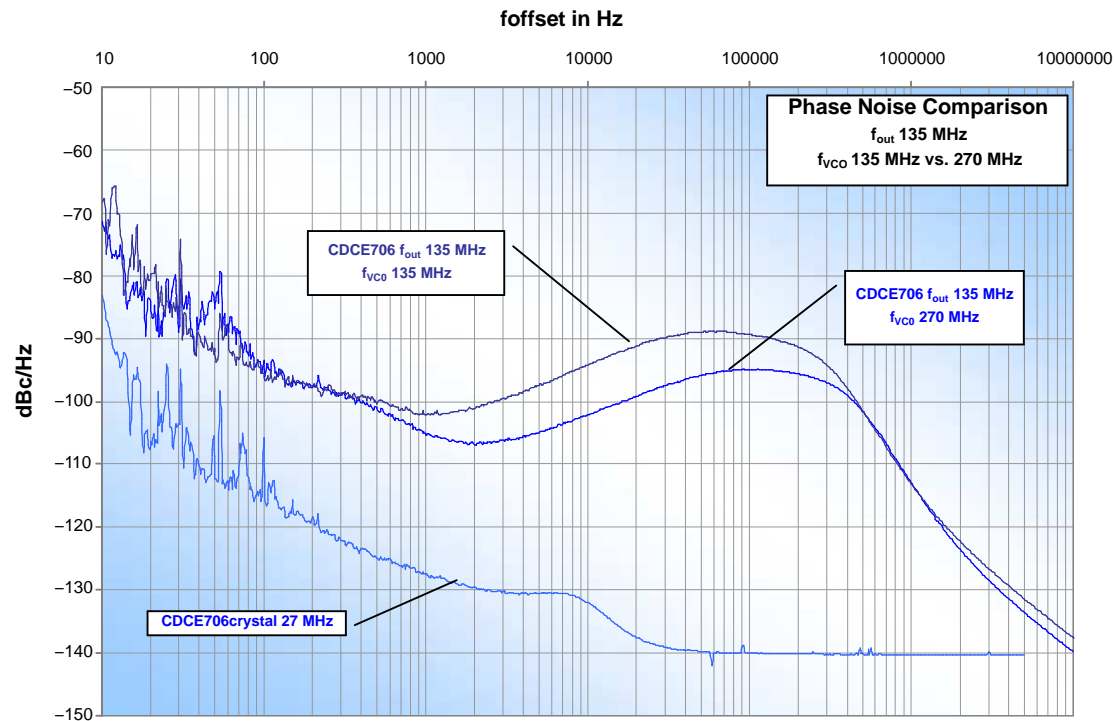


Figure 26. Phase Noise Characteristic

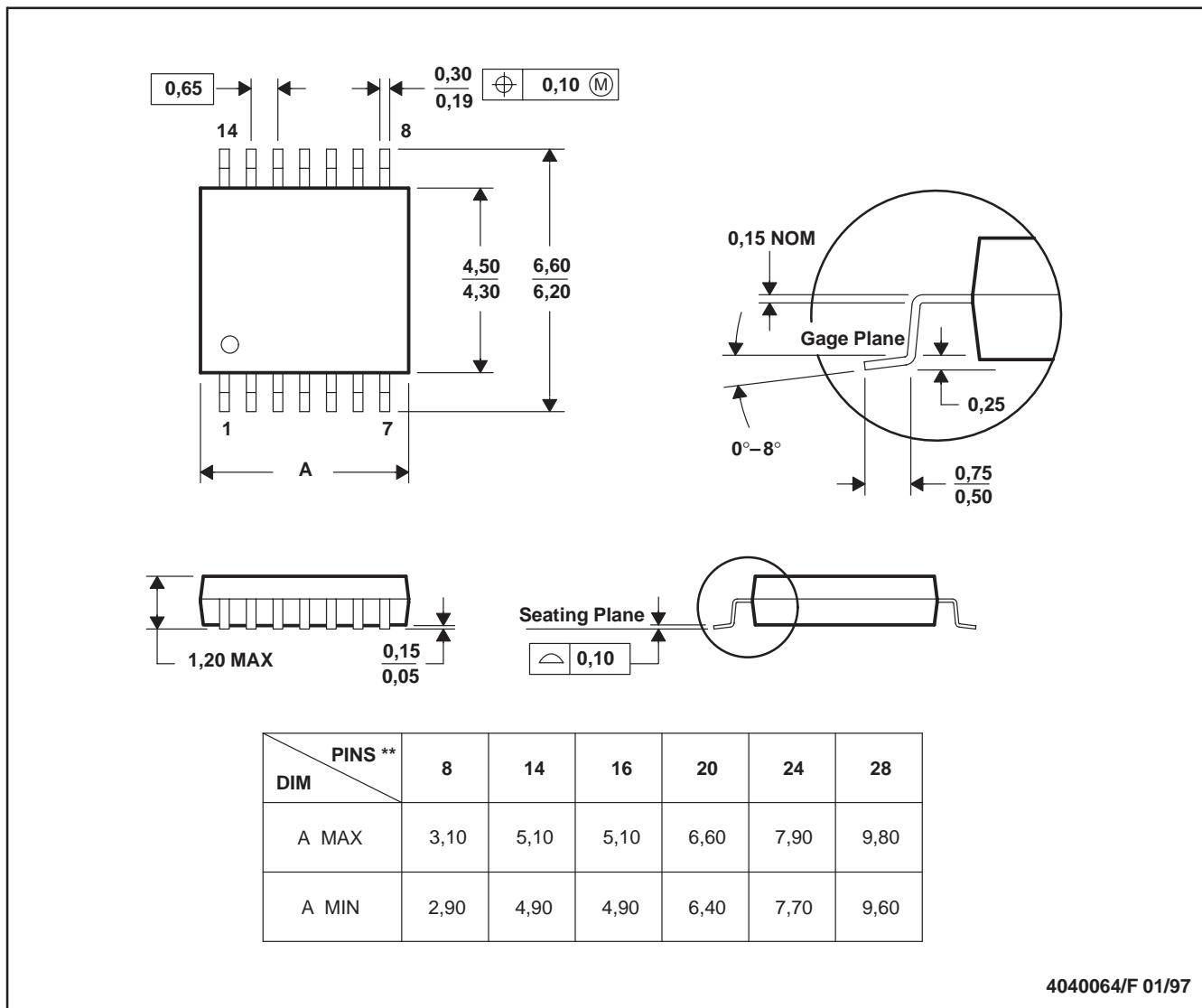
EVM and Programming SW

The CDCE706 comes with a development kit consisting of a performance evaluation module, the TI Pro Clock software, and the User's Guide. Contact Texas Instruments sales or marketing representative for more information.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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