

SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

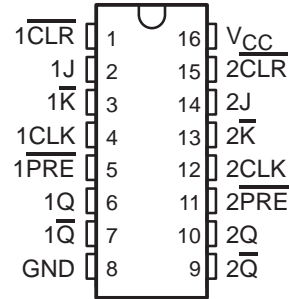
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS109A	50	6
'AS109A	129	29

description

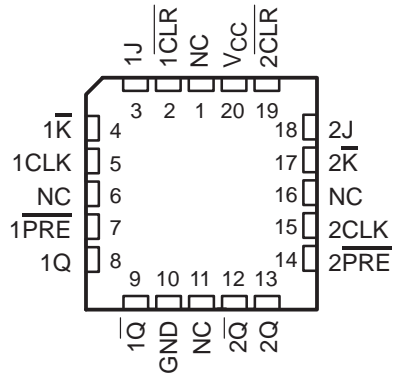
These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and $\overline{\text{K}}$ inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and $\overline{\text{K}}$ inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{\text{K}}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{\text{K}}$ are tied together.

The SN54ALS109A and SN54AS109A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS109A and SN74AS109A are characterized for operation from 0°C to 70°C .

SN54ALS109A, SN54AS109A ... J PACKAGE
SN74ALS109A, SN74AS109A ... D OR N PACKAGE
(TOP VIEW)



SN54ALS109A, SN54AS109A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q0	$\overline{\text{Q}}0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{\text{Q}}0$

[†] The output levels in this configuration are not specified to meet the minimum levels for V_{OH} if the lows at $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

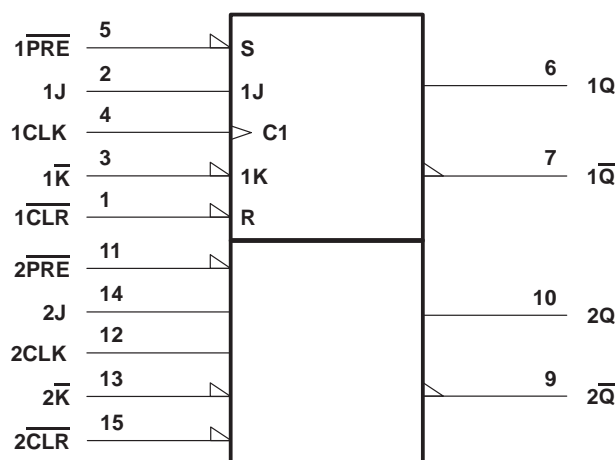
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DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS109A	–55°C to 125°C
SN74ALS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage		0.7			0.8			V		
I _{OH}	High-level output current		−0.4			−0.4			mA		
I _{OL}	Low-level output current		4			8			mA		
f _{clock}	Clock frequency		0	30		0	34		MHz		
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	15			15			ns		
		CLK high	16.5			14.5					
		CLK low	16.5			14.5					
t _{su}	Setup time before CLK↑	Data	15			15			ns		
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	10			10					
t _h	Hold time after CLK↑	Data	0			0			ns		
T _A	Operating free-air temperature		−55			125			0	70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS109A		SN74ALS109A		UNIT
			MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA	−1.5		−1.5		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA	V _{CC} − 2		V _{CC} − 2		V
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 4 mA		0.25 0.4		V
			I _{OL} = 8 mA		0.35 0.5		
I _I	CLK, J, or \overline{K}	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA
	\overline{PRE} or \overline{CLR}		0.2		0.2		
I _{IH}	CLK, J, or \overline{K}	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA
	\overline{PRE} or \overline{CLR}		40		40		
I _{IL}	CLK, J, or \overline{K}	V _{CC} = 5.5 V, V _I = 0.4 V	−0.2		−0.2		mA
	\overline{PRE} or \overline{CLR}		−0.4		−0.4		
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V	−20	−112	−30	−112	mA
I _{CC}		V _{CC} = 5.5 V, See Note 1	2.4	4	2.4	4	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with J, \overline{K} , CLK, and \overline{PRE} grounded, then with J, \overline{K} , CLK, and \overline{CLR} grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f _{max}			30		34		MHz
t _{PLH}	PRE or CLR	Q or Q̄	3	17	3	13	ns
t _{PHL}			5	17	5	15	
t _{PLH}	CLK	Q or Q̄	5	21	5	16	ns
t _{PHL}			5	20	5	18	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54AS109A	–55°C to 125°C
SN74AS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS109A			SN74AS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		−2			−2			mA
I _{OL}	Low-level output current		20			20			mA
f _{clock} *	Clock frequency		0	90		0	105		MHz
t _w *	Pulse duration	PRE or CLR low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t _{su} *	Setup time before CLK↑	Data	5.5			5.5			ns
		PRE or CLR inactive	2			2			
t _h *	Hold time after CLK↑	Data	0			0			ns
T _A	Operating free-air temperature		−55	125		0	70		°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109A			SN74AS109A			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2			–1.2	V
V_{OH}		$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}		$V_{CC} = 4.5$ V,	$I_{OL} = 20$ mA		0.25	0.5		0.25	0.5	V
I_I		$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	CLK, J, or \overline{K}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μ A
	\overline{PRE} or \overline{CLR}					40			40	
I_{IL}	CLK, J, or \overline{K}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.5			–0.5	mA
	\overline{PRE} or \overline{CLR}					–1.8			–1.8	
I_{O}^{\S}		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	–30		–112	–30		–112	mA
I_{CC}		$V_{CC} = 5.5$ V,	See Note 1		11.5	17		11.5	17	mA

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with J, \overline{K} , CLK, and \overline{PRE} grounded, then with J, K, CLK, and \overline{CLR} grounded.



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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS109A		SN74AS109A		
			MIN	MAX	MIN	MAX	
f _{max} *			90		105		MHz
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	2	9	2	8	ns
t _{PHL}			3.5	11.5	3.5	10.5	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	2.5	10	2.5	9	ns
t _{PHL}			3.5	10.5	3.5	9	

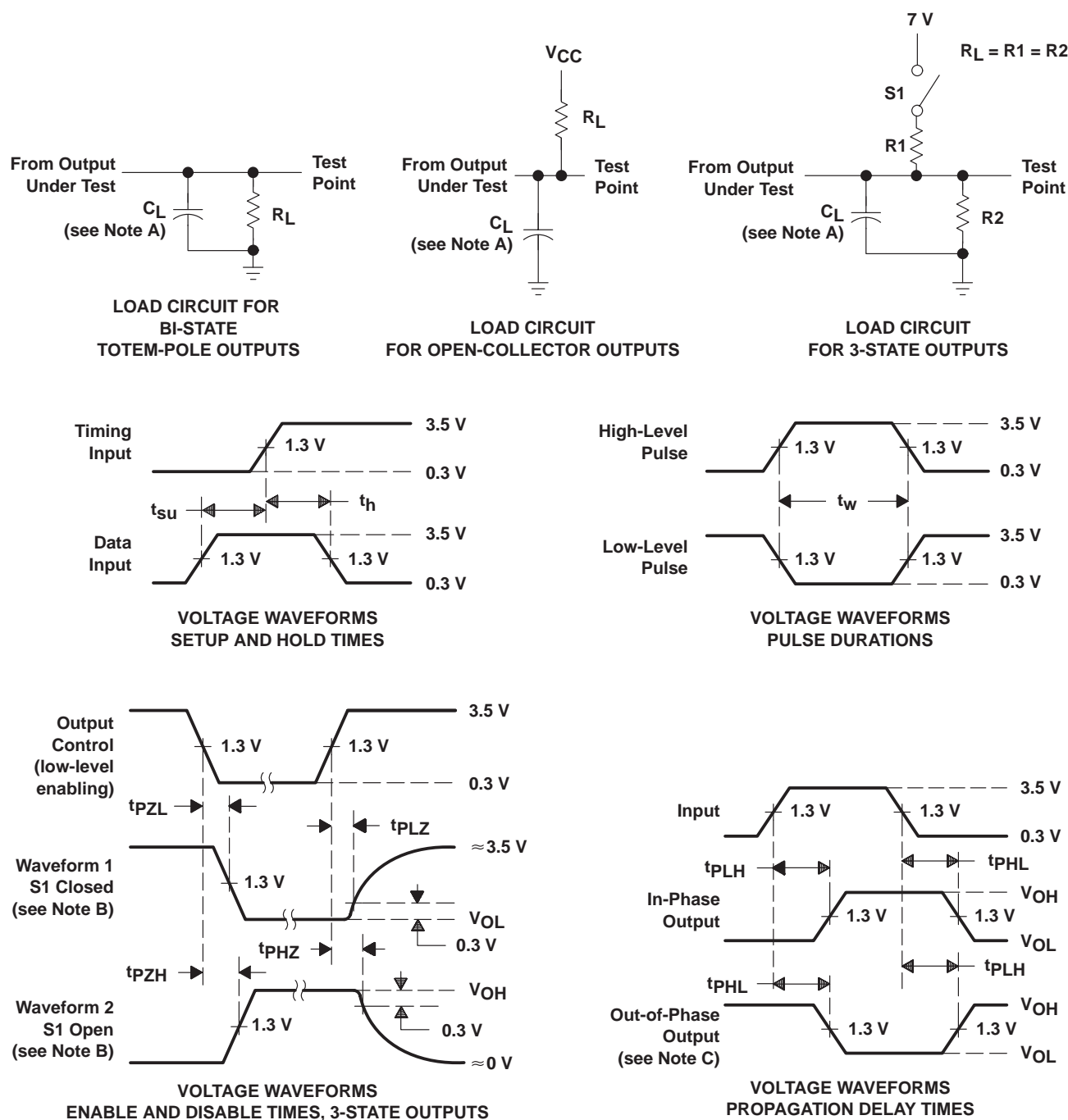
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† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
84000012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8400001EA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
8400001FA	OBSOLETE	CFP	W	16		None	Call TI	Call TI
JM38510/37102B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/37102BEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SN54ALS109AJ	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SN54AS109AJ	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SN74ALS109AD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS109ADR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS109AN3	OBSOLETE	PDIP	N	16		None	Call TI	Call TI
SN74ALS109ANSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AS109AD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AS109ADR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AS109AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AS109ANSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54ALS109AFK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54ALS109AJ	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
SNJ54AS109AFK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54AS109AJ	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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