

SN54LVC540A, SN74LVC540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)

description

The SN54LVC540A octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC540A octal buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

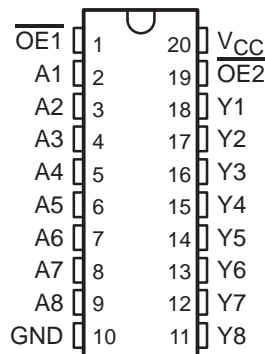
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

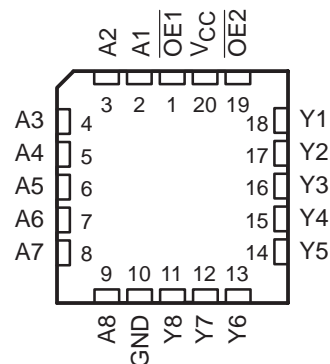
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVC540A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC540A is characterized for operation from -40°C to 85°C .

SN54LVC540A . . . J OR W PACKAGE
SN74LVC540A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVC540A . . . FK PACKAGE
(TOP VIEW)



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**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LVC540A		SN74LVC540A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating		2	3.6	1.65	3.6	V
	Data retention only		1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				1.7		
	$V_{CC} = 2.7$ V to 3.6 V		2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V				$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V				0.7		
	$V_{CC} = 2.7$ V to 3.6 V			0.8	0.8		
V_I Input voltage			0	5.5	0	5.5	V
V_O Output voltage	High or low state		0	V_{CC}	0	V_{CC}	V
	3 state		0	5.5	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V				–4		mA
	$V_{CC} = 2.3$ V				–8		
	$V_{CC} = 2.7$ V			–12	–12		
	$V_{CC} = 3$ V			–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V				4		mA
	$V_{CC} = 2.3$ V				8		
	$V_{CC} = 2.7$ V			12	12		
	$V_{CC} = 3$ V			24	24		
T_A Operating free-air temperature			–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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OCTAL BUFFERS/DRIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	SN54LVC540A			SN74LVC540A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA		1.65 V to 3.6 V				V _{CC} –0.2			V
			2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA		1.65 V				1.2			
	I _{OH} = –8 mA		2.3 V				1.7			
	I _{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I _{OH} = –24 mA		3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA		1.65 V to 3.6 V				0.2			V
			2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA		1.65 V				0.45			
	I _{OL} = 8 mA		2.3 V				0.7			
	I _{OL} = 12 mA		2.7 V	0.4			0.4			
	I _{OL} = 24 mA		3 V	0.55			0.55			
I _I	V _I = 0 to 5.5 V		3.6 V	±5			±5			μA
I _{off}	V _I or V _O = 5.5 V		0				±10			μA
I _{OZ}	V _O = 0 to 5.5 V		3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	10			10			μA
	3.6 V ≤ V _I ≤ 5.5 V‡			10			10			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND		3.3 V	4			4			pF
C _o	V _O = V _{CC} or GND		3.3 V	5.5			5.5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC540A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A	Y	7.1		1	5.3	ns
t _{en}	$\overline{\text{OE}}$	Y	8		1	6.6	ns
t _{dis}	$\overline{\text{OE}}$	Y	8.2		1	7.4	ns



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC540A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	†	†	†	†	7.1		1.4	5.3	ns
t _{en}	\overline{OE}	Y	†	†	†	†	8		1.1	6.6	ns
t _{dis}	\overline{OE}	Y	†	†	†	†	8.2		1.8	7.4	ns
t _{sk(o)} [‡]									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$	†	†	31	pF
		Outputs disabled		†	†	3	

† This information was not available at the time of publication.

SN54LVC540A, SN74LVC540A

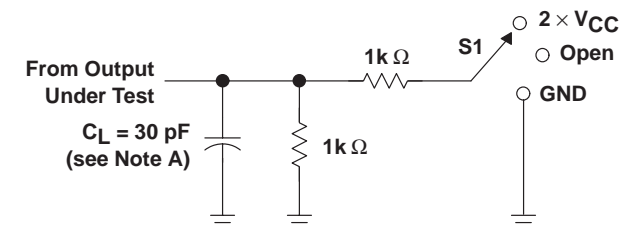
OCTAL BUFFERS/DRIVERS

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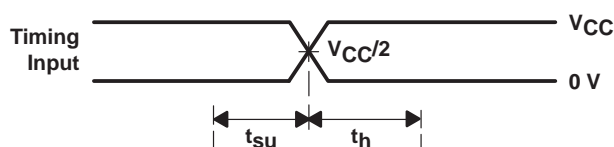
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

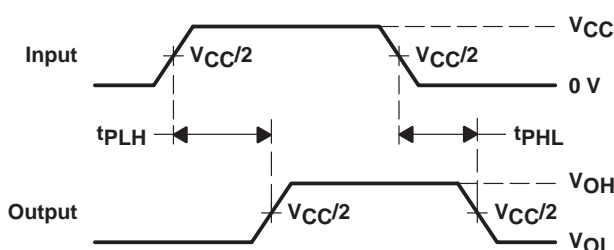


LOAD CIRCUIT

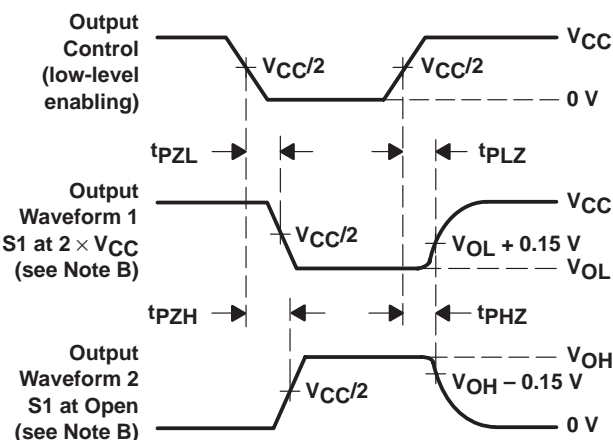
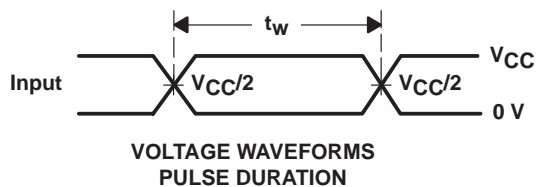
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



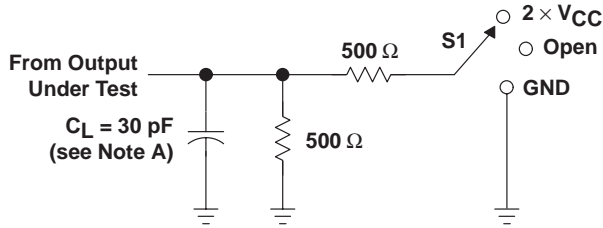
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

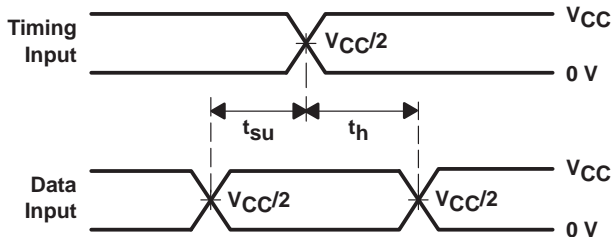
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

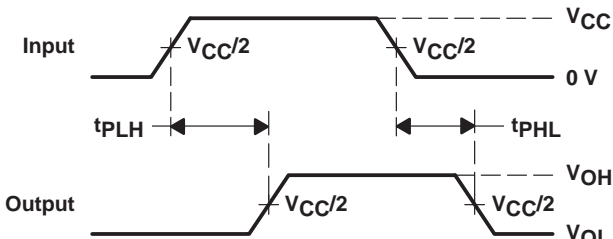


LOAD CIRCUIT

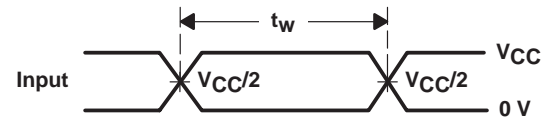
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



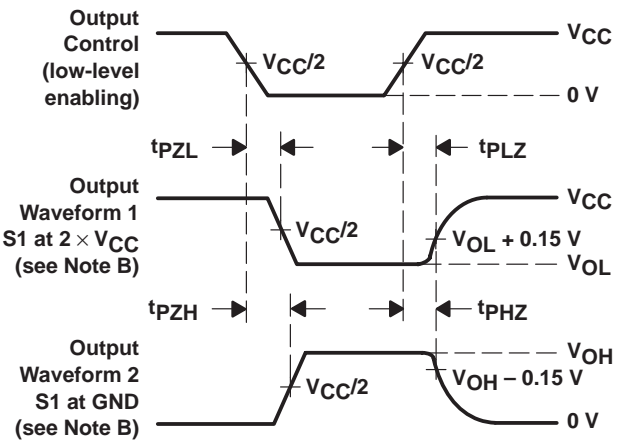
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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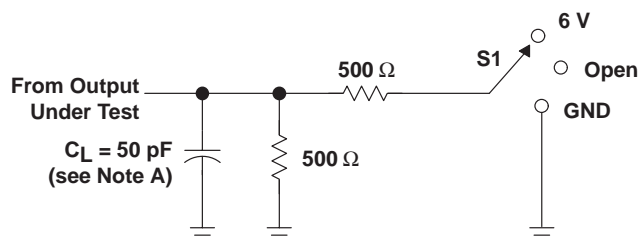
OCTAL BUFFERS/DRIVERS

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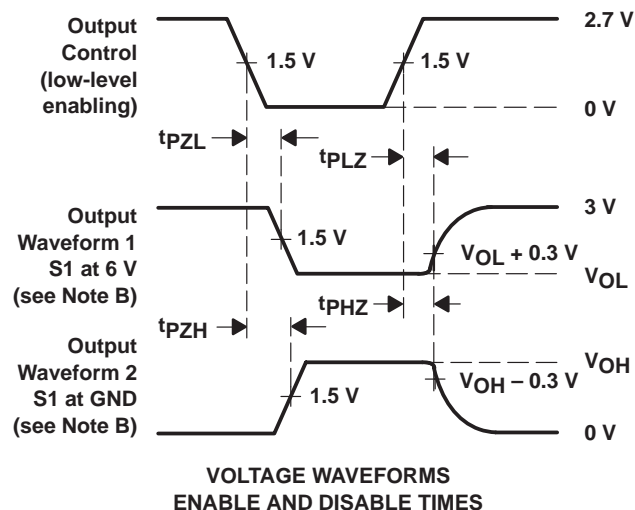
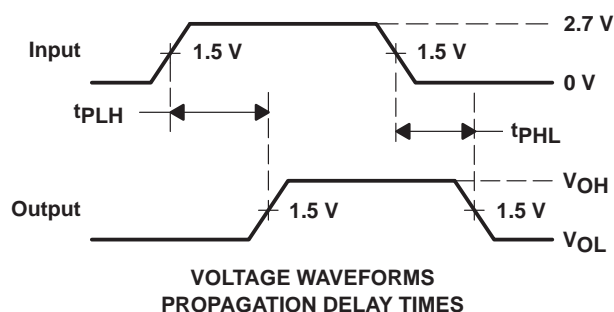
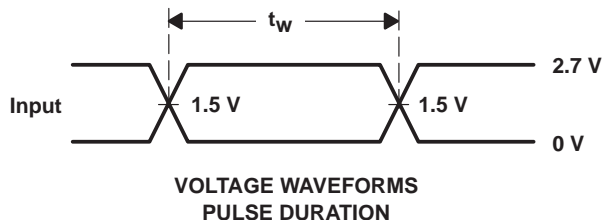
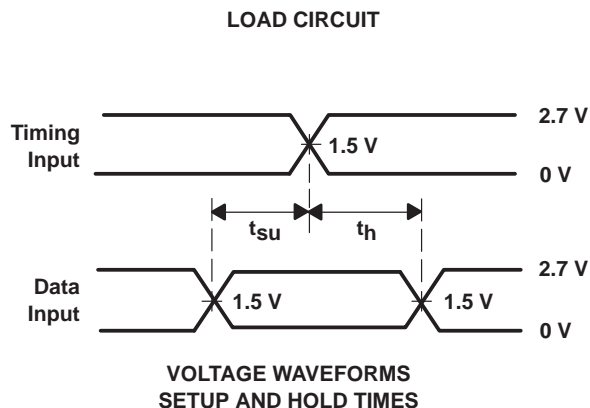
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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