

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- pnp Inputs Reduce dc Loading on Data Lines

description

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

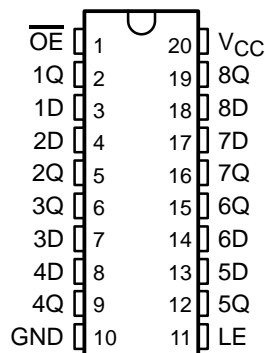
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

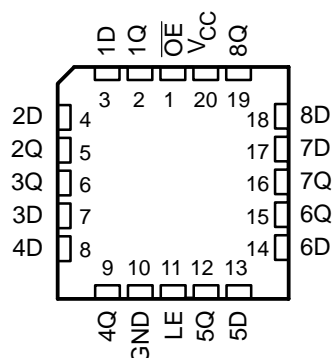
SN54ALS373A, . . . J OR W PACKAGE

SN54AS373 . . . J PACKAGE

SN74ALS373A, SN74AS373 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS373A, SN54AS373 . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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SDAS083C – APRIL 1982 – REVISED MARCH 2002

ORDERING INFORMATION

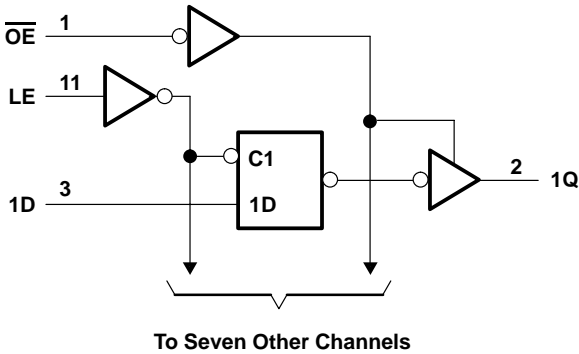
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS373AN	SN74ALS373AN
			SN74AS373N	SN74AS373N
	SOIC – DW	Tube	SN74ALS373ADW	ALS373A
		Tape and reel	SN74ALS373ADWR	
		Tube	SN74AS373DW	AS373
		Tape and reel	SN74AS373DWR	
–55°C to 125°C	SOP – NS	Tape and reel	SN74ALS373ANSR	ALS373A
			SN74AS373NSR	74AS373
	CDIP – J	Tube	SNJ54ALS373AJ	SNJ54ALS373AJ
			SNJ54AS373J	SNJ54AS373J
	CFP – W	Tube	SNJ54ALS373AW	SNJ54ALS373AW
			SNJ54ALS373AFK	SNJ54ALS373AFK
	LCCC – FK	Tube	SNJ54AS373FK	SNJ54AS373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic diagram (positive logic)



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

absolute maximum ratings over operating free-air temperature range (SN54ALS373A, SN74ALS373A) (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54ALS373A			SN74ALS373A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ALS373A		SN74ALS373A		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration, LE high	12		10		ns
t_{su}	Setup time, data before LE↓	10		10		ns
t_h	Hold time, data after LE↓	7		7		ns



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373A		SN74ALS373A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.5		−1.5			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} −2		V _{CC} −2			V
	V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4	3.3				
		I _{OH} = −2.6 mA			2.4	3.2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
		I _{OL} = 24 mA			0.35	0.5		
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		20		20			μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		−20		−20			μA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20		20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		−0.1		−0.1			mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		−20	−112	−30	−112		mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	9	16	9	16		mA
		Outputs low	16	25	16	25		
		Outputs disabled	17	27	17	27		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS373A		SN74ALS373A		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	2	17	2	12	ns
t _{PHL}			1	19	4	16	
t _{PLH}	LE	Any Q	6	29	6	22	ns
t _{PHL}			1	27	7	23	
t _{PZH}	\overline{OE}	Any Q	6	22	1	18	ns
t _{PZL}			5	24	5	20	
t _{PHZ}	\overline{OE}	Any Q	2	16	1	10	ns
t _{PLZ}			2	24	2	12	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

absolute maximum ratings over operating free-air temperature range (SN54AS373, SN74AS373) (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54AS373		SN74AS373		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration, LE high	5.5*		4.5*		ns
t_{su}	Setup time, data before LE↓	2*		2*		ns
t_h	Hold time, data after LE↓	3*		3*		ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS373			SN74AS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA		V _{CC} −2			V _{CC} −2			V
	V _{CC} = 4.5 V	I _{OH} = −12 mA	2.4	3.2					
		I _{OH} = −15 mA			2.4	3.3			
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 32 mA	0.27	0.5					V
		I _{OL} = 48 mA			0.32	0.5			
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		50			50			μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		−50			−50			μA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		−0.02	−0.5	−0.02		−0.5	mA	
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		−30	−112	−30	−112			mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	55	90	55	90			mA
		Outputs low	55	85	55	85			
		Outputs disabled	65	100	65	100			

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

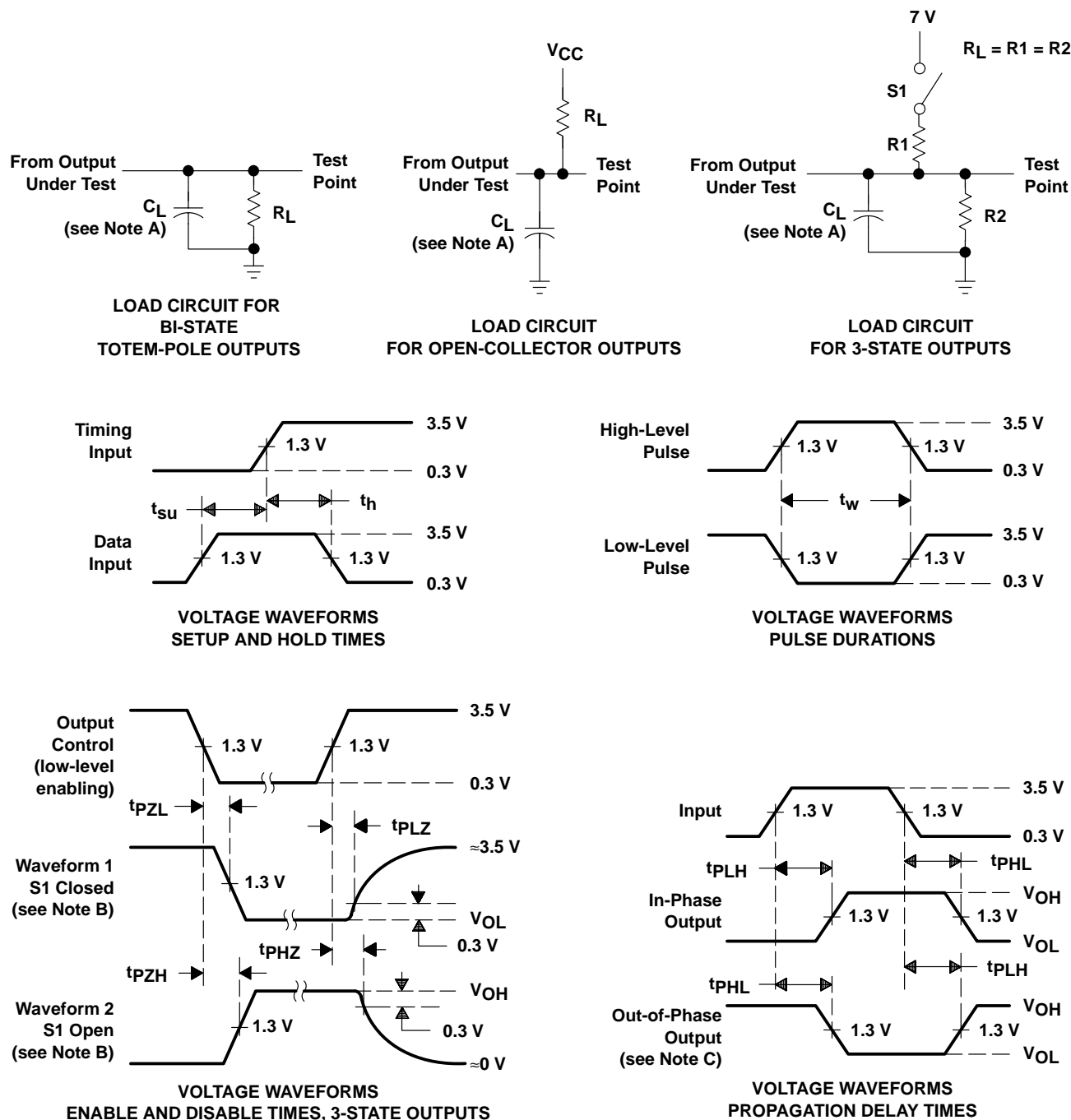
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	3	9	3.5	6	ns
t _{PHL}			3	8	3.5	6	
t _{PLH}	LE	Any Q	6.5	14.5	6.5	11.5	ns
t _{PHL}			5	9	5	7.5	
t _{PZH}	$\overline{\text{OE}}$	Any Q	2	7.5	2	6.5	ns
t _{PZL}			4.5	10.5	4.5	9.5	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	3	10	3	6.5	ns
t _{PLZ}			3	8	3	7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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SDAS083C – APRIL 1982 – REVISED MARCH 2002

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
83020012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8302001RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8302001SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
JM38510/37203B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/37203BRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SN54ALS373AJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SN54AS373J	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SN74ALS373ADBLE	OBSOLETE	SSOP	DB	20		None	Call TI	Call TI
SN74ALS373ADBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS373ADW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS373ADWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS373AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS373AN3	OBSOLETE	PDIP	N	20		None	Call TI	Call TI
SN74ALS373ANSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AS373DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AS373DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AS373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AS373N3	OBSOLETE	PDIP	N	20		None	Call TI	Call TI
SN74AS373NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54ALS373AFK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54ALS373AJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SNJ54ALS373AW	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
SNJ54AS373FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54AS373J	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens,

including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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