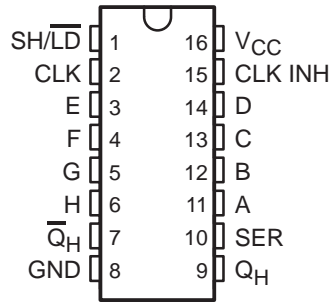


# SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

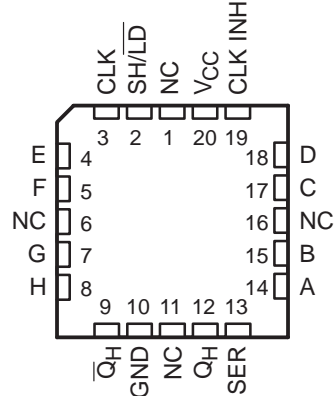
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 13$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

SN54HC165 . . . J OR W PACKAGE  
SN74HC165 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC165 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HC165 devices are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial ( $Q_H$ ) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load ( $SH/LD$ ) input. The 'HC165 devices also feature a clock-inhibit ( $CLK$  INH) function and a complementary serial ( $\bar{Q}_H$ ) output.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC165N	SN74HC165N
	SOIC – D	Tube of 40	SN74HC165D	HC165
		Reel of 2500	SN74HC165DR	
		Reel of 250	SN74HC165DT	
	SOP – NS	Reel of 2000	SN74HC165NSR	HC165
	SSOP – DB	Reel of 2000	SN74HC165DBR	HC165
–55°C to 125°C	TSSOP – PW	Tube of 90	SN74HC165PW	HC165
		Reel of 2000	SN74HC165PWR	
		Reel of 250	SN74HC165PWT	
	CDIP – J	Tube of 25	SNJ54HC165J	SNJ54HC165J
	CFP – W	Tube of 150	SNJ54HC165W	SNJ54HC165W
	LCCC – FK	Tube of 55	SNJ54HC165FK	SNJ54HC165FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## SN54HC165, SN74HC165

## 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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**description/ordering information (continued)**

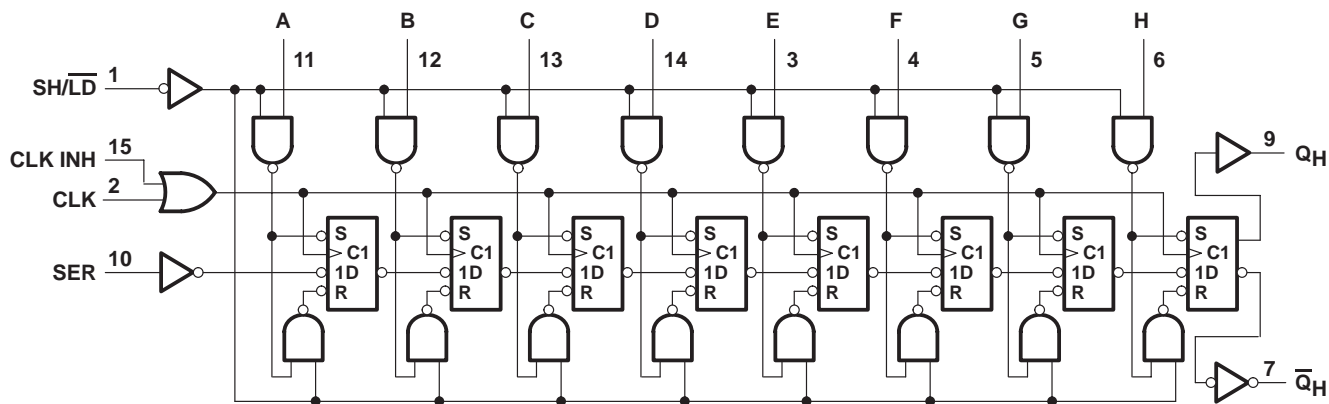
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while  $\overline{\text{SH}/\overline{\text{LD}}}$  is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when  $\overline{\text{SH}/\overline{\text{LD}}}$  is held high. While  $\overline{\text{SH}/\overline{\text{LD}}}$  is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

## FUNCTION TABLE

INPUTS			FUNCTION
SH/LD	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift↑
H	↑	L	Shift↑

† Shift = content of each internal register shifts toward serial output  $Q_H$ . Data at SER is shifted into the first register.

**logic diagram (positive logic)**

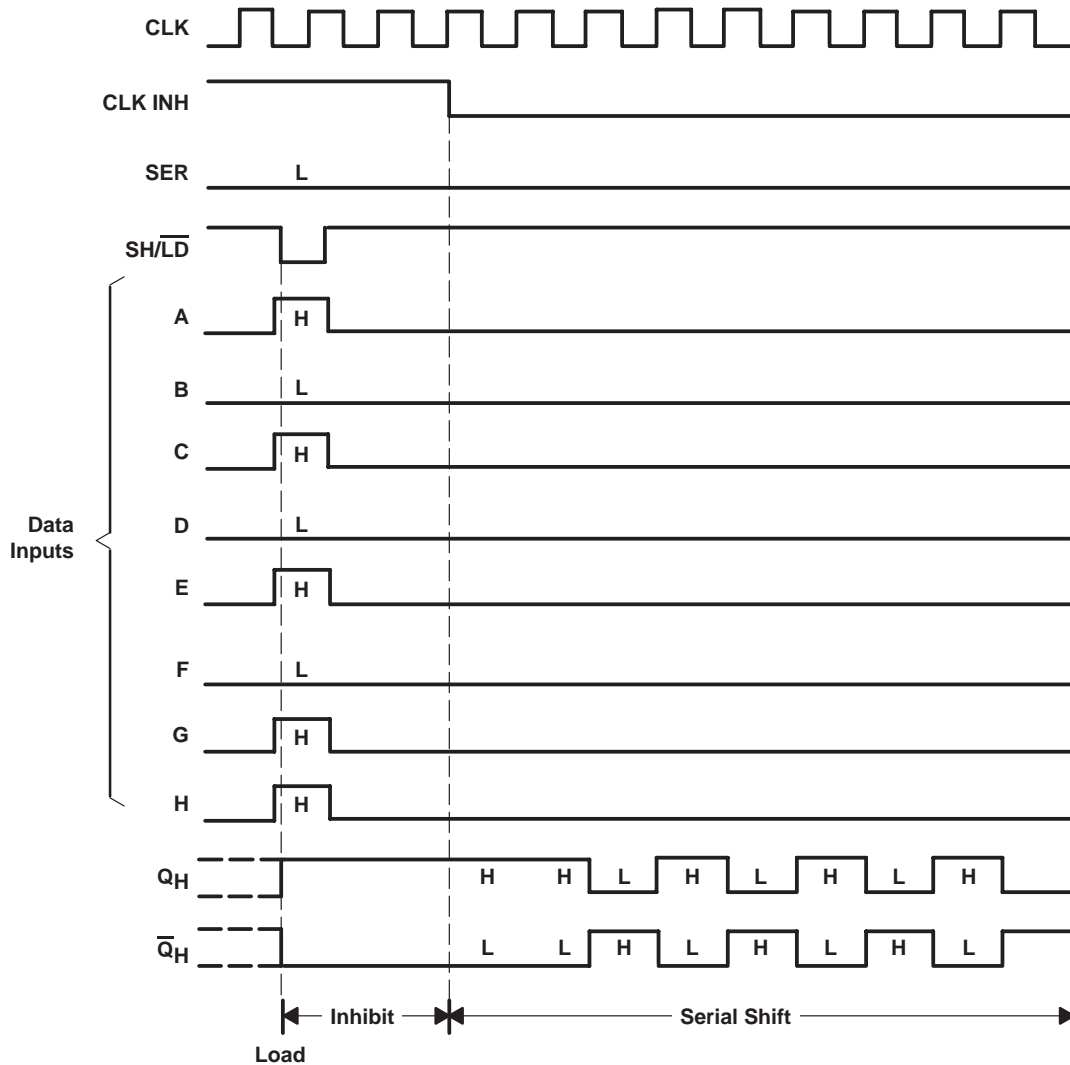


Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

# SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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## typical shift, load, and inhibit sequence



# SN54HC165, SN74HC165

## 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

			SN54HC165			SN74HC165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5			1.5			V
		V <sub>CC</sub> = 4.5 V	3.15			3.15			
		V <sub>CC</sub> = 6 V	4.2			4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5			0.5			V
		V <sub>CC</sub> = 4.5 V	1.35			1.35			
		V <sub>CC</sub> = 6 V	1.8			1.8			
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
Δt/Δv‡	Input transition rise/fall time	V <sub>CC</sub> = 2 V	1000			1000			ns
		V <sub>CC</sub> = 4.5 V	500			500			
		V <sub>CC</sub> = 6 V	400			400			
T <sub>A</sub>	Operating free-air temperature		−55	125		−40	85		°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

<sup>‡</sup> If this device is used in the threshold region (from  $V_{ILmax} = 0.5$  V to  $V_{IHmin} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

# SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	µA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF



# SN54HC165, SN74HC165

## 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC165		SN74HC165		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V		6		4.2		5	MHz
		4.5 V		31		21		25	
		6 V		36		25		29	
t <sub>w</sub>	SH/ $\overline{\text{LD}}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t <sub>su</sub>	SH/ $\overline{\text{LD}}$ high before CLK↑	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	SER before CLK↑	2 V	40		60		50		
		4.5 V	8		12		10		
		6 V	7		10		9		
	CLK INH low before CLK↑	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
	CLK INH high before CLK↑	2 V	40		60		50		
		4.5 V	8		12		10		
		6 V	7		10		9		
	Data before SH/ $\overline{\text{LD}}$ ↓	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
t <sub>h</sub>	SER data after CLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		
	PAR data after SH/ $\overline{\text{LD}}$ ↓	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		

# SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			2 V	6	13		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	62		25		29		
$t_{pd}$	SH/ $\overline{LD}$	$Q_H$ or $\overline{Q}_H$	2 V		80	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		16	26		38		32	
	CLK	$Q_H$ or $\overline{Q}_H$	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	H	$Q_H$ or $\overline{Q}_H$	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
		Any	2 V		38	75		110		95	
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics,  $T_A = 25^\circ\text{C}$

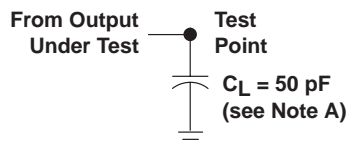
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	75	pF



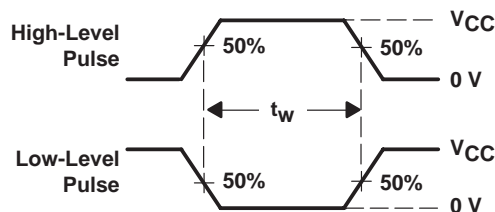
# SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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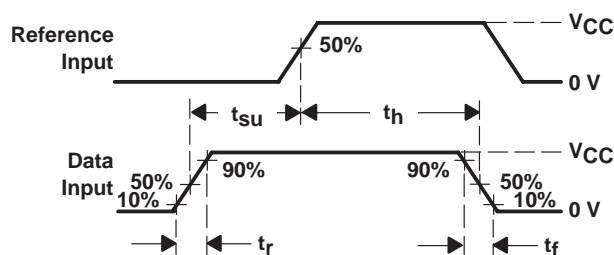
## PARAMETER MEASUREMENT INFORMATION



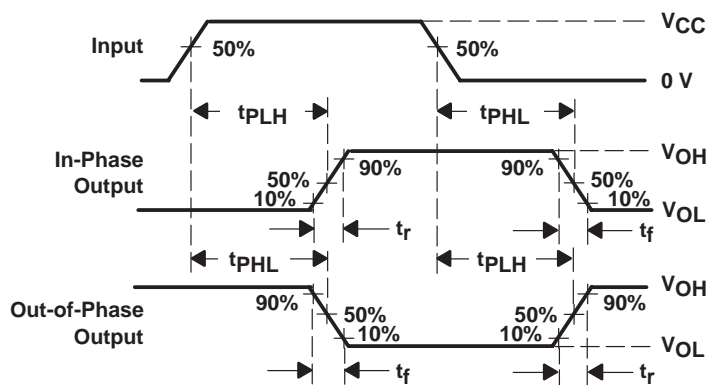
LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
84095012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
8409501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
8409501FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN54HC165J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN74HC165D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74HC165N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74HC165NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74HC165NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
SN74HC165PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165PWG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC165PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC165FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54HC165J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54HC165W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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