

SN54290, SN54293, SN54LS290, SN54LS293 SN74290, SN74293, SN74LS290, SN74LS293 DECADE AND 4-BIT BINARY COUNTERS

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'290, 'LS290 . . . DECADE COUNTERS
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

- GND and V_{CC} on Corner Pins
(Pins 7 and 14 Respectively)

description

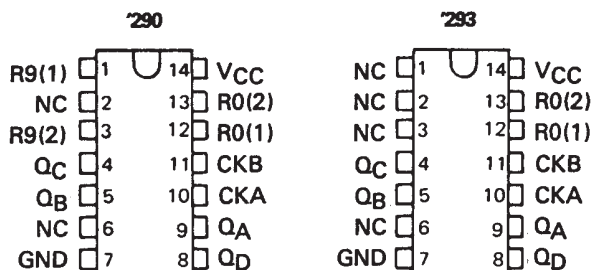
The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

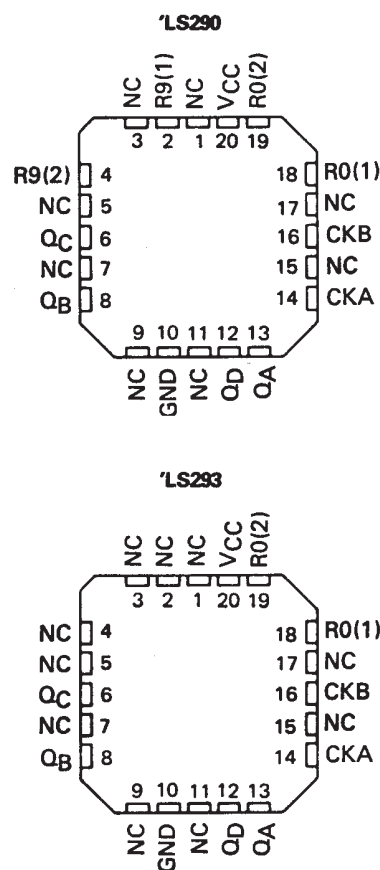
All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

SN54290, SN54LS290, SN54293,
SN54LS293 . . . J OR W PACKAGE
SN74290, SN74293 . . . N PACKAGE
SN74LS290, SN74LS293 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS290, SN54LS293 . . . FK PACKAGE
(TOP VIEW)

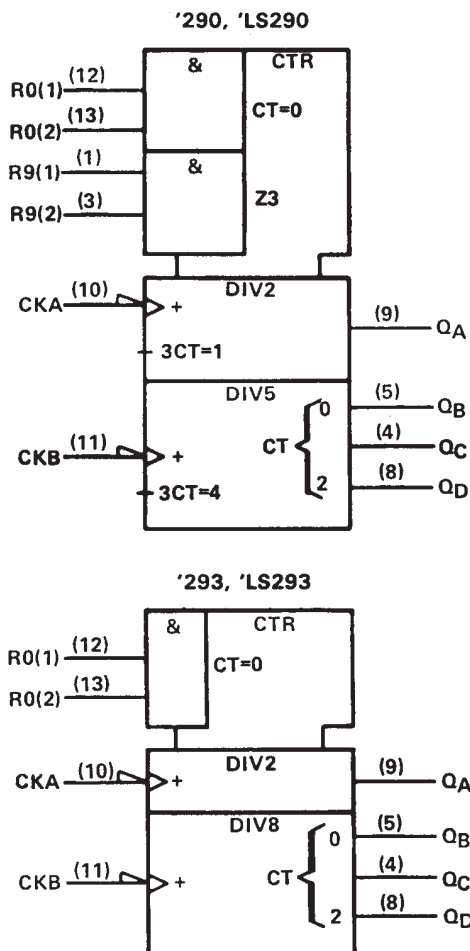


NC - No internal connection

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logic symbols[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

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**'290, 'LS290
BCD COUNT SEQUENCE
(See Note A)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**'290, 'LS290
BI-QUINARY (5-2)
(See Note B)**

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**'290, 'LS290
RESET/COUNT FUNCTION TABLE**

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

**'293, 'LS293
COUNT SEQUENCE
(See Note C)**

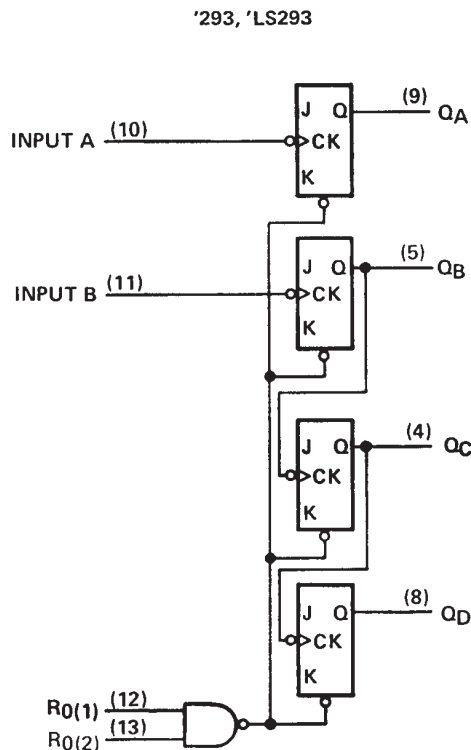
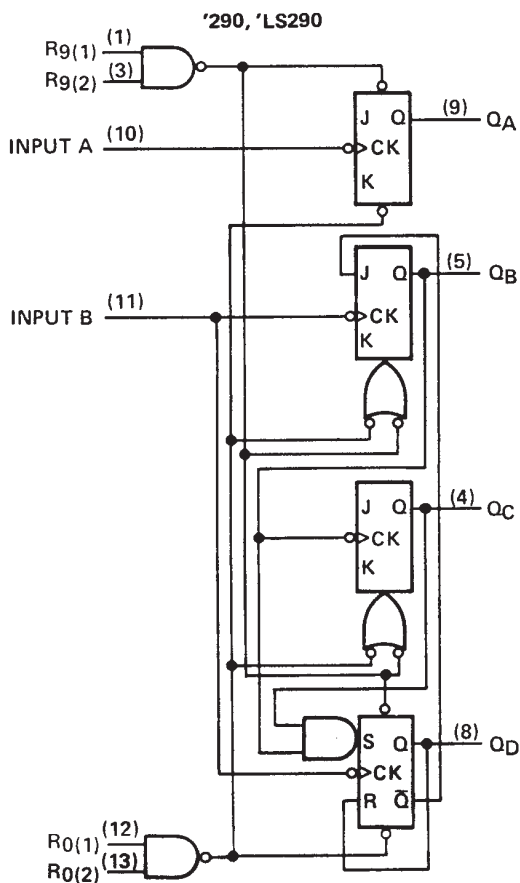
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

**'293, 'LS293
RESET/COUNT FUNCTION TABLE**

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

logic diagrams (positive logic)



Pin numbers shown are for D, J, N, and W packages.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

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The diagram shows a 7414 hex inverters circuit. A pull-up resistor R_{eq} is connected between V_{CC} and the input of the inverters. The input is labeled "INPUT". The output of the inverters is labeled "OUTPUT". The output is connected to a 7400 NAND gate. The output of the NAND gate is labeled "OUTPUT".

INPUT	R_{eq} NOM
A	2.5 $k\Omega$
B ('290)	1.25 $k\Omega$
B ('293)	2.5 $k\Omega$
All resets	6 $k\Omega$



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SN74290, SN74293, SN74LS290, SN74LS293
DECADE AND 4-BIT BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'290			'293			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		2.4	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA¶		0.2	0.4		0.2	0.4	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	High-level input current	Any reset			40			40	µA
		A input			80			80	
		B input			120			80	
I _{IL}	Low-level input current	Any reset			-1.6			-1.6	mA
		A input			-3.2			-3.2	
		B input			-4.8			-3.2	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	SN54'	-20	-57	-20	-57		mA
			SN74'	-18	-57	-18	-57		
I _{CC}	Supply current	V _{CC} = MAX, See Note 3		29	42		26	39	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

¶ Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'290			'293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 400 Ω, See Note 4	32	42		32	42		MHz
	B	Q _B		16			16			
t _{PLH}	A	Q _A			10	16		10	16	ns
t _{PHL}					12	18		12	18	
t _{PLH}	A	Q _D			32	48		46	70	ns
t _{PHL}					34	50		46	70	
t _{PLH}	B	Q _B			10	16		10	16	ns
t _{PHL}					14	21		14	21	
t _{PLH}	B	Q _C			21	32		21	32	ns
t _{PHL}					23	35		23	35	
t _{PLH}	B	Q _D			21	32		34	51	ns
t _{PHL}					23	35		34	51	
t _{PHL}	Set-to-0	Any			26	40		26	40	ns
t _{PLH}	Set-to-9	Q _A , Q _D			20	30				ns
t _{PHL}		Q _B , Q _C			26	40				

f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

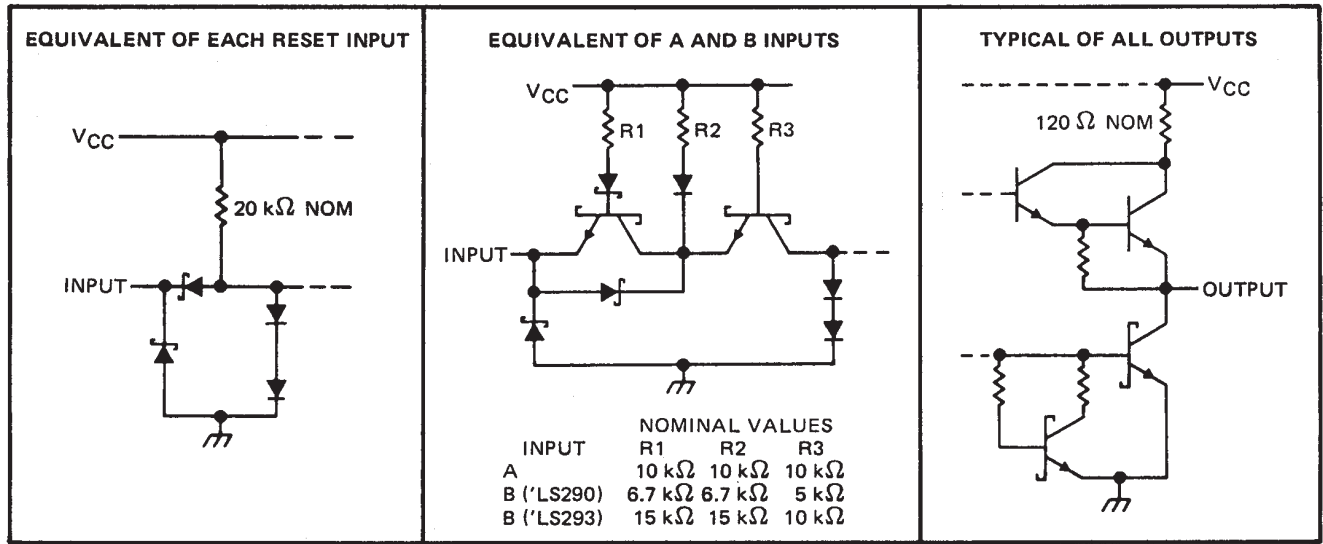


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SN54290, SN54293, SN54LS290, SN54LS293
SN74290, SN74293, SN74LS290, SN74LS293
DECADE AND 4-BIT BINARY COUNTERS

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 5)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS290, SN54LS293	-55°C to 125°C
SN74LS290, SN74LS293	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 5: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		-400			-400			μA
Low-level output current, I_{OL}		4			8			mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	30			30			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}\text{C}$

SN54290, SN54293, SN54LS290, SN54LS293
SN74290, SN74293, SN74LS290, SN74LS293
DECADE AND 4-BIT BINARY COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS*		SN74LS*		UNIT
					MIN	TYP‡	MAX	MIN	
V _{IH}	High-level input voltage				2		2		V
V _{IL}	Low-level input voltage					0.7		0.8	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5	V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 µA		2.5	3.4	2.7	3.4	V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max		I _{OL} = 4 mA¶		0.25 0.4		V
					I _{OL} = 8 mA¶		0.35 0.5		
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V				0.1 0.1		mA
		A input					0.2 0.2		
		B of 'LS290	V _{CC} = MAX, V _I = 5.5 V				0.4 0.4		
		B of 'LS293					0.2 0.2		
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V				20 20		µA
		A input					40 40		
		B of 'LS290					80 80		
		B of 'LS293					40 40		
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V				-0.4 -0.4		mA
		A input					-2.4 -2.4		
		B of 'LS290					-3.2 -3.2		
		B of 'LS293					-1.6 -1.6		
I _{OS}	Short-circuit output current§		V _{CC} = MAX		-20	-100	-20	-100	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 3		'LS290		9 15		mA
					'LS293		9 15		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS290			'LS293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 2 kΩ, See Note 4	32	42		32	42		MHz
	B	Q _B		16			16			
t _{PLH}	A	Q _A		10	16		10	16		ns
t _{PHL}	A	Q _A		12	18		12	18		
t _{PLH}	A	Q _D		32	48		46	70		ns
t _{PHL}	A	Q _D		34	50		46	70		
t _{PLH}	B	Q _B		10	16		10	16		ns
t _{PHL}	B	Q _B		14	21		14	21		
t _{PLH}	B	Q _C		21	32		21	32		ns
t _{PHL}	B	Q _C		23	35		23	35		
t _{PLH}	B	Q _D		21	32		34	51		ns
t _{PHL}	B	Q _D		23	35		34	51		
t _{PHL}	Set-to-0	Any		26	40		26	40		ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30					ns
t _{PHL}	Set-to-9	Q _B , Q _C		26	40					

#f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



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