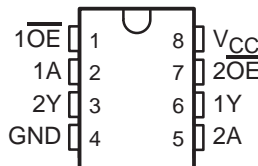


# SN74LVC2G240 DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

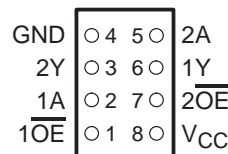
SCES208F – APRIL 1999 – REVISED SEPTEMBER 2003

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.6 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

DCT OR DCU PACKAGE  
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE  
(BOTTOM VIEW)



## description/ordering information

This dual buffer/driver is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G240 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
$-40^\circ\text{C}$ to $85^\circ\text{C}$	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Tape and reel	SN74LVC2G240YEAR	_ _ _ CK _
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74LVC2G240YZAR	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC2G240YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC2G240YZPR	
	SSOP – DCT	Tape and reel	SN74LVC2G240DCTR	C40_ _ _
	VSSOP – DCU	Tape and reel	SN74LVC2G240DCUR	C40_ _

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# SN74LVC2G240

## DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

This device is organized as two 1-bit buffers/drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A input to the Y output. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

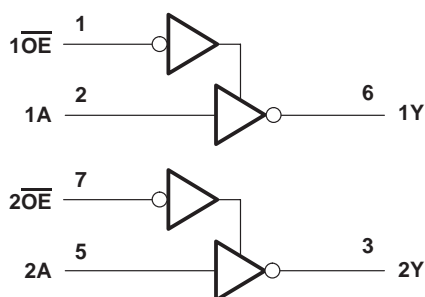
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

### logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	227°C/W
YEA/YZA package	140°C/W
YEP/YZP package	102°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74LVC2G240

## DUAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$ Supply voltage	Operating	1.65	5.5	V
	Data retention only	1.5		
$V_{IH}$ High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
	$V_{CC} = 3\text{ V to }3.6\text{ V}$	2		
	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$		
$V_{IL}$ Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
	$V_{CC} = 3\text{ V to }3.6\text{ V}$	0.8		
	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.3 \times V_{CC}$		
$V_I$ Input voltage		0	5.5	V
$V_O$ Output voltage	High or low state	0	$V_{CC}$	V
	3-state	0	5.5	
$I_{OH}$ High-level output current	$V_{CC} = 1.65\text{ V}$		-4	mA
	$V_{CC} = 2.3\text{ V}$		-8	
	$V_{CC} = 3\text{ V}$		-16	
	$V_{CC} = 4.5\text{ V}$		-24	
$I_{OL}$ Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
	$V_{CC} = 2.3\text{ V}$		8	
	$V_{CC} = 3\text{ V}$		16	
	$V_{CC} = 4.5\text{ V}$		24	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$		20	ns/V
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		10	
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		5	
$T_A$ Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74LVC2G240**  
**DUAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = –100 µA	1.65 V to 5.5 V	V <sub>CC</sub> –0.1			V
		I <sub>OH</sub> = –4 mA	1.65 V	1.2			
		I <sub>OH</sub> = –8 mA	2.3 V	1.9			
		I <sub>OH</sub> = –16 mA	3 V	2.4			
		I <sub>OH</sub> = –24 mA		2.3			
		I <sub>OH</sub> = –32 mA	4.5 V	3.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	1.65 V to 5.5 V	0.1			V
		I <sub>OL</sub> = 4 mA	1.65 V	0.45			
		I <sub>OL</sub> = 8 mA	2.3 V	0.3			
		I <sub>OL</sub> = 16 mA	3 V	0.4			
		I <sub>OL</sub> = 24 mA		0.55			
		I <sub>OL</sub> = 32 mA	4.5 V	0.55			
I <sub>I</sub>	A or $\overline{\text{OE}}$ inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	µA
I <sub>OZ</sub>		V <sub>O</sub> = 0 to 5.5 V	3.6 V			10	µA
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10	µA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			4	pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			6	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2	11.3	1.4	5.5	1.1	4.6	1	4	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	2.7	11.7	1.9	6.6	1.4	5.4	1.1	5	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	1.7	12.8	0.8	5.7	1.2	5.5	0.5	4.2	ns

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
				TYP	TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz			15	17	pF
		Outputs disabled		1	1	2	3	



# SN74LVC2G240

## DUAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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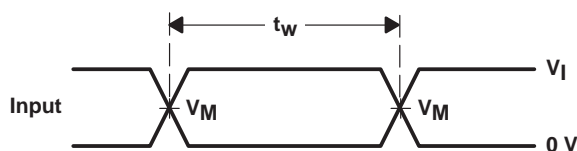
#### PARAMETER MEASUREMENT INFORMATION



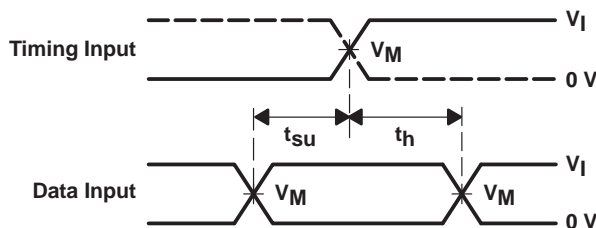
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	$GND$

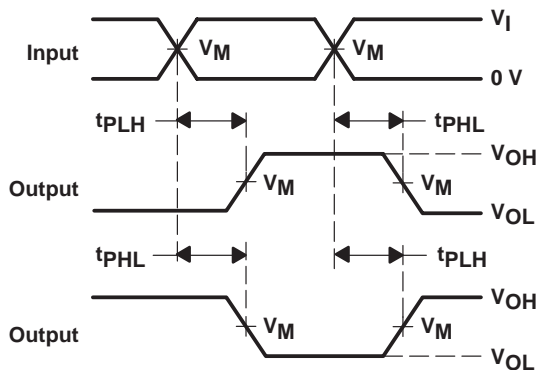
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8 V \pm 0.15 V$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3 V \pm 0.3 V$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5 V \pm 0.5 V$	$V_{CC}$	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



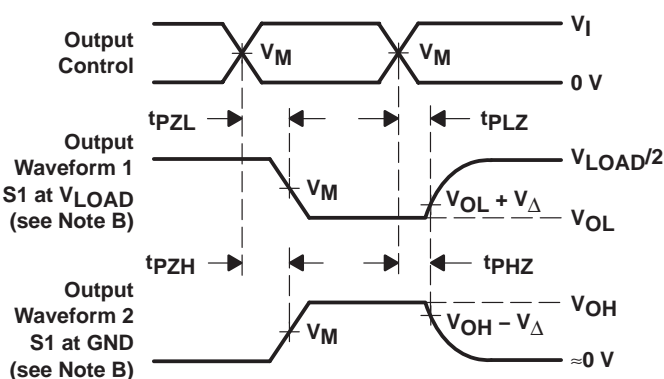
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

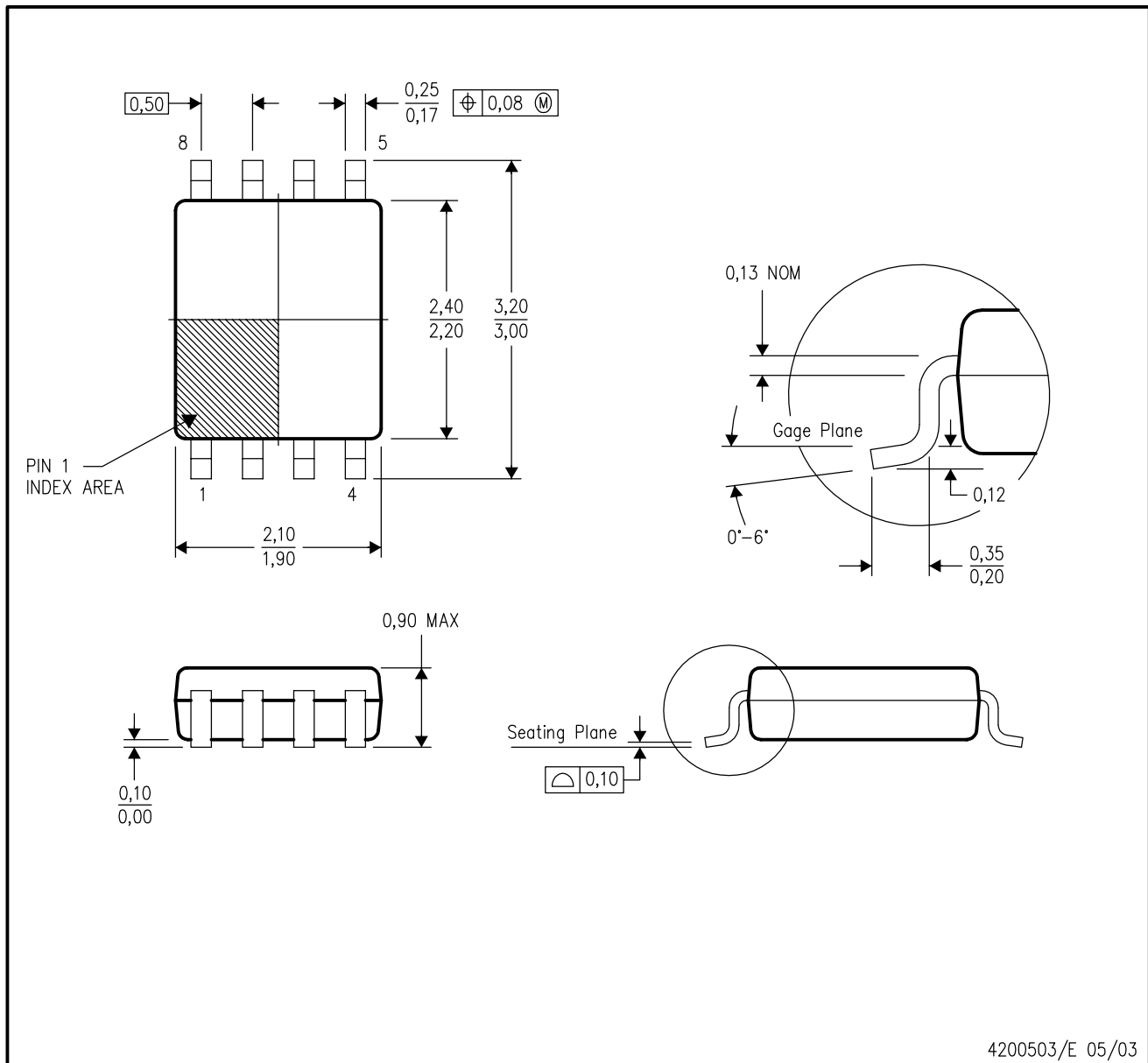
## DCT (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



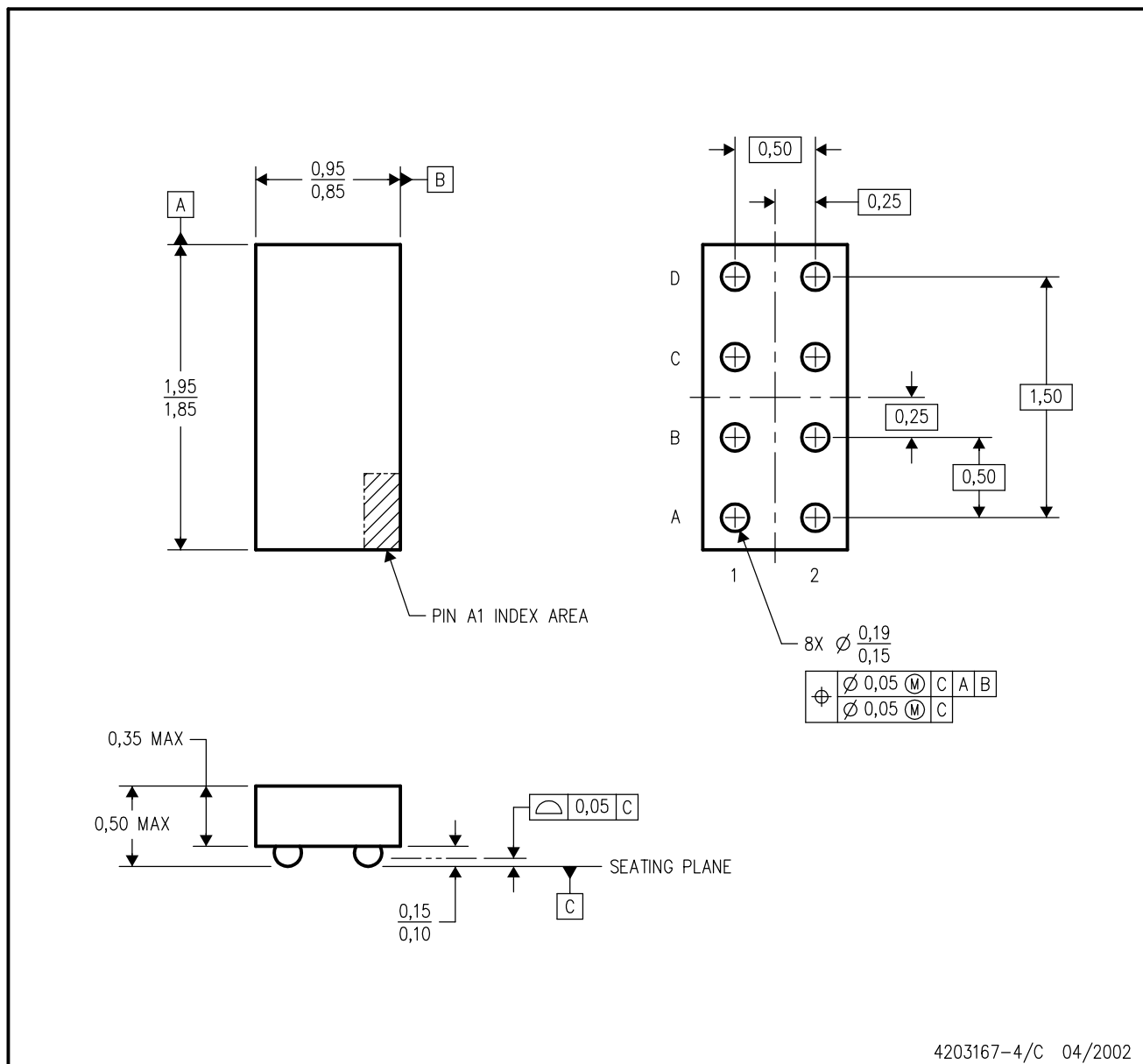
4200503/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation CA.



## YEA (R-XBGA-N8)

## DIE-SIZE BALL GRID ARRAY

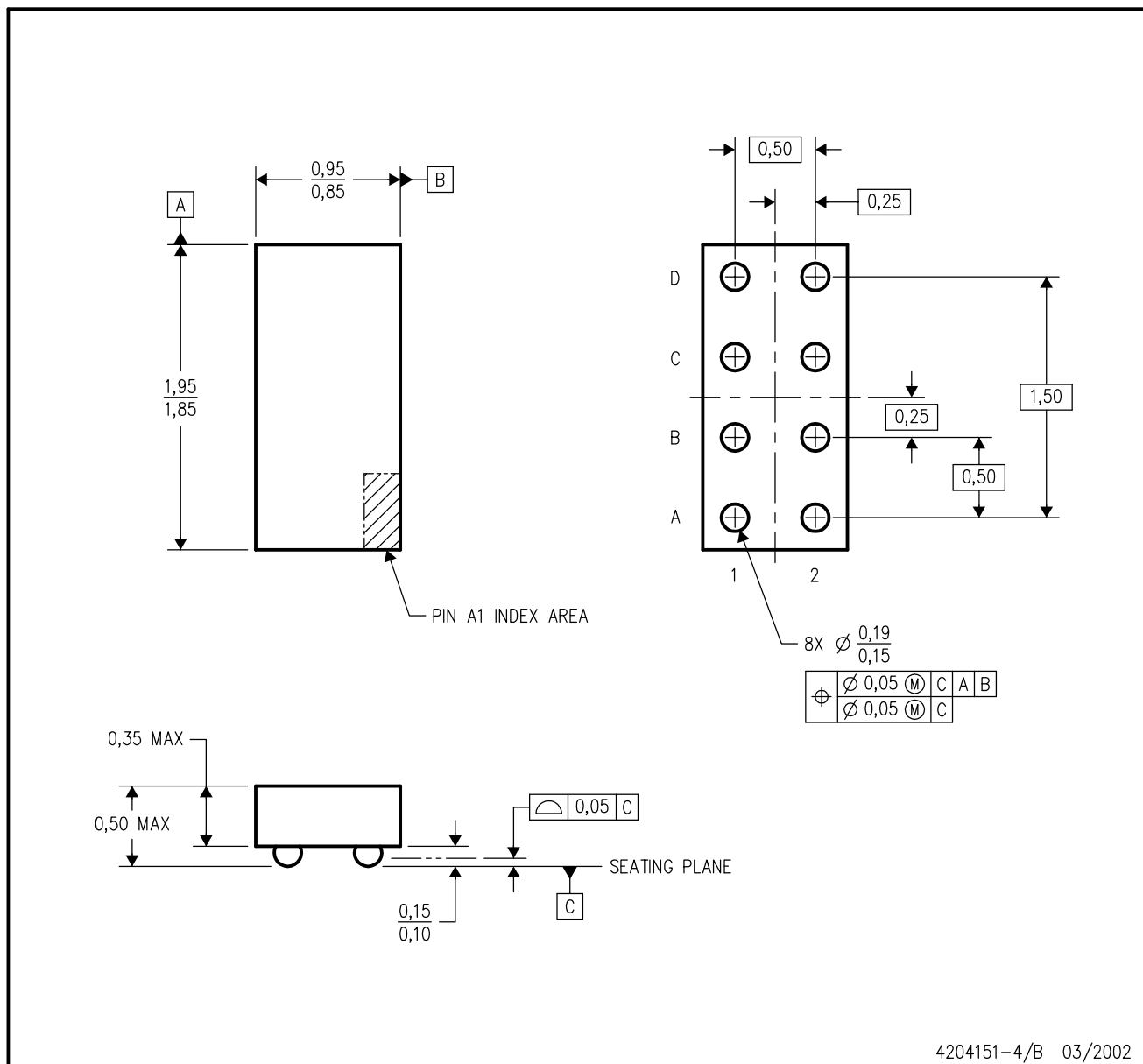


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. Package complies to JEDEC MO-211 variation EB.
  - E. This package is tin-lead (SnPb). Refer to the 8 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

## YZA (R-XBGA-N8)

## DIE-SIZE BALL GRID ARRAY

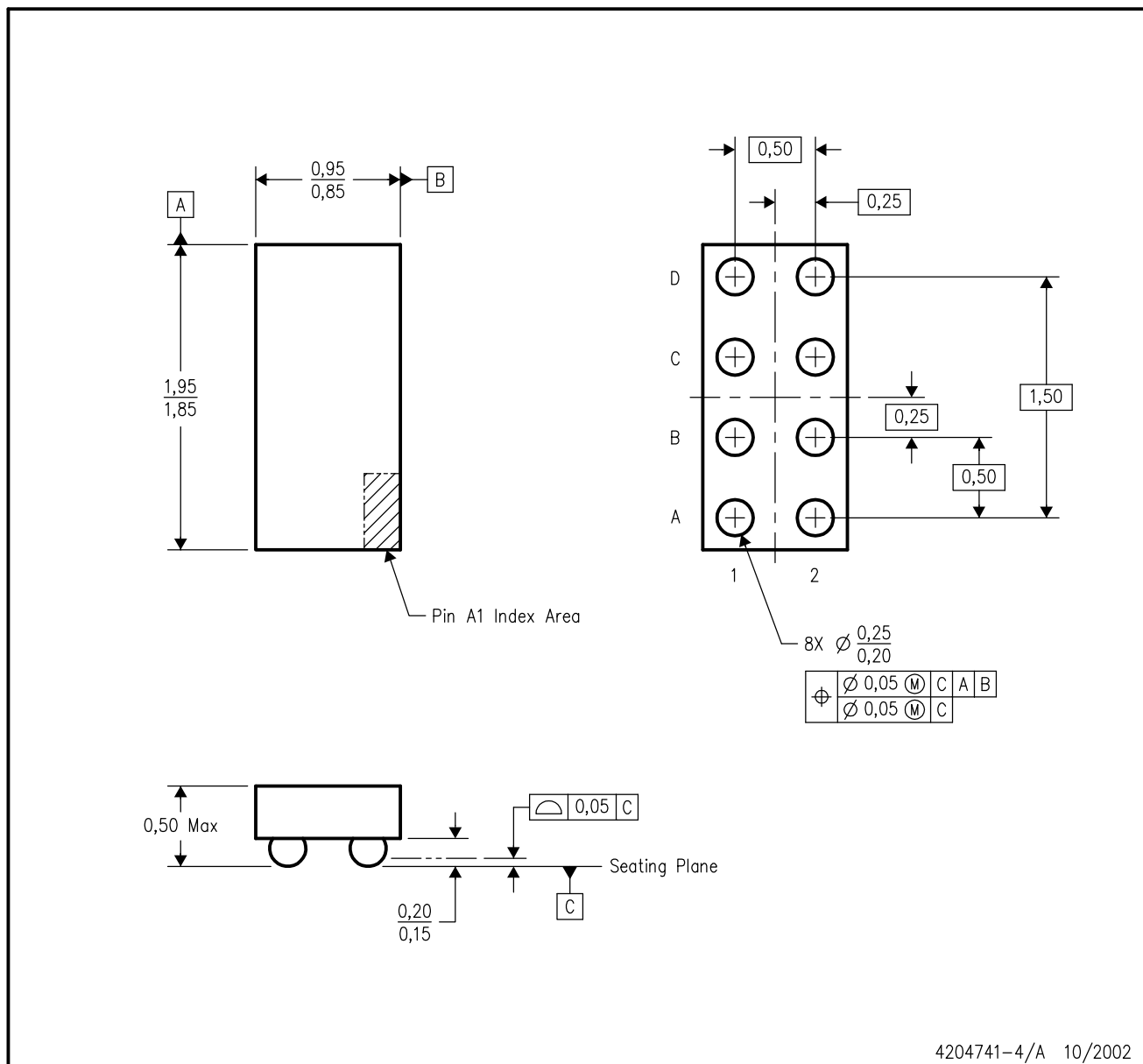


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. Package complies to JEDEC MO-211 variation EB.
  - E. This package is lead-free. Refer to the 8 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

## YZP (R-XBGA-N8)

## DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

YEP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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