

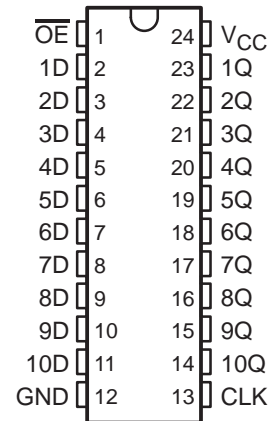
# SN74LVC821A

## 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS304F – MARCH 1993 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE  
(TOP VIEW)



### description

This 10-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC821A features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC821A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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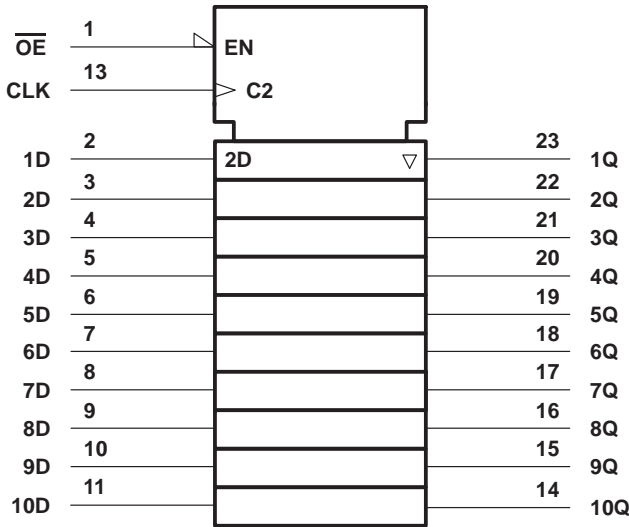
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FUNCTION TABLE  
(each flip-flop)

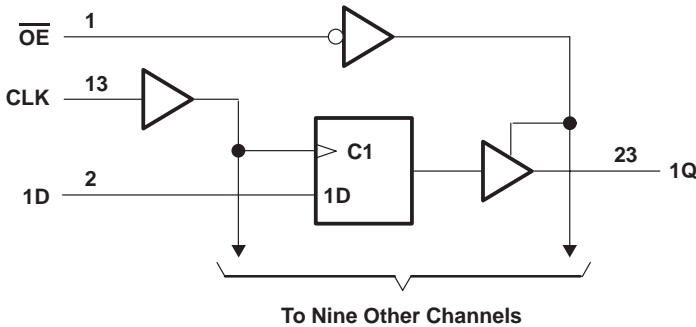
INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$ Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
$V_{IH}$ High-level input voltage	$V_{CC} = 1.65$ V to $1.95$ V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to $2.7$ V	1.7		
	$V_{CC} = 2.7$ V to $3.6$ V	2		
$V_{IL}$ Low-level input voltage	$V_{CC} = 1.65$ V to $1.95$ V		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3$ V to $2.7$ V		0.7	
	$V_{CC} = 2.7$ V to $3.6$ V		0.8	
$V_I$ Input voltage		0	5.5	V
$V_O$ Output voltage	High or low state	0	$V_{CC}$	V
	3 state	0	5.5	
$I_{OH}$ High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 2.7$ V		–12	
	$V_{CC} = 3$ V		–24	
$I_{OL}$ Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 2.7$ V		12	
	$V_{CC} = 3$ V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
$T_A$ Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = –100 µA	1.65 V to 3.6 V	V <sub>CC</sub> –0.2			V
	I <sub>OH</sub> = –4 mA	1.65 V	1.2			
	I <sub>OH</sub> = –8 mA	2.3 V	1.7			
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I <sub>OH</sub> = –24 mA	3 V	2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 8 mA	2.3 V			0.7	
	I <sub>OL</sub> = 12 mA	2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	µA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	µA
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V			±10	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			10	µA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V‡				10	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	µA
C <sub>i</sub>	Control inputs	3.3 V			5	pF
	Data inputs				4	
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			7	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This applies in the disabled state only.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	§		§		150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	§		§		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK	§		§		1.9		1.9		ns
t <sub>h</sub>	Hold time, data after CLK	§		§		1.5		1.5		ns

§ This information was not available at the time of publication.



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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			†		†		150		150		MHz
t <sub>pd</sub>	CLK	Q	†	†	†	†	8.5		2.2	7.3	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Q	†	†	†	†	8.8		1.3	7.6	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Q	†	†	†	†	6.8		1.6	6.2	ns
t <sub>sk(o)</sub> †									1		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz	†	†	65	pF
		Outputs disabled		†	†	48	

† This information was not available at the time of publication.

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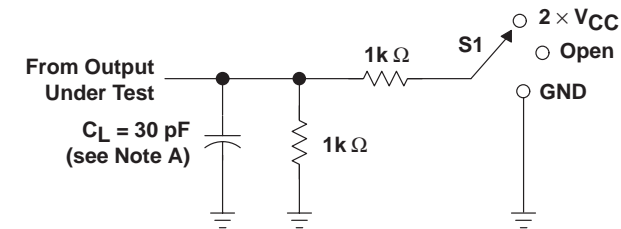
## 10-BIT BUS-INTERFACE FLIP-FLOP

### WITH 3-STATE OUTPUTS

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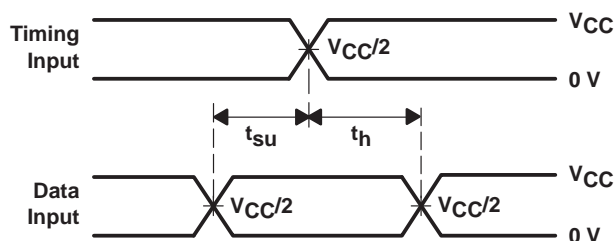
#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

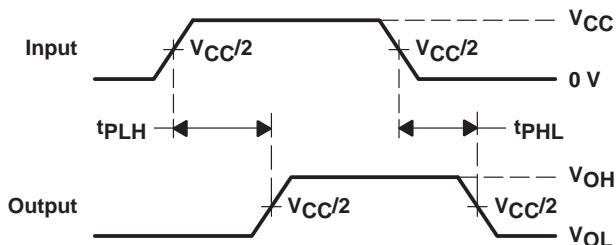


LOAD CIRCUIT

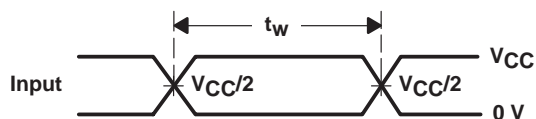
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PHZ}$	Open



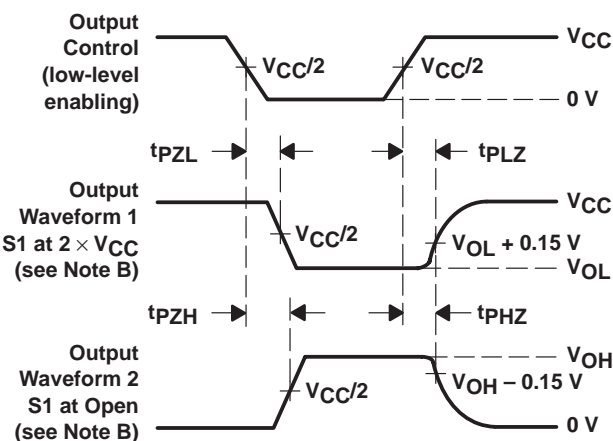
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



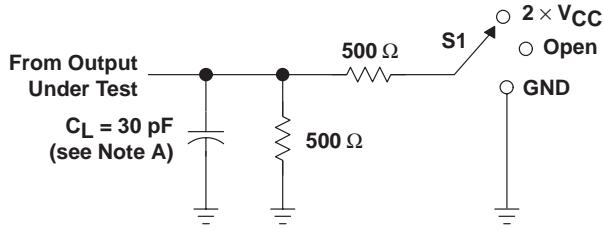
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

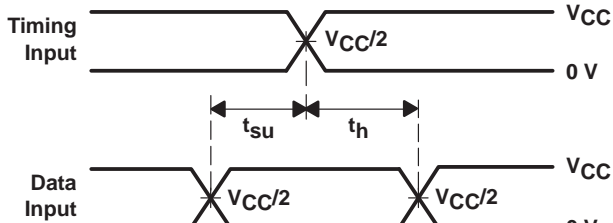
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

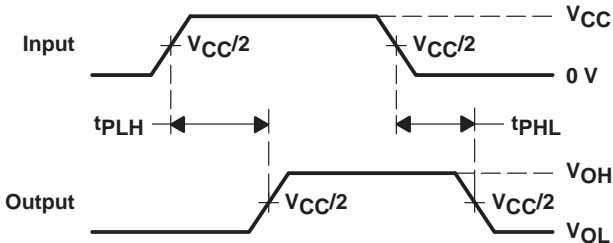


**LOAD CIRCUIT**

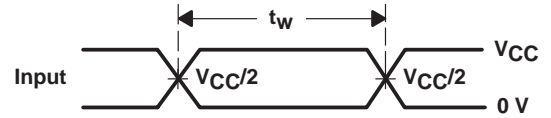
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



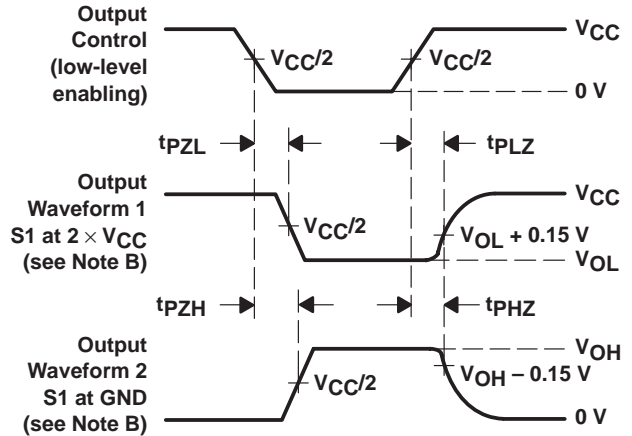
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
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 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

# SN74LVC821A

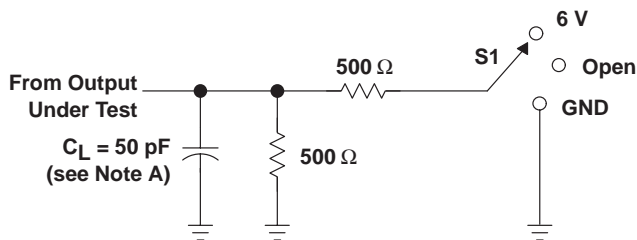
## 10-BIT BUS-INTERFACE FLIP-FLOP

### WITH 3-STATE OUTPUTS

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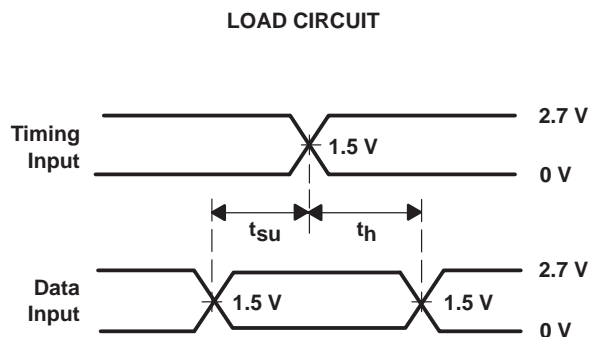
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

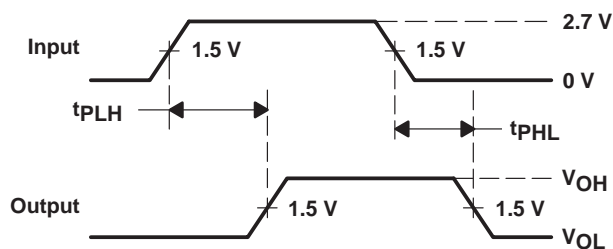


LOAD CIRCUIT

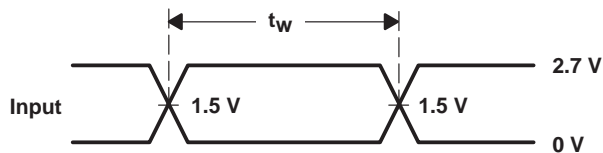
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



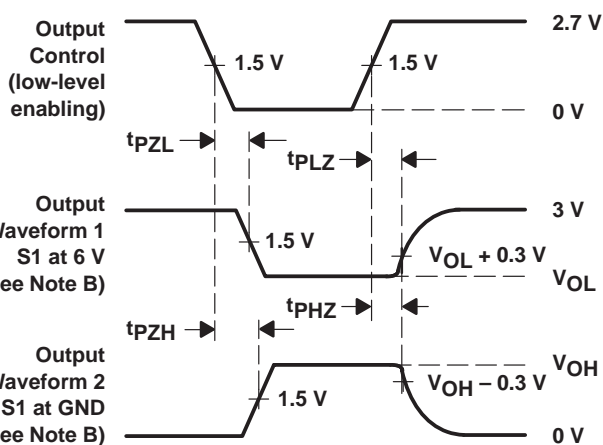
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



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PULSE DURATION



VOLTAGE WAVEFORMS  
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  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms



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