

SN74LVCH16901

18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

SCES145A – OCTOBER 1998 – REVISED MAY 1999

- Member of the Texas Instruments **Widebus+™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **UBT™** (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Simultaneously Generates and Checks Parity
- Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or B-to-A Directions
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down-Mode Operation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class I
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Thin Shrink Small-Outline Package

DGG PACKAGE
(TOP VIEW)

1CLKENAB	1	64	1CLKENBA
LEAB	2	63	LEBA
CLKAB	3	62	CLKBA
1ERRA	4	61	1ERRB
1APAR	5	60	1BPAR
GND	6	59	GND
1A1	7	58	1B1
1A2	8	57	1B2
1A3	9	56	1B3
V _{CC}	10	55	V _{CC}
1A4	11	54	1B4
1A5	12	53	1B5
1A6	13	52	1B6
GND	14	51	GND
1A7	15	50	1B7
1A8	16	49	1B8
2A1	17	48	2B1
2A2	18	47	2B2
GND	19	46	GND
2A3	20	45	2B3
2A4	21	44	2B4
2A5	22	43	2B5
V _{CC}	23	42	V _{CC}
2A6	24	41	2B6
2A7	25	40	2B7
2A8	26	39	2B8
GND	27	38	GND
2APAR	28	37	2BPAR
2ERRA	29	36	2ERRB
OEAB	30	35	OEBA
SEL	31	34	ODD/EVEN
2CLKENAB	32	33	2CLKENBA

description

This 18-bit (dual-octal) noninverting registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver, or it can generate/check parity from the two 8-bit data buses in either direction.

The SN74LVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) inputs. It also provides parity-enable ($\overline{\text{SEL}}$) and parity-select (ODD/EVEN) inputs and separate error-signal ($\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$) outputs for checking parity. The direction of data flow is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$) inputs. When $\overline{\text{SEL}}$ is low, the parity functions are enabled. When $\overline{\text{SEL}}$ is high, the parity functions are disabled, and the device acts as an 18-bit registered transceiver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+, EPIC, and UBT are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

SN74LVCH16901

18-BIT UNIVERSAL BUS TRANSCEIVER

WITH PARITY GENERATORS/CHECKERS

SCES145A – OCTOBER 1998 – REVISED MAY 1999

description (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74LVCH16901 is characterized for operation from -40°C to 85°C .

Function Tables

FUNCTION†					
INPUTS					OUTPUT B
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0^{\ddagger}
L	L	L	\uparrow	L	L
L	L	L	\uparrow	H	H
L	L	L	L	X	B_0^{\ddagger}
L	L	L	H	X	B_0^{\S}

† A-to-B data flow is shown; B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY ENABLE

INPUTS			OPERATION OR FUNCTION
$\overline{\text{SEL}}$	$\overline{\text{OEBA}}$	$\overline{\text{OEAB}}$	
L	H	L	Parity is checked on port A and is generated on port B.
L	L	H	Parity is checked on port B and is generated on port A.
L	H	H	Parity is checked on port B and port A.
L	L	L	Parity is generated on port A and B if device is in FF mode.
H	L	L	Parity functions are disabled; device acts as a standard 18-bit registered transceiver.
H	L	H	
H	H	L	
H	H	H	

Q_A data to B, Q_B data to A
 Q_B data to A
 Q_A data to B
 Isolation

Function Tables (Continued)

PARITY											
INPUTS								OUTPUTS			
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1–A8 = H	Σ OF INPUTS B1–B8 = H	APAR	BPAR	APAR	ERRA	BPAR	ERRB
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	H	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE†	Z	PE†	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO‡	Z	PO‡	Z

† Parity output is set to the level so that the specific bus side is set to even parity.

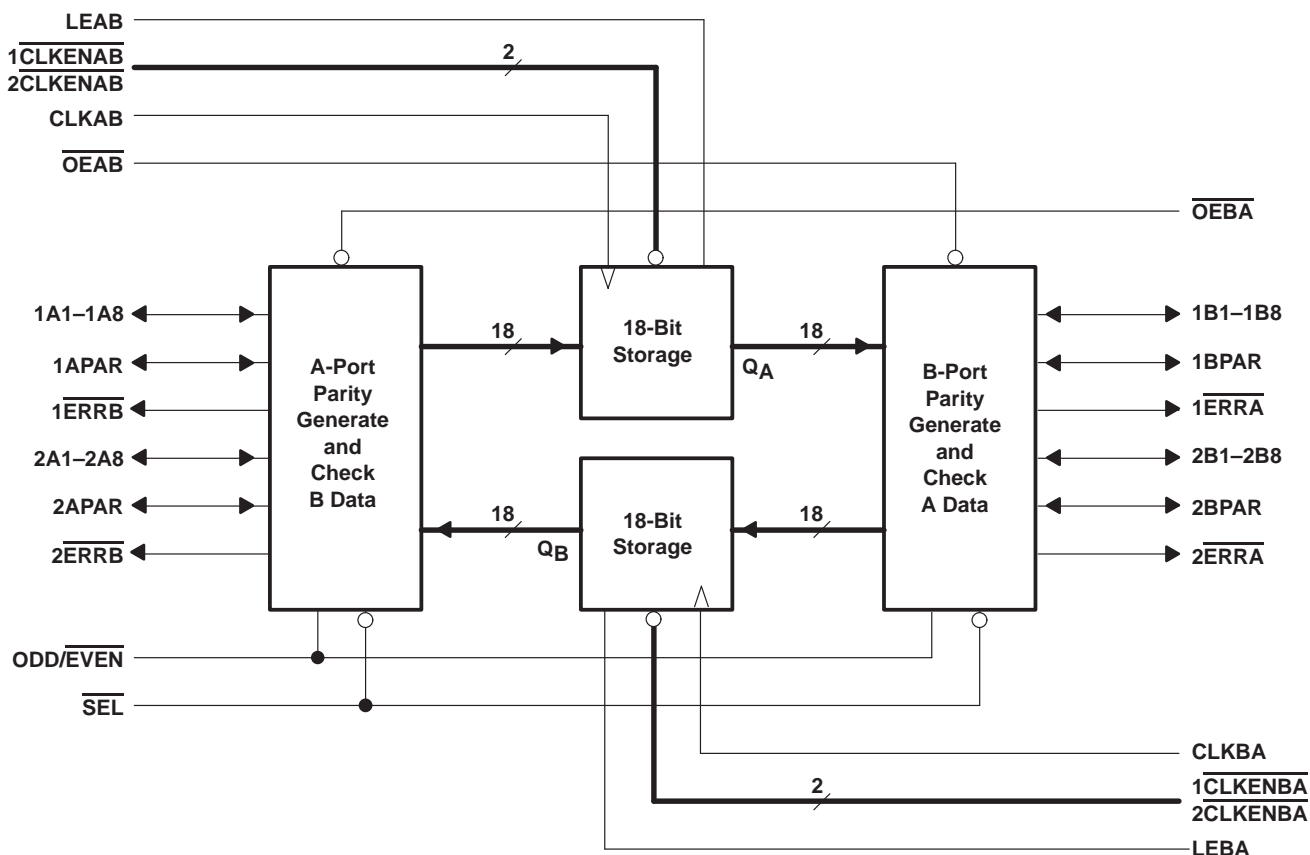
‡ Parity output is set to the level so that the specific bus side is set to odd parity.

SN74LVCH16901

18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

SCES145A – OCTOBER 1998 – REVISED MAY 1999

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	73°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3 state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V	−4		mA
		V _{CC} = 2.3 V	−8		
		V _{CC} = 2.7 V	−12		
		V _{CC} = 3 V	−24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate		5	ns/V	
T _A	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVCH16901
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH PARITY GENERATORS/CHECKERS

SCES145A – OCTOBER 1998 – REVISED MAY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} –0.2			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.7			
		I _{OH} = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I _{OH} = –24 mA	3 V	2.2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.7	
		I _{OL} = 12 mA	2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V			±5	µA
I _{I(hold)}	A or B ports	V _I = 0.58 V	1.65 V	25			µA
		V _I = 1.07 V		–25			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V		–45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V		–75			
		V _I = 0 to 3.6 V‡	3.6 V			±600	
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{OZ} §		V _O = 0 to 5.5 V	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND	3.6 V			20	µA
		3.6 V ≤ V _I ≤ 5.5 V¶				20	
I _O = 0							
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		7		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V		9.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current, but not I_{I(hold)}.

¶ This applies in the disabled state only.



SN74LVCH16901
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH PARITY GENERATORS/CHECKERS

SCES145A – OCTOBER 1998 – REVISED MAY 1999

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} = 1.8 V†		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		125		125		125		125		MHz
t _w	Pulse duration	CLK↑	4		3		3		3		ns
		LE high	3		3		3		3		
t _{su}	Setup time	A, APAR or B, BPAR before CLK↑	4.7		2.7		2.8		2.5		ns
		CLKEN before CLK↑	4.5		2.9		2.9		2.5		
		A, APAR or B, BPAR before LE↓	0		2.2		2.1		2		
t _h	Hold time	A, APAR or B, BPAR after CLK↑	0		1.2		1.2		1.3		ns
		CLKEN after CLK↑	0		1.3		1.3		1.5		
		A, APAR or B, BPAR after LE↓	1		1.7		1.9		1.7		

† Texas Instruments SPICE simulation data

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}^\dagger$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	125		125		125		MHz
t_{pd}	A or B	B or A	5.9	1	6.2		5.8	1	5.4	ns
		BPAR or APAR	12.7	2	9.9		8.6	2	7.7	
	APAR or BPAR	BPAR or APAR	7	1	6.7		6.2	1	5.7	
		ERRA or ERRB	13	2	10.7		9.7	2	8.5	
	ODD/EVEN	ERRA or ERRB	9.9	1.5	9.7		8.9	1.5	7.8	
		BPAR or APAR	10.4	1.5	9.3		8.6	1.5	7.5	
	SEL	BPAR or APAR	6.9	1	7.1		6.9	1	6.1	
	CLKAB or CLKBA	A or B	6.9	1	7.4		6.8	1	6.1	
		BPAR or APAR parity feedthrough	8.5	1.5	8.1		7.3	1.5	6.6	
		BPAR or APAR parity generated	14.1	2.5	11.2		9.7	2	8.7	
		ERRA or ERRB	14.3	2.5	11.5		9.9	2	8.9	
	LEAB or LEBA	A or B	6.8	1	7		6.5	1	5.8	
		BPAR or APAR parity feedthrough	7.9	1.5	7.7		7	1.5	6.3	
		BPAR or APAR parity generated	13.6	2.5	10.8		9.3	2	8.4	
		ERRA or ERRB	13.5	2.5	10.9		9.5	2	8.5	
t_{en}	OEAB or OEBA	B, BPAR or A, APAR	6.8	1.4	7.3		7.1	1	6.3	ns
t_{dis}	OEAB or OEBA	B, BPAR or A, APAR	6.9	1.3	7.1		6.2	1.5	5.9	ns
t_{en}	OEAB or OEBA	ERRA or ERRB	7.4	1.4	7.2		6.5	1	5.9	ns
t_{dis}	OEAB or OEBA	ERRA or ERRB	9.3	1.3	8.3		7.5	1	6.7	ns
t_{en}	SEL	ERRA or ERRB	7.6	1.4	7.7		7.5	1	6.5	ns
t_{dis}	SEL	ERRA or ERRB	7.8	1.3	7.4		6.4	1.5	5.9	ns

† Texas Instruments SPICE simulation data



SN74LVCH16901

18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

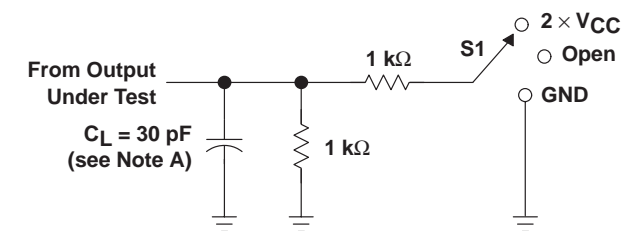
SCES145A – OCTOBER 1998 – REVISED MAY 1999

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	37	52	68	pF
	Outputs disabled		16	22	28	

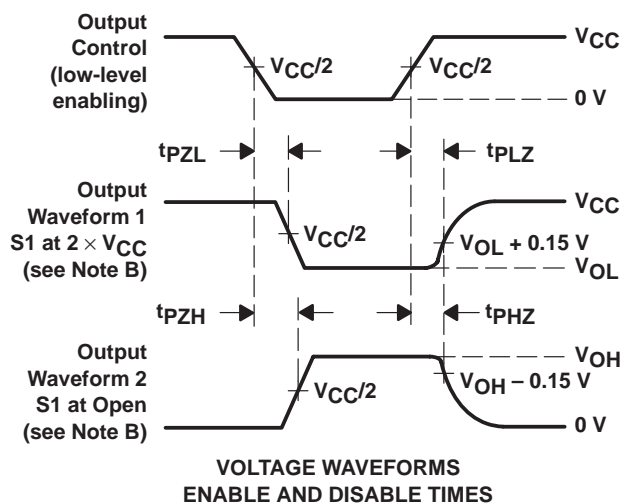
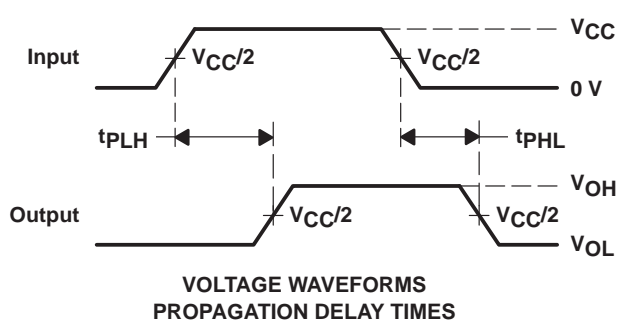
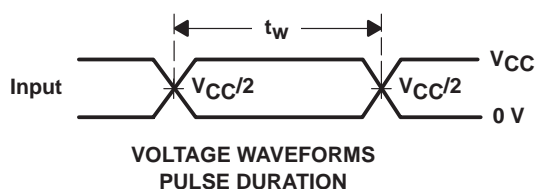
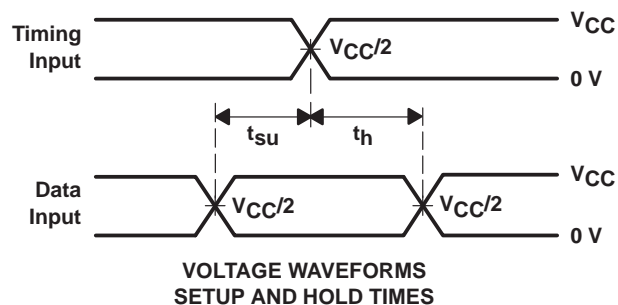
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



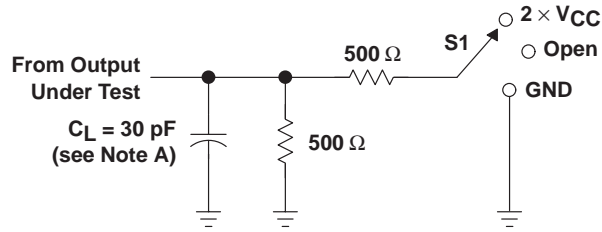
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



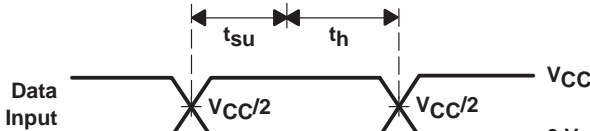
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

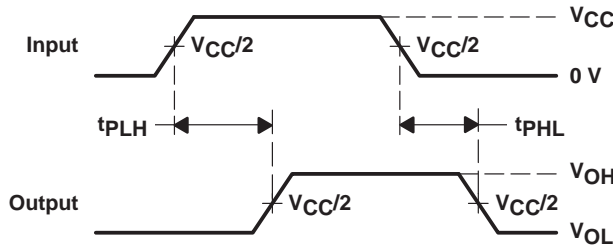


LOAD CIRCUIT

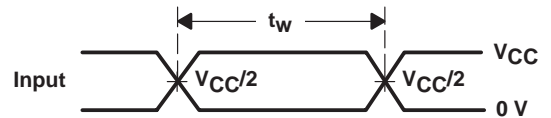
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



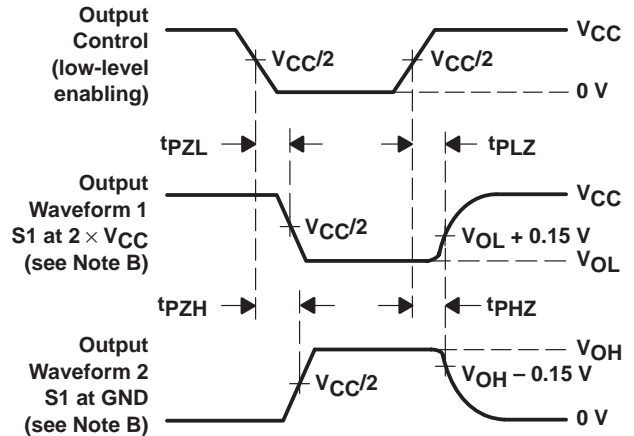
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

SN74LVCH16901

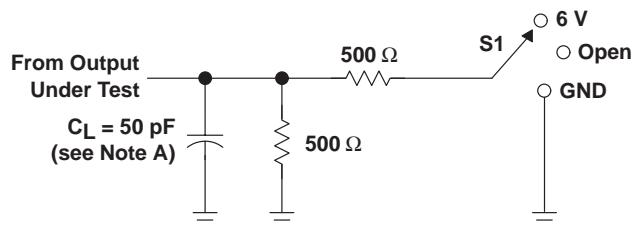
18-BIT UNIVERSAL BUS TRANSCEIVER

WITH PARITY GENERATORS/CHECKERS

SCES145A – OCTOBER 1998 – REVISED MAY 1999

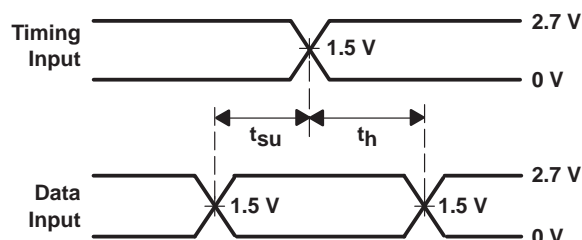
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

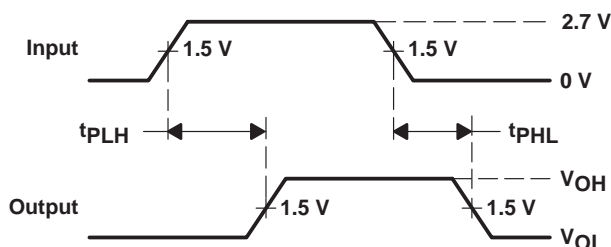


LOAD CIRCUIT

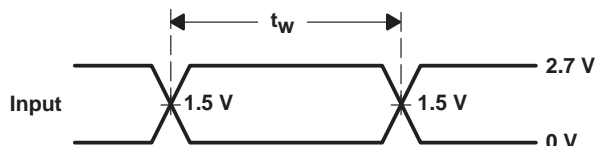
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



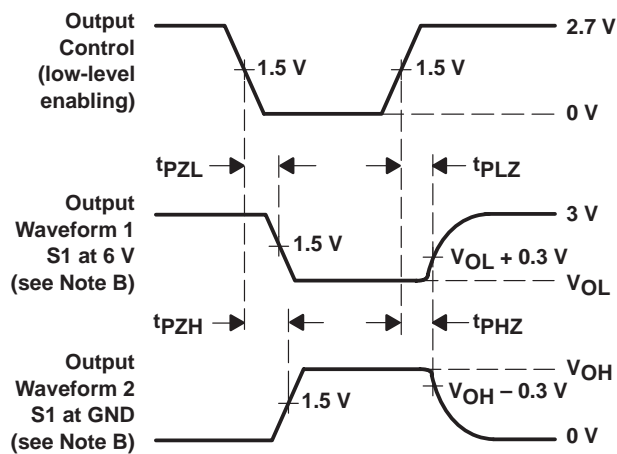
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.