

# SN74LVCZ16240A

## 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES276B – JUNE 1999 – REVISED MARCH 2000

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce)  
<0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
>2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE  
(TOP VIEW)

$\overline{1OE}$	1	48	$2\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
$V_{CC}$	7	42	$V_{CC}$
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
$V_{CC}$	18	31	$V_{CC}$
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
$4\overline{OE}$	24	25	$3\overline{OE}$

### description

This 16-bit buffer/driver is designed for 3-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCZ16240A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN74LVCZ16240A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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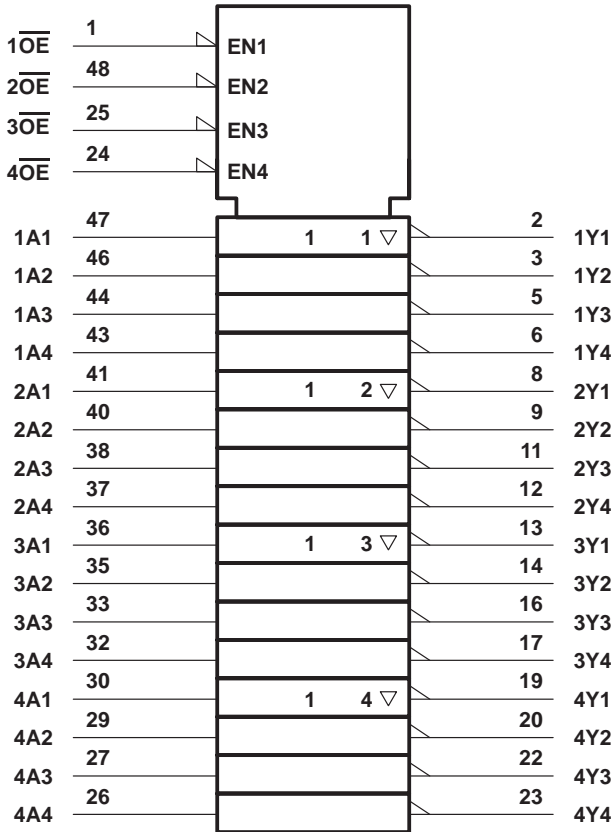
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FUNCTION TABLE  
(each 4-bit buffer)

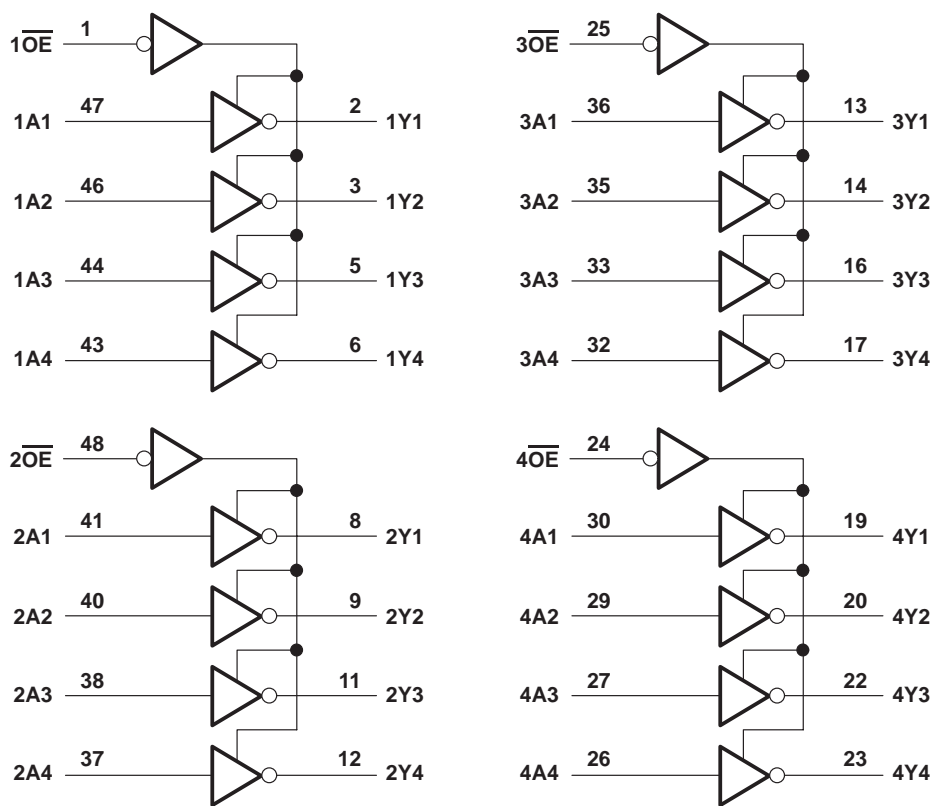
INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package	70°C/W
DL package	63°C/W
Storage temperature range, $T_{Stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

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## 16-BIT BUFFER/DRIVER

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#### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V to } 3.6\text{ V}$		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V to } 3.6\text{ V}$		V
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$
		3-state	0	5.5
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$		–24
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$		24
$\Delta t/\Delta v$	Input transition rise or fall rate	10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	150		$\mu\text{s/V}$
$T_A$	Operating free-air temperature	–40	85	$^{\circ}\text{C}$

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA		3 V to 3.6 V	V <sub>CC</sub> −0.2		V	
	I <sub>OH</sub> = −12 mA		3 V	2.4			
	I <sub>OH</sub> = −24 mA		3 V	2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		3 V to 3.6 V	0.2		V	
	I <sub>OL</sub> = 12 mA		3 V	0.4			
	I <sub>OL</sub> = 24 mA		3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V		3.6 V	±5		μA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0	±5		μA	
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V		3.6 V	±5		μA	
I <sub>OZPU</sub>	V <sub>O</sub> = 0.5 to 2.5 V, $\overline{OE}$ = don't care		0 to 1.5 V	±5		μA	
I <sub>OZPD</sub>	V <sub>O</sub> = 0.5 to 2.5 V, $\overline{OE}$ = don't care		1.5 V to 0	±5		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V	100		μA	
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V‡			100			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		3 V to 3.6 V	100		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V	4.5		pF	
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	6		pF	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

‡ This applies in the disabled state only.

#### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}$	A or B	B or A	1	4.2	ns
$t_{en}$	$\overline{OE}$	A or B	1.5	4.7	ns
$t_{dis}$	$\overline{OE}$	A or B	1.5	5.9	ns



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**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	31	pF
		Outputs disabled	3.5	



# SN74LVCZ16240A

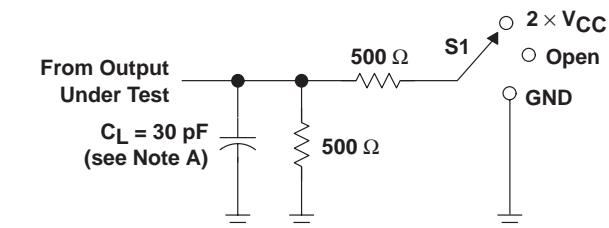
## 16-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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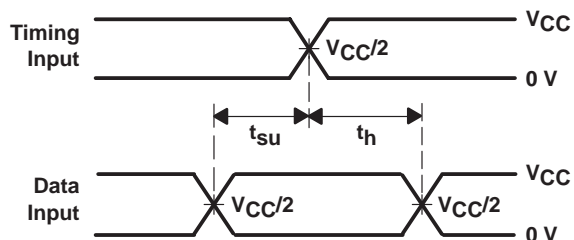
#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

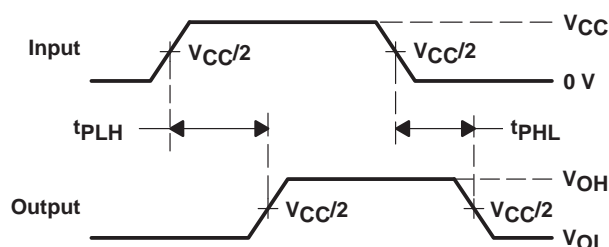


LOAD CIRCUIT

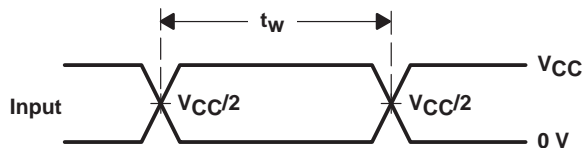
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



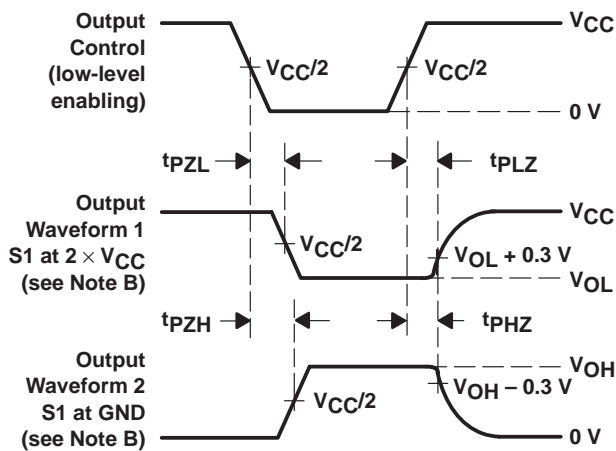
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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