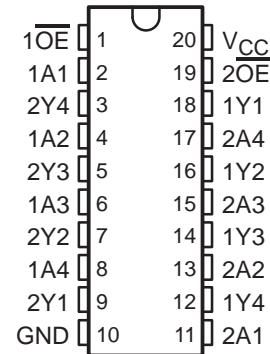


SN74LVCZ240A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES273B – JUNE 1999 – REVISED JANUARY 2000

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Shrink Small-Outline (DB), Plastic Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCZ240A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

This device is organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN74LVCZ240A is characterized for operation from -40°C to 85°C .



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**TEXAS
INSTRUMENTS**

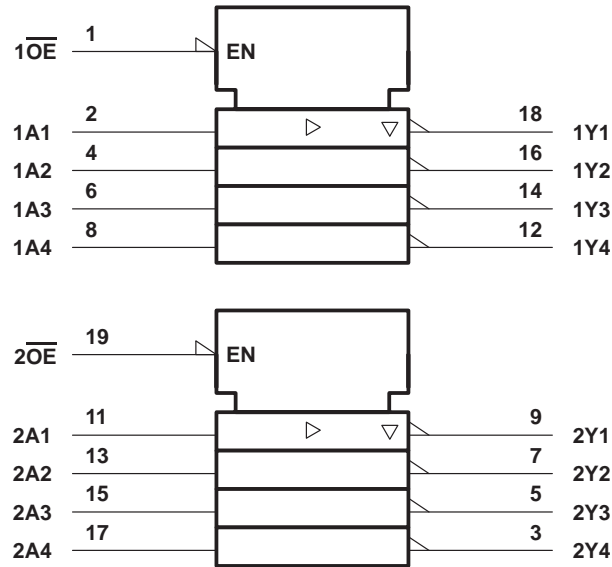
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FUNCTION TABLE
(each buffer)

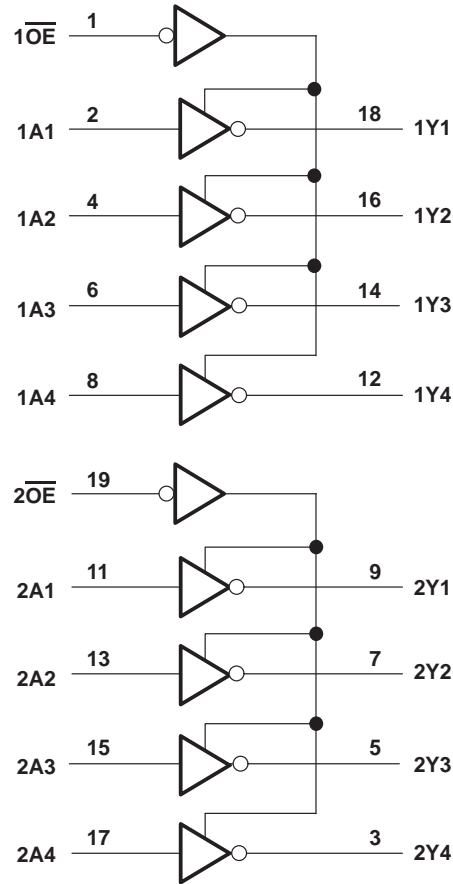
INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SN74LVCZ240A

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	2.7 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 µA	2.7 V to 3.6 V	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 0 to 5.5 V	3.6 V	±5			µA
I _{off}	V _I or V _O = 5.5 V	0	±5			µA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	±5			µA
I _{OZPU}	V _O = 0.5 to 2.5 V, $\overline{\text{OE}}$ = don't care	0 to 1.5 V	±5			µA
I _{OZPD}	V _O = 0.5 to 2.5 V, $\overline{\text{OE}}$ = don't care	1.5 V to 0	±5			µA
I _{CC}	V _I = V _{CC} or GND	3.6 V	100			µA
	3.6 V ≤ V _I ≤ 5.5 V‡		100			
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	100			µA
C _i	V _I = V _{CC} or GND	3.3 V	3.5			pF
C _o	V _O = V _{CC} or GND	3.3 V	5.5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	7.5		1.3	6.5	ns
t _{en}	$\overline{\text{OE}}$	A or B	9		1.1	8	ns
t _{dis}	$\overline{\text{OE}}$	A or B	8		1.4	7	ns

operating characteristics, T_A = 25°C

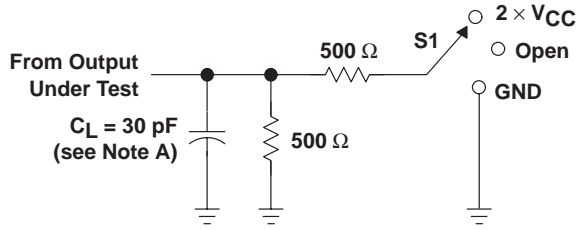
PARAMETER		TEST CONDITIONS	V _{CC} = 3.3 V TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	37	pF
		Outputs disabled	3	



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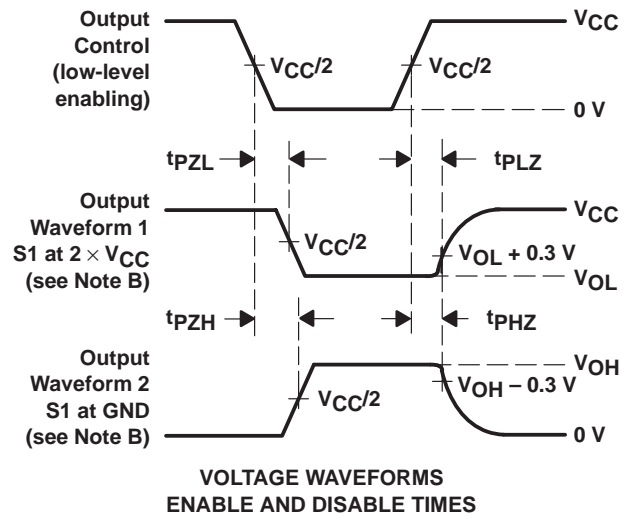
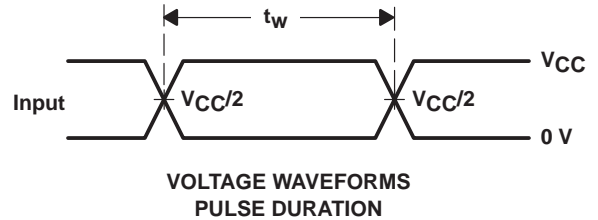
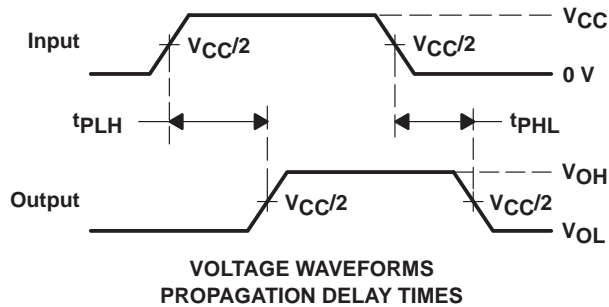
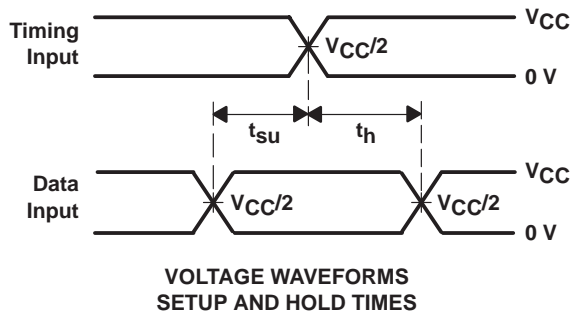
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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