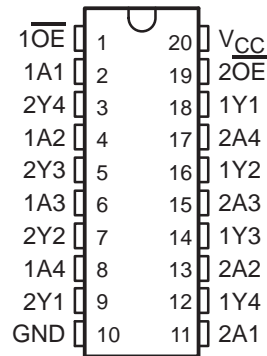


SN54LVT244, SN74LVT244 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

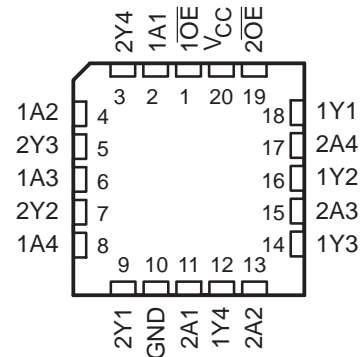
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flatpacks (W), and Ceramic DIPS (J)

SN54LVT244 . . . J OR W PACKAGE
SN74LVT244 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT244 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT244 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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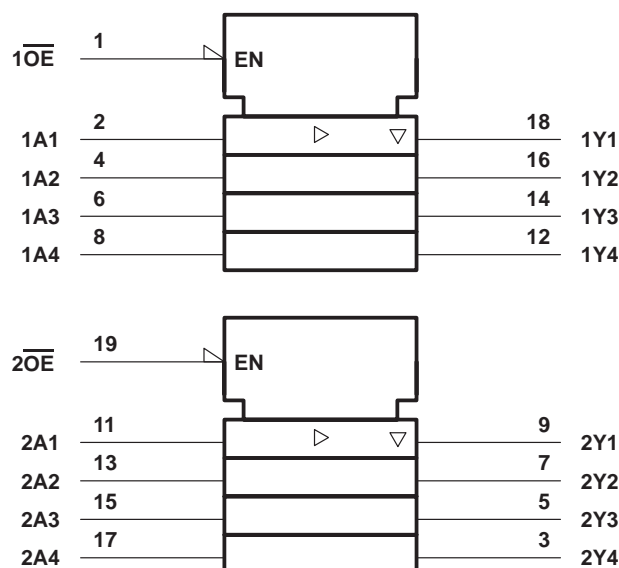
SN54LVT244, SN74LVT244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

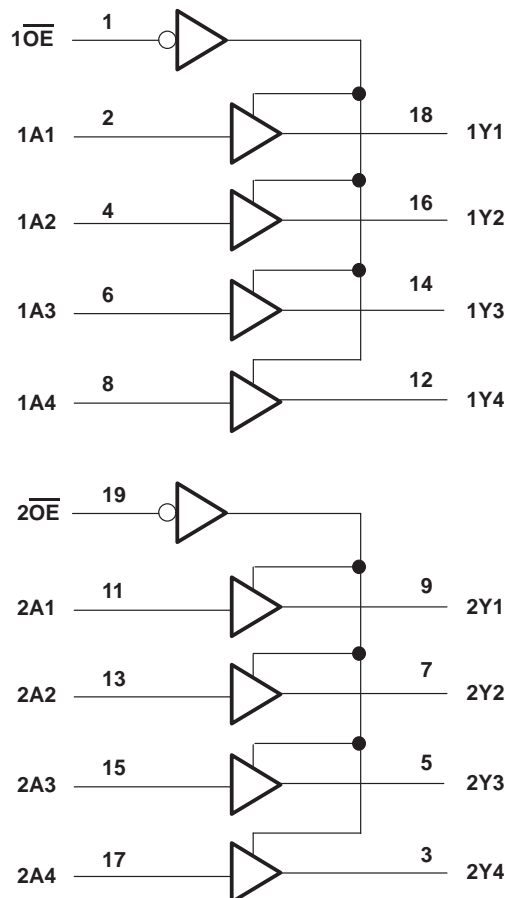
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVT244	96 mA
SN74LVT244	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT244	48 mA
SN74LVT244	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



SN54LVT244, SN74LVT244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LVT244		SN74LVT244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



SN54LVT244, SN74LVT244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT244		SN74LVT244		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 2.7 V, I _I = −18 mA			−1.2		−1.2		V
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = −100 μA			V _{CC} −0.2		V _{CC} −0.2		V
	V _{CC} = 2.7 V, I _{OH} = − 8 mA			2.4		2.4		
	V _{CC} = 3 V, I _{OH} = − 24 mA			2				
	V _{CC} = 3 V, I _{OH} = −32 mA					2		
V _{OL}	V _{CC} = 2.7 V, I _{OL} = 100 μA			0.2		0.2		V
	V _{CC} = 2.7 V, I _{OL} = 24 mA			0.5		0.5		
	V _{CC} = 3 V, I _{OL} = 16 mA			0.4		0.4		
	V _{CC} = 3 V, I _{OL} = 32 mA			0.5		0.5		
	V _{CC} = 3 V, I _{OL} = 48 mA			0.55				
	V _{CC} = 3 V, I _{OL} = 64 mA					0.55		
I _I	V _{CC} = 0 or MAX‡, V _I = 5.5 V			50		10		μA
	V _{CC} = 3.6 V, V _I = V _{CC} or GND		Control pins	±1		±1		
	V _{CC} = 3.6 V, V _I = V _{CC}		Data pins	1		1		
	V _{CC} = 3.6 V, V _I = 0			−5		−5		
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100		μA
I _{I(hold)}	V _{CC} = 3 V, V _I = 0.8 V		A inputs	75		75		μA
	V _{CC} = 3 V, V _I = 2 V			−75		−75		
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V			1		1		μA
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V			−1		−1		μA
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high	0.12 0.39		0.12 0.19		mA
			Outputs low	8.6 14		8.6 12		
			Outputs disabled	0.12 0.39		0.12 0.19		
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND			0.3		0.2		mA
C _i	V _I = 3 V or 0			4		4		pF
C _o	V _O = 3 V or 0			8		8		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT244, SN74LVT244
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT244				SN74LVT244				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN		MAX
t _{PLH}	A	Y	0.5	4.7	5.2		1	2.5	4.3	5		ns
t _{PHL}			0.5	4.4	5.4		1	2.5	4.2	5.2		
t _{PZH}	$\overline{\text{OE}}$	Y	0.8	5.4	6.5		1	2.7	5.2	6.3		ns
t _{PZL}			0.8	5.4	7.6		1.1	3.1	5.2	6.7		
t _{PHZ}	$\overline{\text{OE}}$	Y	1.5	6.2	6.9		2.1	3.9	5.6	6.3		ns
t _{PLZ}			1.2	5.5	6		1.8	3.2	5.1	5.6		

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

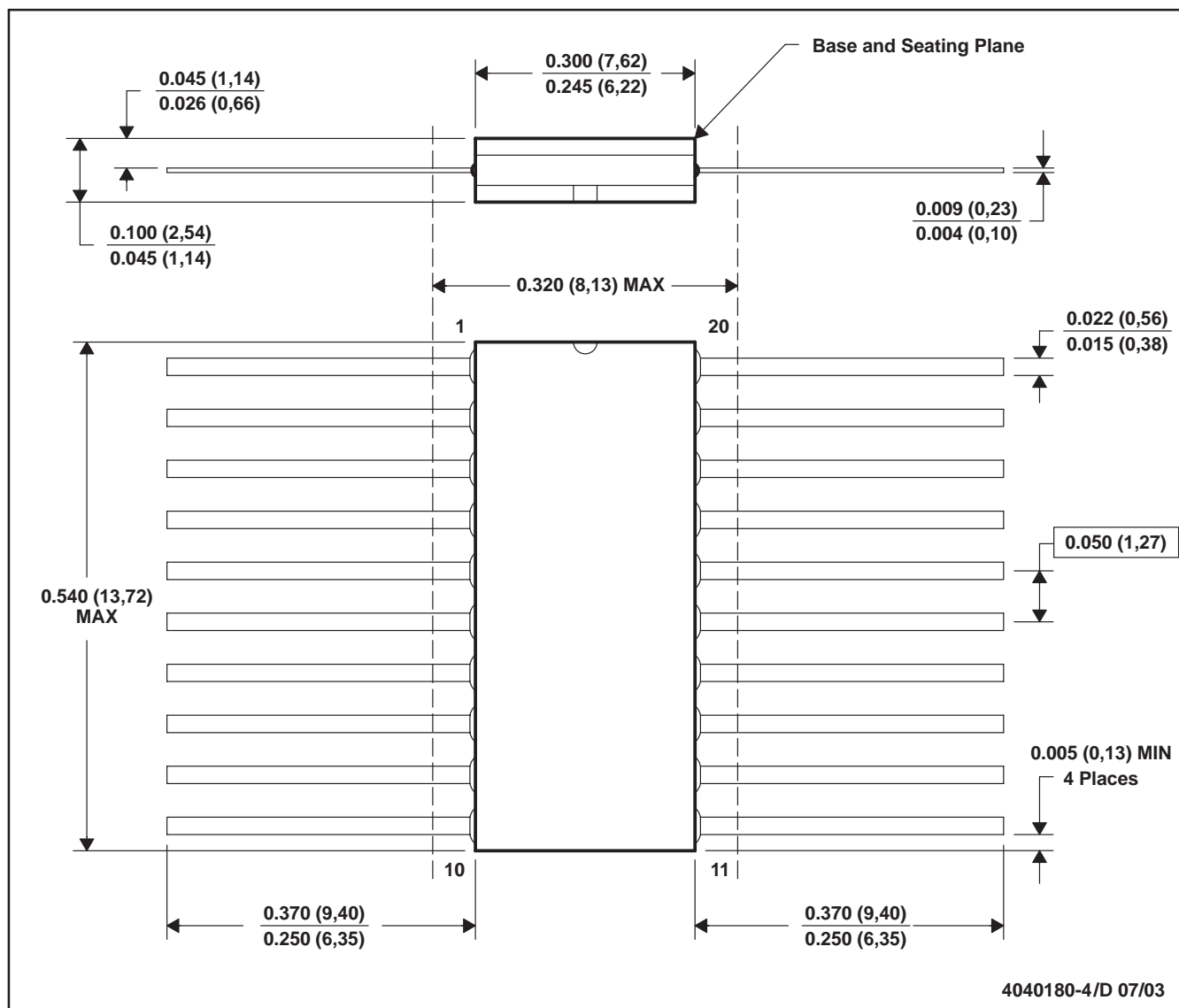


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

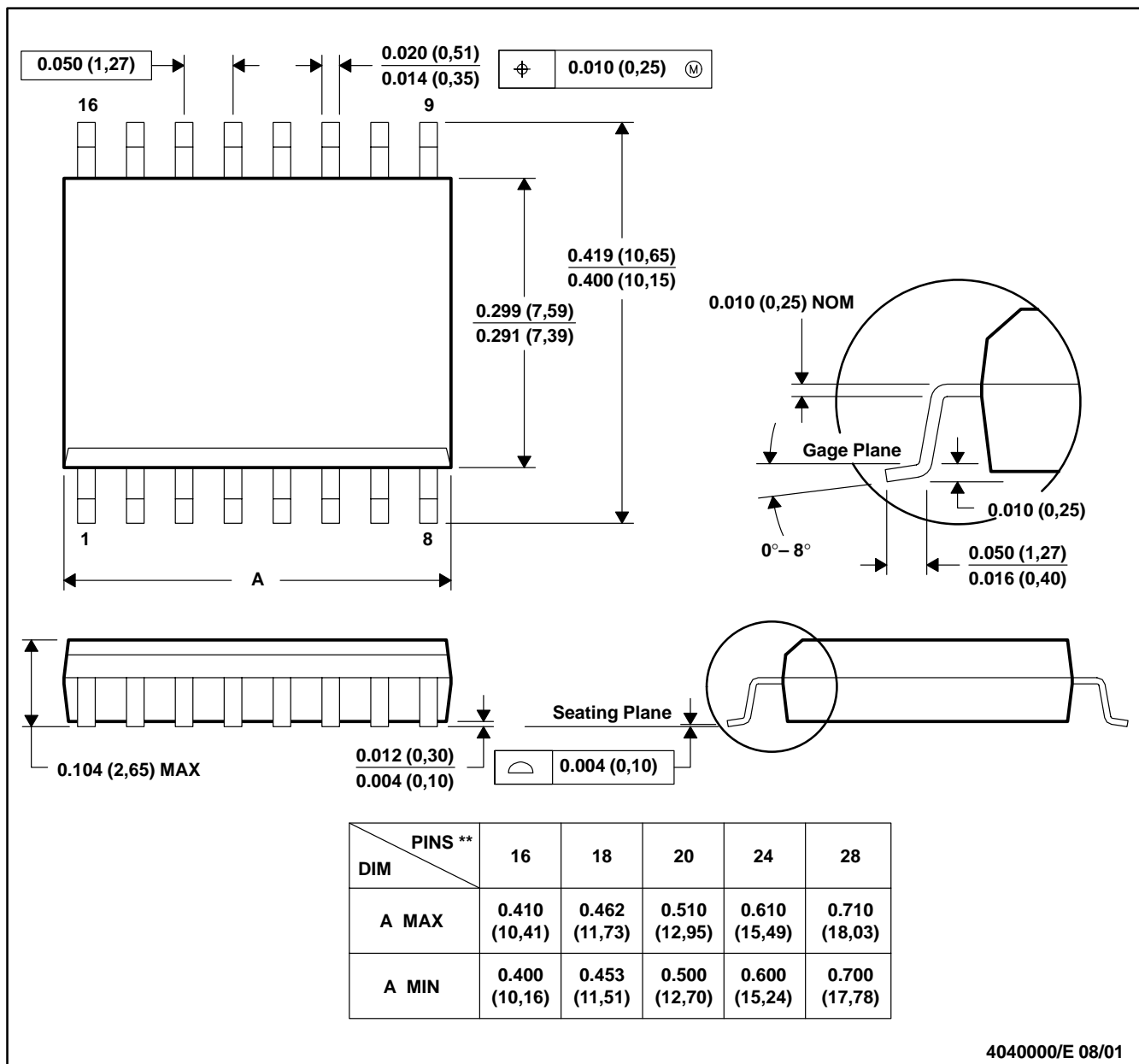


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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