

# SN74ALS29841

## 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SDAS149A – JUNE 1988 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity
- Buffered Control Inputs Reduce dc Loading Effects
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

### description

This 10-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

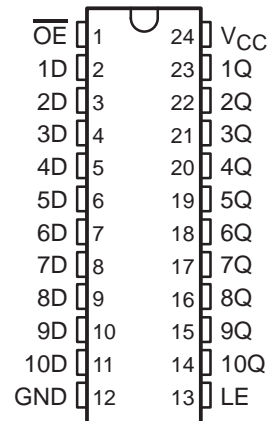
The ten latches are transparent D-type latches. The SN74ALS29841 has noninverting data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can place the ten outputs in either a normal logic state (high or low logic levels) or in a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN74ALS29841 is characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE  
(TOP VIEW)



FUNCTION TABLE

| INPUTS          |    |   | OUTPUT<br>Q |
|-----------------|----|---|-------------|
| $\overline{OE}$ | LE | D |             |
| L               | H  | H | H           |
| L               | H  | L | L           |
| L               | L  | X | $Q_0$       |
| H               | X  | X | Z           |

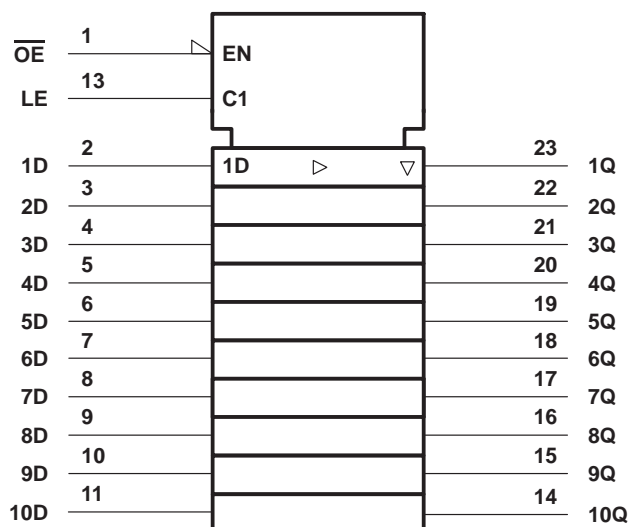
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## 10-BIT BUS-INTERFACE D-TYPE LATCH

### WITH 3-STATE OUTPUTS

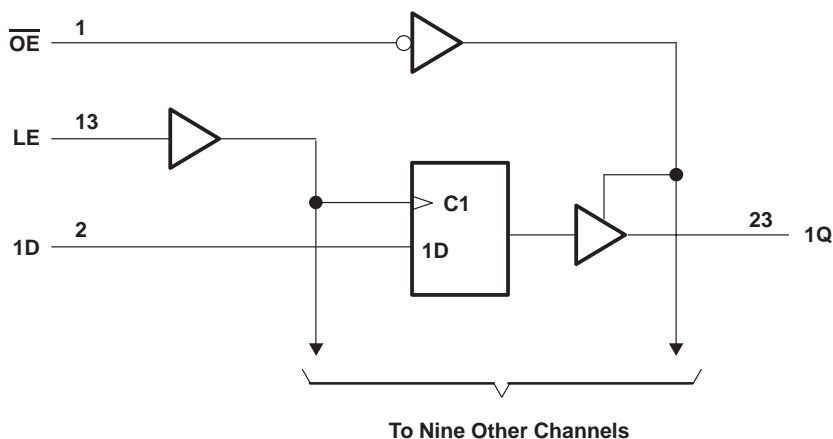
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|  |                |
|--|----------------|
| Supply voltage, $V_{CC}$                     | 7 V            |
| Input voltage, $V_I$                         | 7 V            |
| Voltage applied to a disabled 3-state output | 5.5 V          |
| Operating free-air temperature range, $T_A$  | 0°C to 70°C    |
| Storage temperature range                    | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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**recommended operating conditions**

|          |                                | MIN  | NOM | MAX  | UNIT |
|----------|--------------------------------|------|-----|------|------|
| $V_{CC}$ | Supply voltage                 | 4.75 | 5   | 5.25 | V    |
| $V_{IH}$ | High-level input voltage       | 2    |     |      | V    |
| $V_{IL}$ | Low-level input voltage        |      |     | 0.8  | V    |
| $I_{OH}$ | High-level output current      |      |     | –24  | mA   |
| $I_{OL}$ | Low-level output current       |      |     | 48   | mA   |
| $t_w$    | Pulse duration, LE high        | 6    |     |      | ns   |
| $t_{su}$ | Setup time, data before LE↓    | 2.5  |     |      | ns   |
| $t_h$    | Hold time, data after LE↓      | 4.5  |     |      | ns   |
| $T_A$    | Operating free-air temperature | 0    |     | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS                                    | MIN | TYP†                     | MAX  | UNIT |
|-----------|--|-----|--------------------------|------|------|
| $V_{IK}$  | $V_{CC} = 4.75\text{ V}$ , $I_I = -18\text{ mA}$   |     |                          | –1.2 | V    |
| $V_{OH}$  | $V_{CC} = 4.75\text{ V}$                           |     | $I_{OH} = -15\text{ mA}$ | 2.4  | 3.3  |
|           |  |     | $I_{OH} = -24\text{ mA}$ | 2    | 3.1  |
| $V_{OL}$  | $V_{CC} = 4.75\text{ V}$ , $I_{OL} = 48\text{ mA}$ |     |                          | 0.35 | 0.5  |
| $I_{OZH}$ | $V_{CC} = 5.25\text{ V}$ , $V_O = 2.7\text{ V}$    |     |                          | 20   | μA   |
| $I_{OZL}$ | $V_{CC} = 5.25\text{ V}$ , $V_O = 0.4\text{ V}$    |     |                          | –20  | μA   |
| $I_I$     | $V_{CC} = 5.25\text{ V}$ , $V_I = 5.5\text{ V}$    |     |                          | 0.1  | mA   |
| $I_{IH}$  | $V_{CC} = 5.25\text{ V}$ , $V_I = 2.7\text{ V}$    |     |                          | 20   | μA   |
| $I_{IL}$  | $V_{CC} = 5.25\text{ V}$ , $V_I = 0.4\text{ V}$    |     |                          | –0.2 | mA   |
| $I_{OS}‡$ | $V_{CC} = 5.25\text{ V}$ , $V_O = 0$               | –75 |                          | –250 | mA   |
| $I_{CC}$  | $V_{CC} = 5.25\text{ V}$ , Outputs low             |     | 55                       | 85   | mA   |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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#### switching characteristics (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS         | V <sub>CC</sub> = MIN to MAX†, T <sub>A</sub> = MIN to MAX† |     | UNIT |
|------------------|-----------------|----------------|-------------------------|---|-----|------|
|                  |                 |                |                         | MIN   | MAX |      |
| t <sub>PLH</sub> | D               | Any Q          | C <sub>L</sub> = 50 pF  | 2   | 9.5 | ns   |
| t <sub>PHL</sub> |                 |                |                         | 2   | 9.5 |      |
| t <sub>PLH</sub> | D               | Any Q          | C <sub>L</sub> = 300 pF |   | 14  | ns   |
| t <sub>PHL</sub> |                 |                |                         |   | 14  |      |
| t <sub>PLH</sub> | LE              | Any Q          | C <sub>L</sub> = 50 pF  |   | 12  | ns   |
| t <sub>PHL</sub> |                 |                |                         |   | 12  |      |
| t <sub>PLH</sub> | LE              | Any Q          | C <sub>L</sub> = 300 pF |   | 16  | ns   |
| t <sub>PHL</sub> |                 |                |                         |   | 16  |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Any Q          | C <sub>L</sub> = 50 pF  |   | 14  | ns   |
| t <sub>PZL</sub> |                 |                |                         |   | 14  |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Any Q          | C <sub>L</sub> = 300 pF |   | 20  | ns   |
| t <sub>PZL</sub> |                 |                |                         |   | 23  |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Any Q          | C <sub>L</sub> = 50 pF  |   | 15  | ns   |
| t <sub>PLZ</sub> |                 |                |                         |   | 12  |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Any Q          | C <sub>L</sub> = 5 pF   |   | 9   | ns   |
| t <sub>PLZ</sub> |                 |                |                         |   | 9   |      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

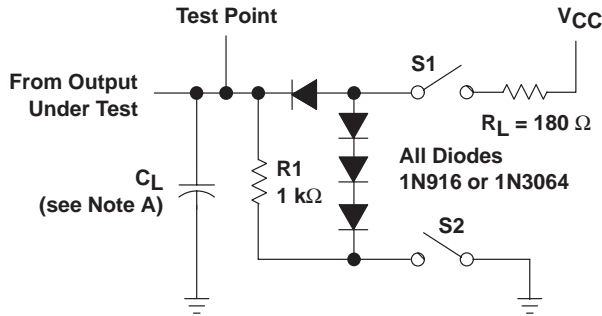
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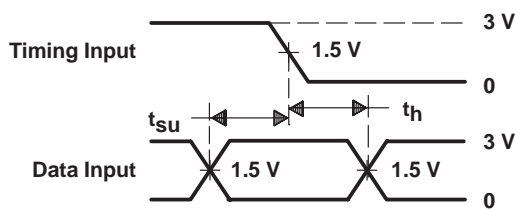
#### PARAMETER MEASUREMENT INFORMATION



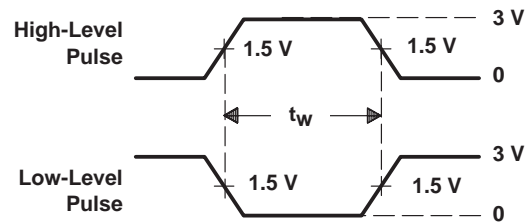
LOAD CIRCUIT

SWITCH POSITION TABLE

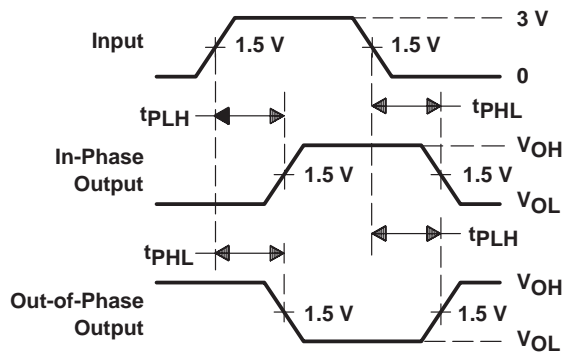
| TEST      | S1     | S2     |
|-----------|--------|--------|
| $t_{PLH}$ | Closed | Closed |
| $t_{PHL}$ | Closed | Closed |
| $t_{PZH}$ | Open   | Closed |
| $t_{PZL}$ | Closed | Open   |
| $t_{PHZ}$ | Closed | Closed |
| $t_{PLZ}$ | Closed | Closed |



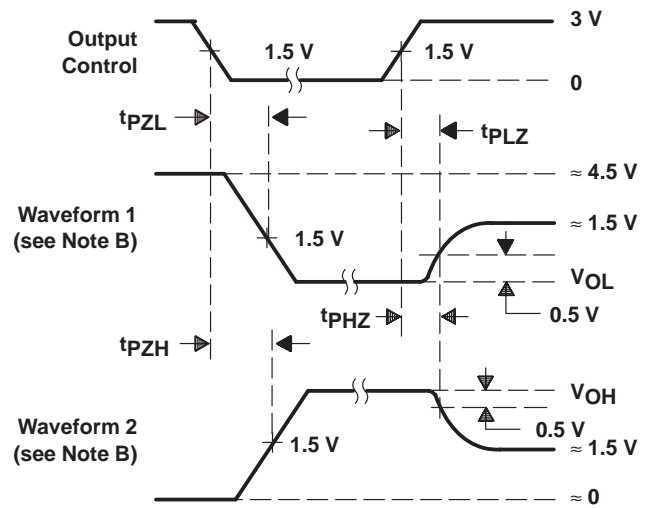
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

Figure 1. Load Circuit and Voltage Waveforms

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